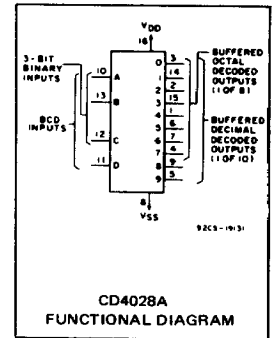


CMOS BCD-to-Decimal Decoder

The RCA-CD4028A types are BCD-to-decimal or binary-to-octal decoders consisting of pulse-shaping circuits on all 4 inputs, decoding logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7. A high-level signal at the D input inhibits octal decoding and causes outputs

0 through 7 to go low. If unused, the D input must be connected to VSS. High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltages references to VSS Terminal)	-0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR $T_A = -40$ to +60°C (PACKAGE TYPE E)	500 mW
FOR $T_A = +60$ to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR $T_A = -55$ to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR $T_A = +100$ to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to $V_{DD} + 0.5$ V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

Features:

- BCD-to-decimal decoding or binary-to-octal decoding
- High decoded output drive capability 8 mA (typ.) sink or source
- "Positive logic" inputs and outputs. decoded outputs go high on selection
- Medium-speed operation
- . . . $t_{HL}, t_{LH} = 30$ ns (typ.) @ $V_{DD} = 10$ V
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μ A at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Code conversion
- Address decoding—memory selection control
- Indicator-tube decoder

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V _{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E PACKAGE		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T _A =Full Package-Temperature Range)		3	12	3	12	V

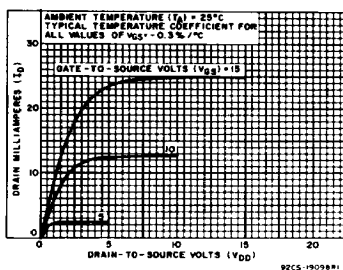


Fig. 1 — Typical output n-channel drain characteristics.

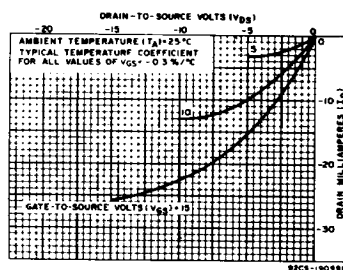


Fig. 2 — Typical output p-channel drain characteristics.

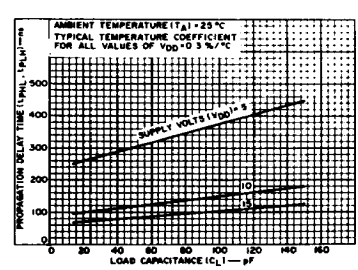


Fig. 3 — Typical propagation delay time vs. C_L .

CD4028A Types

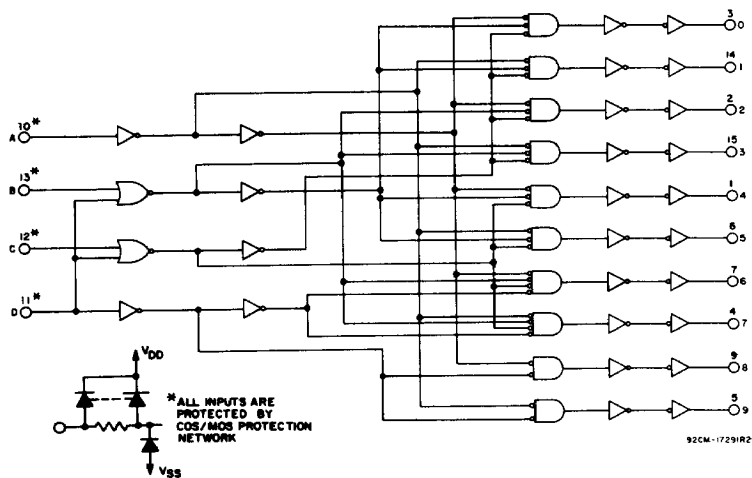


Fig. 4 — Logic diagram.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, F, K, H PACKAGES				E PACKAGE				
	VO (V)	VIN (V)	VDD (V)	-55	+25		+125	-40	+25		+85	
					TYP.	LIMIT			TYP.	LIMIT		
Quiescent Device Current, IL Max.	—	—	5	5	0.5	5	300	50	5	50	700	μA
	—	—	10	10	1	10	600	100	10	100	1400	
	—	—	15	50	1	50	2000	500	10	500	5000	
Output Voltage: Low-Level, VOL	—	5	5	0 Typ.; 0.05 Max.								V
	—	10	10	0 Typ.; 0.05 Max.								
	—	0	5	4.95 Min.; 5 Typ.								
	—	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, VNL	4.2	—	5	1.5 Min.; 2.25 Typ.								V
	9	—	10	3 Min.; 4.5 Typ.								
	0.8	—	5	1.5 Min.; 2.25 Typ.								
	1	—	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, VNML	4.5	—	5	1 Min.								V
	9	—	10	1 Min.								
	0.5	—	5	1 Min.								
	1	—	10	1 Min.								
Output Drive Current N-Channel (Sink), IDN Min.	0.5	—	5	0.75	1.2	0.6	0.45	0.35	1.2	0.3	0.25	mA
	0.5	—	10	1.5	2.4	1.2	0.9	0.7	2.4	0.6	0.5	
	4.5	—	5	-0.7	-0.9	-0.45	-0.32	-0.32	-0.9	-0.22	-0.18	
	9	—	10	-1.4	-1.9	-0.95	-0.65	-0.65	-1.9	-0.48	-0.4	
Input Leakage Current, IIL, IIH	Any Input			±10 ⁻⁵ Typ., ±1 Max.								μA
	—	—	15									

TABLE I — TRUTH TABLE

DCBA	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	1
1	1	0	0	1	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

* WHERE 1 = HIGH LEVEL
0 = LOW LEVEL

** EXTRAORDINARY
STATES

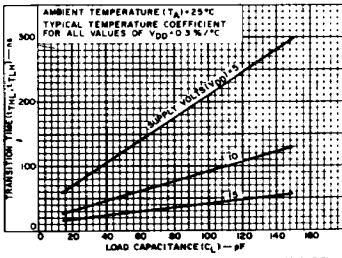


Fig. 5 — Typical transition time vs. C_L .

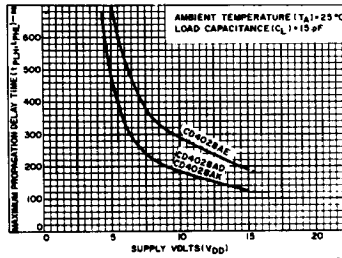


Fig. 6 — Maximum propagation delay time vs. V_{DD} .

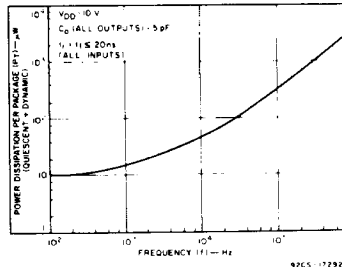


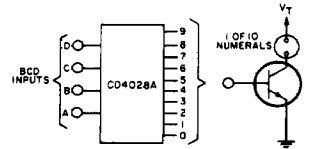
Fig. 7 — Dissipation vs. input frequency.

CD4028A Types

DYNAMIC ELECTRICAL CHARACTERISTICS

at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$, $C_L = 15\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS	
		D, F, K, H PACKAGES			E PACKAGE				
		VDD (V)	MIN.	TYP.	MAX.	MIN.	TYP.		MAX.
Propagation Delay Time; tPLH, tPHL		5	—	250	480	—	250	700	ns
		10	—	100	180	—	100	290	
Transition Time; tTHL, tTLH		5	—	60	150	—	60	300	ns
		10	—	30	75	—	30	150	
Average Input Capacitance, Ci	Any Input	—	5	—	—	5	—	pF	



▲ (Trademark) Burroughs Corp.

92CS-17295M

TUBE REQUIREMENTS

Type	V_T (Vdc)	mA/numeral
Burroughs 840B1	170	1.4
84336/718	170	2
84002	170	1.4
84021	120	1.4

TRANSISTOR CHARACTERISTICS

Leakage with transistor cutoff $\leq 0.05\text{ mA}$

$V_{BIAS} \geq 70\text{ V}$

Fig. 9 — Neon readout (Nixie Tube[▲]) display application.

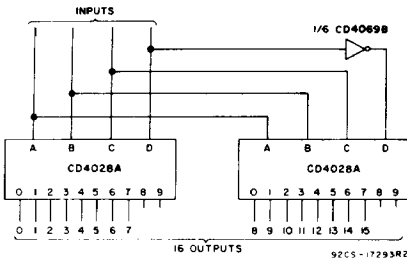


Fig. 8 — Code conversion circuit.

The circuit shown in Fig. 9 converts any 4-bit code to a decimal or hexadecimal code. Table 2 shows a number of codes and the decimal or hexadecimal number in these codes which must be applied to the input terminals of the CD4028A to select a particular output. For example: in order to get a high on output No. 8 the input must be either an 8 expressed in 4-Bit Binary code, a 15 expressed in 4-Bit Gray code, or a 5 expressed in Excess-3 code.

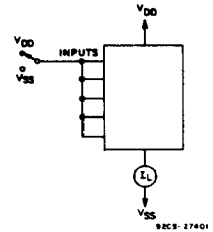


Fig. 10 — Quiescent device current test circuit.

TABLE II — CODE CONVERSION CHART

INPUTS				INPUT CODES						OUTPUT NUMBER															
				Hexa-Decimal	Decimal	EXCESS-3	GRAY	AIKEN	4-2-1																
D	C	B	A	4BIT BINARY	4BIT GRAY	EXCESS-3	GRAY	AIKEN	4-2-1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0				0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1				1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	2	3			0	2	2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	3	2		0	3	3	3	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	4	7		1	4	4	4	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	0	1	5	6		2		3	3	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	0	6	4		3	1	4	4	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
0	1	1	1	7	5		4	2			0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	0	8	15		5				0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	0	1	9	14		6		5	5	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	10	12		7	9	6	6	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	11	13		8		5		0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	12	8		9	5	6		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	13	9		6	7	7		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	14	11		8	8	8		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	15	10		7	9	9		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

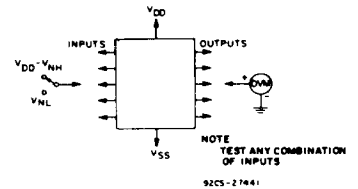


Fig. 11 — Noise-immunity test circuit.

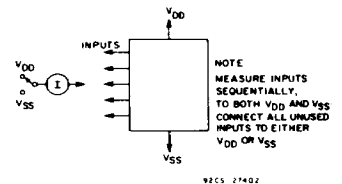


Fig. 12 — Input-leakage-current test circuit.