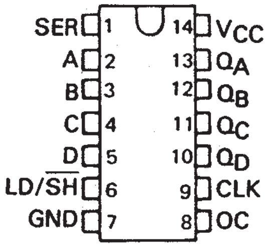
SN54LS295B, SN74LS295B
4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS WITH 3-STATE OUTPUTS

SDLS154 – OCTOBER 1975 – REVISED MARCH 1988

- **'LS295B Offers Three Times the Sink-Current Capability of 'LS295A**
- **Schottky-Diode-Clamped Transistors**
- **Low Power Dissipation . . . 80 mW Typical (Enabled)**
- **Applications:**
  - **N-Bit Serial-To-Parallel Converter**
  - **N-Bit Parallel-To-Serial Converter**
  - **N-Bit Storage Register**

SN54LS295B . . . J OR W PACKAGE
SN74LS295B . . . D OR N PACKAGE
(TOP VIEW)



description

These 4-bit registers feature parallel inputs, parallel outputs, and clock (CLK), serial (SER), mode (LD/$\overline{SH}$), and outputs control (OC) inputs. The registers have three modes of operation:

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

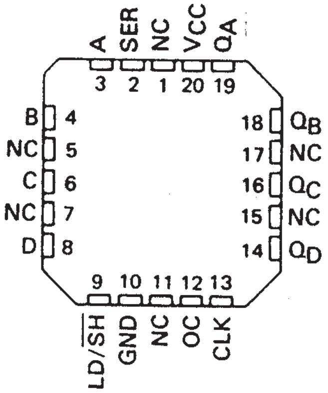
Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

Shift right is accomplished when the mode control is low; shift left is accomplished when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D.

When the output control is high, the normal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a low logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus line; however, sequential operation of the registers is not affected.

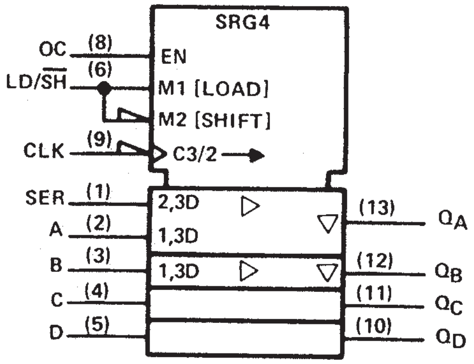
The SN54LS295B is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74LS295B is characterized for operation from 0°C to 70°C.

SN54LS295B . . . FK PACKAGE
(TOP VIEW)



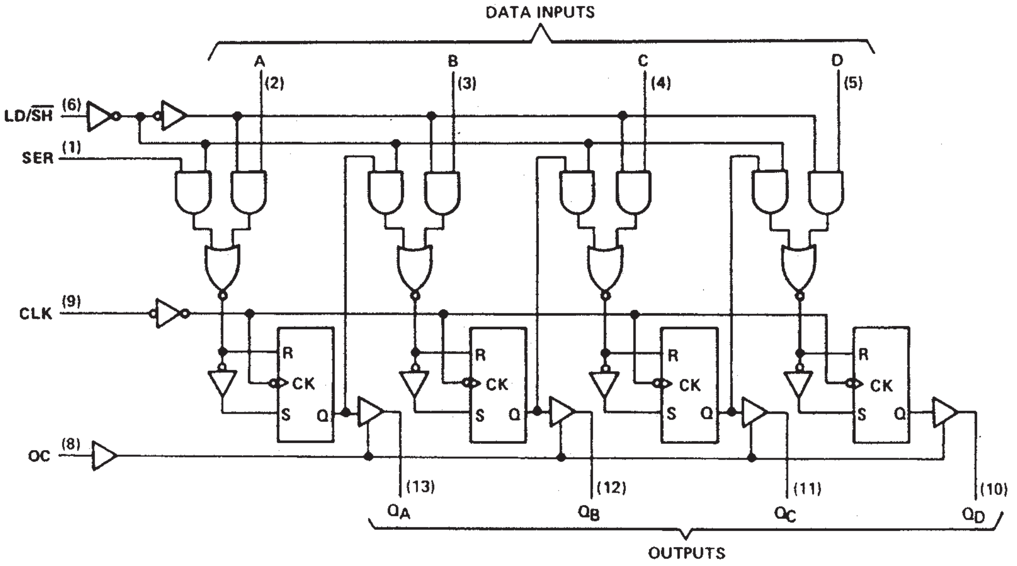
NC - No internal connection

logic symbol†



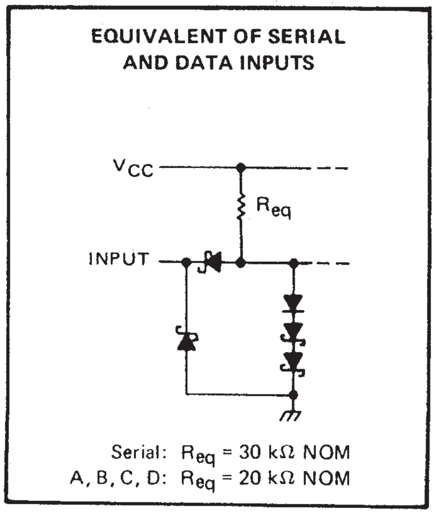
† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

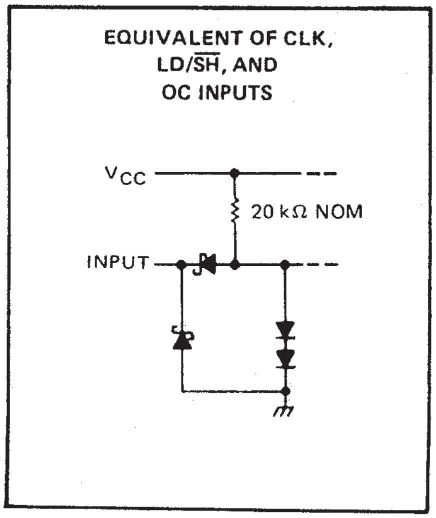
logic diagram (positive logic)

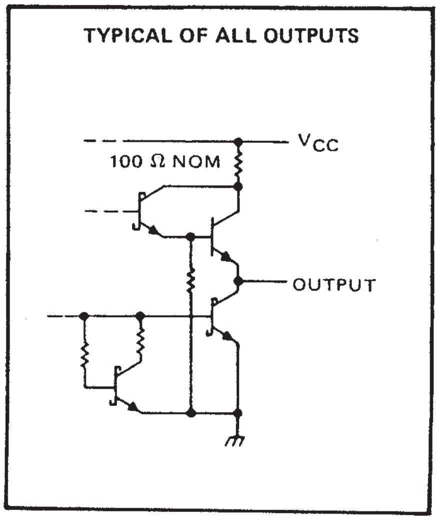


Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs







FUNCTION TABLE

INPUTS							OUTPUTS			
LD/$\overline{\text{SH}}$	CLK	SER	PARALLEL				Q_A	Q_B	Q_C	Q_D
			A	B	C	D				
H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	a	b	c	d	a	b	c	d
H	↓	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
When the output control is low, the outputs are disabled to the high-impedance state; however, sequential operation of the registers is not affected.										

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)

↓ = transition from high to low level.

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage		7 V
Operating free-air temperature range:	SN54LS295B	–55°C to 125°C
	SN74LS295B	0°C to 70°C
Storage temperature range		–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS295B			SN74LS295B			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current				– 1			– 2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency		0		30	0		30	MHz
$t_{w(clock)}$	Width of clock pulse		16			16			ns
t_{su}	Setup time, high-level or low-level data		20			20			ns
t_{su}	Setup time, LD/$\overline{\text{SH}}$ to CLK	high-level	25			25			ns
		low-level	30			30			
t_h	Hold time, high-level or low-level data		20			20			ns
t_h	Hold time, high-level or low-level LD/$\overline{\text{SH}}$ to CLK		0			0			ns
T_A	Operating free-air temperature		– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS295B			SN74LS295B			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = -18$ mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, $V_{IL} = V_{IL}$ max, I_{OH} = MAX		2.4	3.4		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, $V_{IL} = V_{IL}$ max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, $V_{IL} = V_{IL}$ max, V_O = 2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.4 V				−20			−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	Condition A		20	29		20	29	mA
			Condition B		22	33		22	33	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time,and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with the outputs open, the serial input and mode control at 4.5 V, and the data inputs grounded under the following conditions:

A. Output control at 4.5 V and a momentary 3 V, then ground, applied to clock input.
B. Output control and clock input grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25 C, R_L = 667 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 45 pF, See Note 3	30	45		MHz
t_{PLH}	Propagation delay time, low-to-high-level output			14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			19	30	ns
t_{PZH}	Output enable time to high level			18	26	ns
t_{PZL}	Output enable time to low level			20	30	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF, See Note 3		13	20	ns
t_{PLZ}	Output disable time from low level			13	20	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN54LS295BJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN74LS295BN	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS295BN	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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