Numbers in parenthesis denote pin numbers for F package (Case 650).

FUNCTIONS AND CHARACTERISTICS (continued)

Function	Type ①		Propagation Delay ns typ	Power Dissipation mW typ/pkg*	Case
	-30 to +85°C	-55 to +125°C			
Universal Decade Counter	MC10137	MC10537	f = 150 MHz	625	620,650
Bi-Quinary Counter	MC10138	–	f = 150 MHz	370	620
64-Bit Random Access Memory (90 Ω)	MCM10140	–	t_{Access} = 15 (max)	420	620,690
Four-Bit Universal Shift Register	MC10141	MC10541	f = 200 MHz	425	620,648,650
64-Bit Random Access Memory (50 Ω)	MCM10142	–	t_{Access} = 10 (max)	420	620
8 x 2 Multiport Register File (RAM)	MCM10143	–	t_{Access} = 10	610	623
256-Bit Random Access Memory	MCM10144	–	t_{Access} = 30 (max)	420	620,690
64-Bit Register File (RAM)	MCM10145	–	t_{Access} = 10	625	620
128-Bit Random Access Memory	MCM10147	–	t_{Access} = 12 (max)	420	620
64-Bit Random Access Memory (50 Ω)	MCM10148	–	t_{Access} = 15 (max)	420	620
1024-Bit Programmable Read Only Memory	MCM10150	–	t_{Access} = 20	–	690
Quad Latch	MC10153	–	4.0	310	620
12-Bit Parity Generator-Checker	MC10160	MC10560	5.0	320	620,648,650
Binary to 1-8 Decoder (Low)	MC10161	MC10561	4.0	315	620,648,650
Binary to 1-8 Decoder (High)	MC10162	MC10562	4.0	315	620,648,650
Error Detection-Correction Circuit	MC10163	–	5.0	520	620
8-Line Multiplexer	MC10164	MC10564	3.0	310	620,648,650
8-Input Priority Encoder	MC10165	–	7.0	545	620,648
5-Bit Magnitude Comparator	MC10166	–	6.0	440	620
Quad Latch	MC10168	–	3.0	310	620
Dual Binary To 1-4 Decoder (Low)	MC10171	MC10571	4.0	325	620,648,650
Dual Binary To 1-4 Decoder (High)	MC10172	MC10572	4.0	325	620,648,650
Quad 2-Input Multiplexer/Latch	MC10173	–	2.5	275	620,648
Dual 4 To 1 Multiplexer	MC10174	MC10574	3.5	305	620,650
Quint Latch	MC10175	MC10575	2.5	400	620
Hex "D" Master-Slave Flip-Flop	MC10176	–	f = 250 MHz	460	620
Triple MECL to NMOS Translator	MC10177	–	–	1.0 W	620
Binary Counter	MC10178	–	f = 150 MHz	370	620
Look-Ahead Carry Block	MC10179	MC10579	3.0 (Cn,P) 4.0 (G)	300	620,648,650
Dual High Speed Adder/Subtractor	MC10180	MC10580	4.5	360	620,648,650
4-Bit Arithmetic Logic Unit/Function Generator	MC10181	MC10581	See Logic Diag.	600	623,649,652
2-Bit Arithmetic Logic Unit/Function Generator	MC10182	–	See Logic Diag.	575	620
Error Detection-Correction Circuit	MC10193	–	7.5	520	620
Hex Inverter/Buffer	MC10195	–	2.0	200	620
Hex "AND" Gate	MC10197	–	2.8	200	620
High Speed Dual 3-Input 3-Output OR Gate	MC10210	–	1.5	160	620
High Speed Dual 3-Input 3-Output NOR Gate	MC10211	–	1.5	160	620
High Speed Dual 3-Input 3-Output OR/NOR Gate	MC10212	–	1.5	160	620
High Speed Triple Line Receiver	MC10216	MC10616	1.8	100	620,648,650
High Speed Dual Type D Master-Slave Flip-Flop	MC10231	MC10631	f = 225 MHz	270	620,648,650
High Speed 2 x 1 Bit Array Multiplier Block	MC10287	–	–	400	620

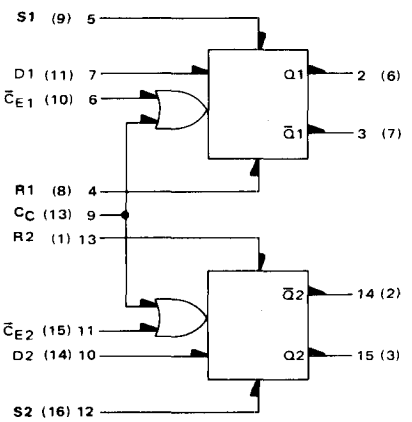
① L suffix denotes Dual In-Line Ceramic Package, P suffix denotes Dual In-Line Plastic Package, F suffix denotes flat package (i.e., MC10100L = Ceramic Dual In-Line Package, MC10100P = Plastic Dual In-Line Package and MC10500F = Ceramic Flat Package.)

*Load Power not included

FLIP-FLOPS

MC10131,MC10531
MC10231,MC10631

Dual Type D Master-Slave Flip-Flop



MC10131, MC10531
P_D = 235 mW typ/pkg (No Load)
f = 160 MHz typ

MC10231, MC10631
P_D = 270 mW typ/pkg (No Load)
f = 225 MHz typ

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

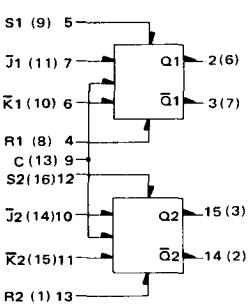
CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	L	L
H	H	H

ϕ = Don't Care
$C = \bar{C}_E + C_C$

MC10135
MC10535

Dual J-K Master-Slave Flip-Flop



R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

CLOCK J-K TRUTH TABLE*

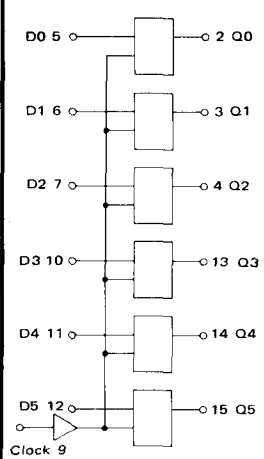
$\bar{J}$	$\bar{K}$	Q_{n+1}
L	L	$\bar{Q}_n$
H	L	L
L	H	H
H	H	Q_n

*Output states change on positive transition of clock for $\bar{J}$-$\bar{K}$ input-condition present.

P_D = 280 mW typ/pkg (No Load)
f_{tog} = 140 MHz typ

MC10176

Hex "D" Master-Slave Flip-Flop



CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H*	L	L
H*	H	H

ϕ = Don't Care.
*A clock H is a clock transition from a low to a *high* state.

P_D = 460 mW typ/pkg (No Load)
f_{tog} = 150 MHz typ

HIGH SPEED DUAL TYPE D
MASTER-SLAVE
FLIP-FLOP

MC10631

The MC10631 is a dual master-slave type D flip-flop. Asynchronous inputs Set (S) and Reset (R) override the Clock (C_C) and Clock Enable ($\overline{C}_E$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}. Output rise and fall times have been optimized to provide relaxation of system design and layout criteria.

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

CLOCKED TRUTH TABLE

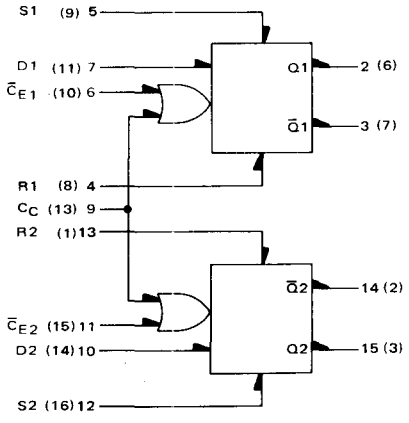
C	D	Q_{n+1}
L	ϕ	Q_n
H	L	L
H	H	H

ϕ = Don't Care
$C = \overline{C}_E + C_C$.
A clock H is a clock transition from a low to a high state.

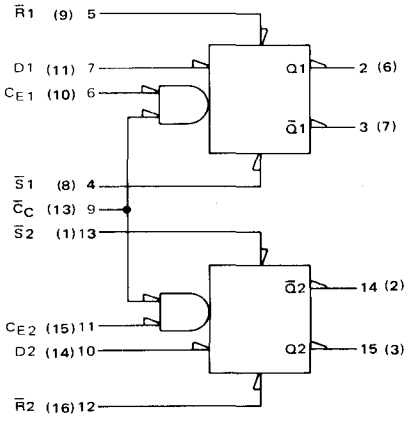
CASE	V_{CC1}	V_{CC2}	V_{EE}
620	Pin 1	Pin 16	Pin 8
650	Pin 5	Pin 4	Pin 12

P_D = 270 mW typ/pkg (No Load)
f_{Tog} = 225 MHz typ

POSITIVE LOGIC



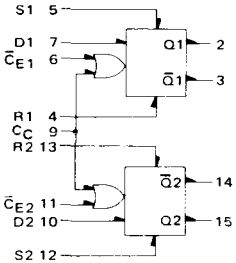
NEGATIVE LOGIC

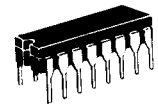


Numbers at ends of terminals denote pin numbers for L package (Case 620).
Numbers in parenthesis denote pin numbers for F package (Case 650).

ELECTRICAL CHARACTERISITCS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs are tested in the same manner.





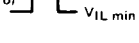
L SUFFIX
CERAMIC PACKAGE
CASE 620

T_{er} @ Test Temperature	TEST VOLTAGE VALUES Vdc ± 1% V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10631L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	72	–	52	65	–	72	mAdc	–	–	–	–	8	1, 16
Input Current	I_{inH}	4	–	700	–	–	410	–	410	µAdc	4	–	–	–	8	1, 16
		5	–	700	–	–	410	–	410		5	–	–	–		
		6	–	375	–	–	220	–	220		6	–	–	–		
		7	–	375	–	–	220	–	220		7	–	–	–		
		9	–	495	–	–	290	–	290		9	–	–	–		
Input Leakage Current	I_{inL}	4,5,*	0.5	–	0.5	–	–	0.3	–	µAdc	–	*	–	–	8	1, 16
		6,7,9*	0.5	–	0.5	–	–	0.3	–	µAdc	–	*	–	–	8	1, 16
Logic "1" Output Voltage	V_{OH}	2	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	5	–	–	–	8	1, 16
		2†	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	7	–	–	–	8	1, 16
Logic "0" Output Voltage	V_{OL}	3	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	5	–	–	–	8	1, 16
		3†	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	7	–	–	–	8	1, 16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	5	–	8	1, 16
		2†	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	7	9	8	1, 16
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	5	–	8	1, 16
		3†	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	7	9	8	1, 16
Switching Times (100-ohm load) Clock Input											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse Out	-3.2 Vdc	+2.0 Vdc
Propagation Delay	t_{9+2-}	2	–	–	1.5	2.0	3.3	–	–	ns	–	–	9	2	8	1, 16
	t_{6+2+}		–	–	1.5	2.0	3.3	–	–		7	–	6			
Rise Time (20 to 80%)	t_{2+}		–	–	1.0	1.3	3.1	–	–		7	–	9			
Fall Time (20 to 80%)	t_{2-}		–	–	1.0	1.3	3.1	–	–		–	–	9			
Set Input Propagation Delay	t_{5+2+}	2	–	–	1.1	2.0	3.3	–	–	ns	–	–	5	2	8	1, 16
	t_{12+15+}	15	–	–				–	–		–	–	12	15		
	t_{5+3-}	3	–	–				–	–		–	–	5	3		
	t_{12+14-}	14	–	–				–	–		–	–	12	14		
Reset Input Propagation Delay	t_{4+2-}	2	–	–	1.1	2.0	3.3	–	–	ns	–	–	4	2	8	1, 16
	t_{13+15-}	15	–	–				–	–		–	–	13	15		
	t_{4+3+}	3	–	–				–	–		–	–	4	3		
	t_{13+14+}	14	–	–				–	–		–	–	13	14		
Setup Time	t_{setup}	7	–	–	1.0	0.75	–	–	–	ns	–	–	6,7	2	8	1, 16
Hold Time	t_{hold}	7	–	–	0.75	-0.5	–	–	–	ns	–	–	6,7	2	8	1, 16
Toggle Frequency (Max)	f_{Tog}	2	200	–	200	225	–	200	–	MHz	••	–	6	2	8	1, 16

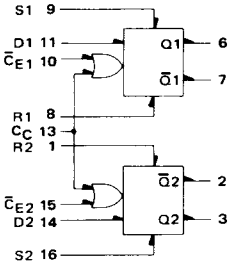
*Individually test each input; apply V_{IL} min to pin under test.

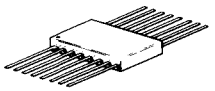
**Pin 3 is tied to pin 7 for these tests.

†Output level to be measured after a clock pulse has been applied to the $\bar{C}_E$ input (pin 6)  V_{IH} max, V_{IL} min

ELECTRICAL CHARACTERISITCS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs are tested in the same manner.





F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES Vdc ± 1% V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC10631F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	12	–	62	–	45	65	–	62	mAdc	–	–	–	–	12	4,5
Input Current	I_{inH}	8	–	700	–	–	410	–	410	µAdc	8	–	–	–	12	4,5
		9	–	700	–	–	410	–	410		9	–	–	–		
		10	–	375	–	–	220	–	220		10	–	–	–		
		11	–	375	–	–	220	–	220		11	–	–	–		
		13	–	495	–	–	290	–	290		13	–	–	–		
Input Leakage Current	I_{inL}	8,9*	0.5	–	0.5	–	–	0.3	–	µAdc	–	*	–	–	12	4,5
		10,11,13*	0.5	–	0.5	–	–	0.3	–	µAdc	–	*	–	–	12	4,5
Logic "1" Output Voltage	V_{OH}	6	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	9	–	–	–	12	4,5
		6†	-1.080	-0.880	-0.930	–	-0.780	-0.825	-0.630	Vdc	11	–	–	–	12	4,5
Logic "0" Output Voltage	V_{OL}	7	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	9	–	–	–	12	4,5
		7†	-1.920	-1.655	-1.850	–	-1.620	-1.820	-1.545	Vdc	11	–	–	–	12	4,5
Logic "1" Threshold Voltage	V_{OHA}	6	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	9	–	12	4,5
		6†	-1.100	–	-0.950	–	–	-0.845	–	Vdc	–	–	11	13	12	4,5
Logic "0" Threshold Voltage	V_{OLA}	7	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	9	–	12	4,5
		7†	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	11	13	12	4,5
											+1.11 Vdc	+0.31 Vdc	Pulse In	Pulse In	-3.2 Vdc	+2.0 Vdc
Switching Times (100-ohm load)	t_{13+6-}	6	–	–	1.5	2.0	3.3	–	–	ns	–	–	13	6	12	4,5
Clock Input Propagation Delay	t_{13+6+}	6	–	–				–	–		11	–	13			
	t_{10+6+}	6	–	–				–	–		11	–	10			
	t_{10+6-}	6	–	–				–	–		–	–	10			
Rise Time (20 to 80%)	t_{6+}	6	–	–	1.0	1.3	3.1	–	–		–	–	13			
Fall Time (20 to 80%)	t_{6-}	6	–	–	1.0	1.3	3.1	–	–		–	–	13			
Set Input Propagation Delay	t_{9+6+}	6	–	–	1.1	2.0	3.0	–	–	ns	–	–	9	6	12	4,5
	t_{16+3+}	3	–	–				–	–		–	–	16	3		
	t_{9+7-}	7	–	–				–	–		–	–	9	7		
	t_{16+2-}	2	–	–				–	–		–	–	16	2		
Reset Input Propagation Delay	t_{8+6-}	6	–	–	1.1	2.0	3.3	–	–	ns	–	–	8	6	12	4,5
	t_{1+3-}	3	–	–				–	–		–	–	1	3		
	t_{8+7+}	7	–	–				–	–		–	–	8	7		
	t_{1+2+}	2	–	–				–	–		–	–	1	2		
Setup Time	t_{setup}	11	–	–	1.0	0.75	–	–	–	ns	–	–	10,11	6	12	4,5
Hold Time	t_{hold}	11	–	–	0.75	-0.5	–	–	–	ns	–	–	10,11	6	12	4,5
Toggle Frequency (Max)	f_{Tog}	6	–	–	200	250	–	–	–	MHz	**	–	10	6	12	4,5

*Individually test each input; apply V_{IL} min to pin under test.

**Pin 7 is tied to pin 11 for these tests.

†Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ input (pin 10)

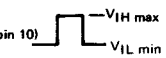


FIGURE 1 – TOGGLE FREQUENCY TEST CIRCUIT

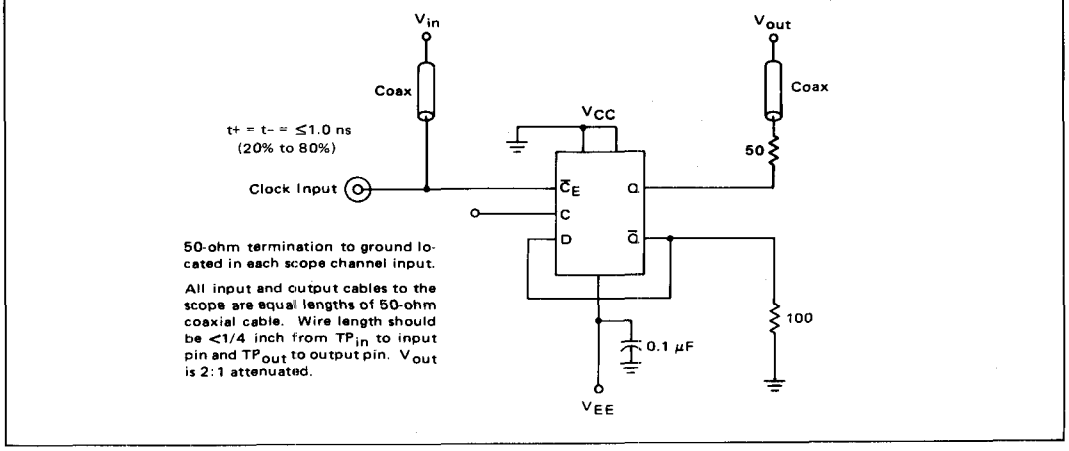
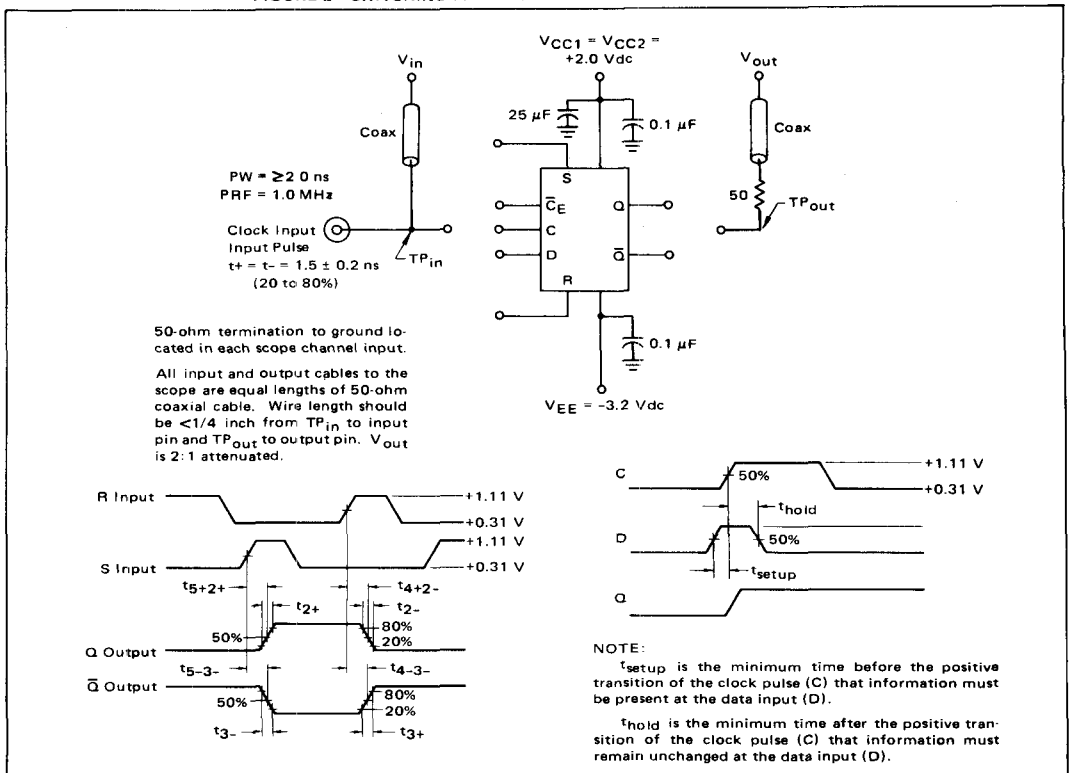


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).