CY14B256L

256 Kbit (32K x 8) nvSRAM

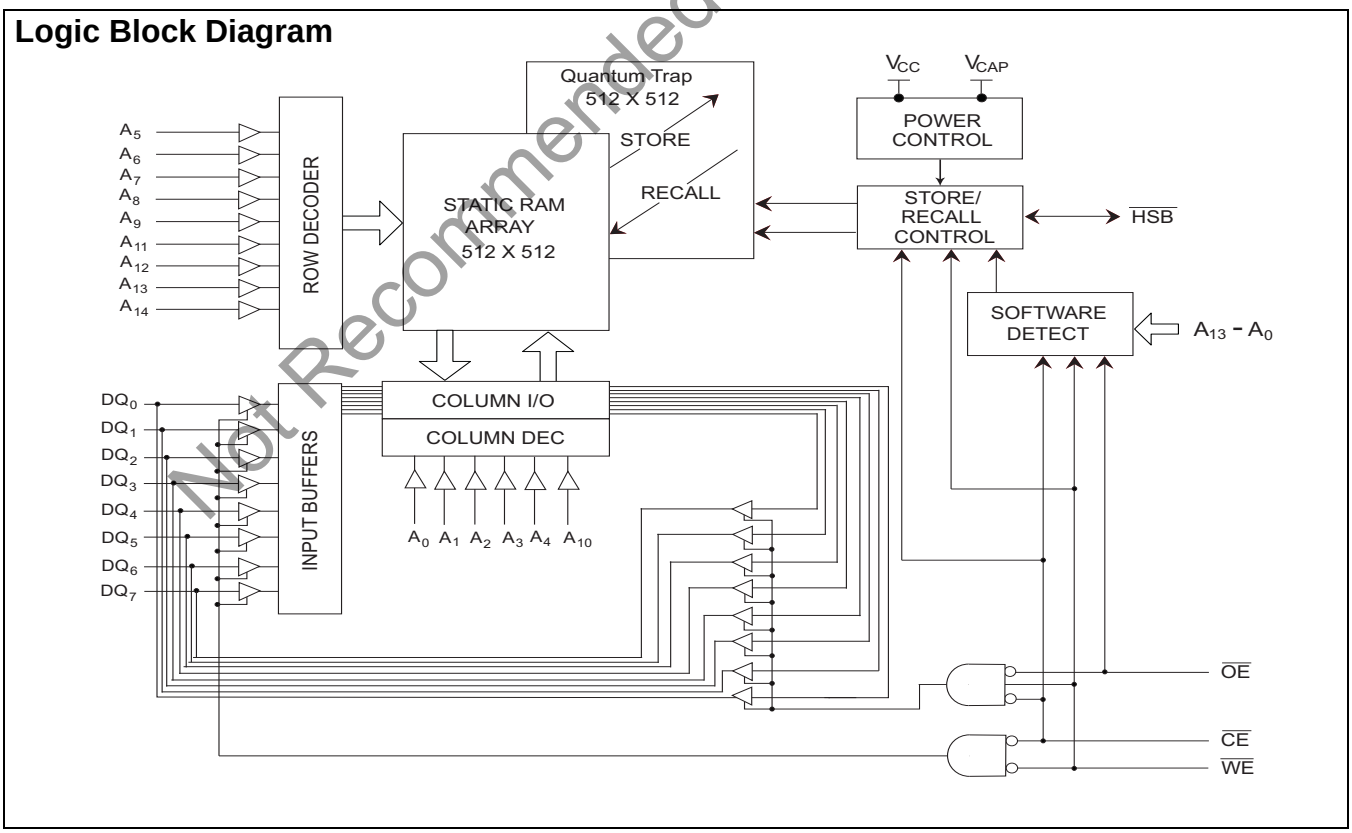
Features

- 25 ns, 35 ns, and 45 ns access times
- Pin compatible with STK14D88
- Hands off automatic STORE on power down with only a small capacitor
- STORE to QuantumTrap™ nonvolatile elements is initiated by software, hardware, or AutoStore™ on power down
- RECALL to SRAM initiated by software or power up
- Unlimited READ, WRITE, and RECALL cycles
- 200,000 STORE cycles to QuantumTrap
- 20 year data retention at 55°C
- Single 3V +20%**,** –10% operation
- Commercial and industrial temperature
- 32-pin (300 mil) SOIC and 48-pin (300 mil) SSOP packages
- RoHS compliance

Functional Description

The Cypress CY14B256L is a fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world's most reliable nonvolatile memory. The SRAM provides unlimited read and write cycles, while independent, nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power down. On power up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control. A hardware STORE is initiated with the $\overline{HSB}$ pin.

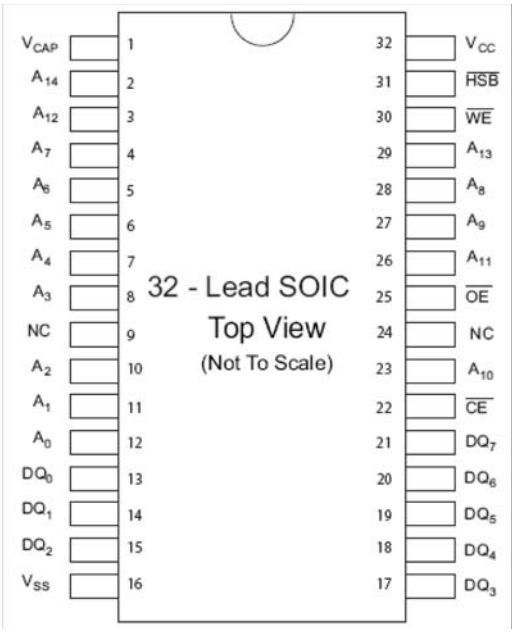
Logic Block Diagram

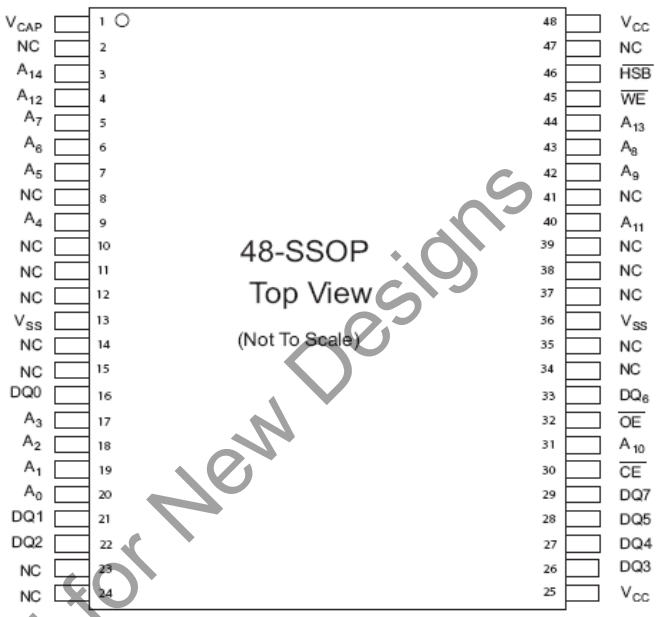


Contents

Pin Configurations

Figure 1. Pin Diagram - 32-Pin SOIC and 48-Pin SSOP





Pin Definitions

Pin Name	Alt	IO Type	Description
A_0–A_{14}		Input	**Address Inputs.** Used to select one of the 32,768 bytes of the nvSRAM.
DQ_0-DQ_7		Input or Output	**Bidirectional Data IO Lines**. Used as input or output lines depending on operation.
$\overline{WE}$	$\overline{W}$	Input	**Write Enable Input, Active LOW**. When the chip is enabled and $\overline{WE}$ is LOW, data on the IO pins is written to the specific address location.
$\overline{CE}$	$\overline{E}$	Input	**Chip Enable Input, Active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	$\overline{G}$	Input	**Output Enable, Active LOW**. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ HIGH causes the IO pins to tri-state.
V_{SS}		Ground	**Ground for the Device**. The device is connected to ground of the system.
V_{CC}		Power Supply	**Power Supply Inputs to the Device**.
$\overline{HSB}$		Input or Output	**Hardware Store Busy (HSB)**. When LOW, this output indicates a Hardware Store is in progress. When pulled low external to the chip, it initiates a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin high if not connected (connection optional).
V_{CAP}		Power Supply	**AutoStore Capacitor**. Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements.
NC		No Connect	**No Connect**. This pin is not connected to the die.

Device Operation

The CY14B256L nvSRAM is made up of two functional components paired in the same physical cell. These are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation) or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture enables the storage and recall of all cells in parallel. During the STORE and RECALL operations, SRAM READ and WRITE operations are inhibited. The CY14B256L supports unlimited reads and writes similar to a typical SRAM. In addition, it provides unlimited RECALL operations from the nonvolatile cells and up to 200K STORE operations.

SRAM Read

The CY14B256L performs a READ cycle whenever $\overline{CE}$ and $\overline{OE}$ are LOW while $\overline{WE}$ and $\overline{HSB}$ are HIGH. The address specified on pins A_{0-14} determines the 32,768 data bytes accessed. When the READ is initiated by an address transition, the outputs are valid after a delay of t_{AA} (READ cycle 1). If the READ is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at t_{ACE} or at t_{DOE}, whichever is later (READ cycle 2). The data outputs repeatedly respond to address changes within the t_{AA} access time without the need for transitions on any control input pins, and remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ or $\overline{HSB}$ is brought LOW.

SRAM Write

A WRITE cycle is performed whenever $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{HSB}$ is HIGH. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common I/O pins DQ_{0-7} are written into the memory if it has valid t_{SD}, before the end of a $\overline{WE}$ controlled WRITE or before the end of an $\overline{CE}$ controlled WRITE. Keep $\overline{OE}$ HIGH during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{OE}$ is left LOW, internal circuitry turns off the output buffers t_{HZWE} after $\overline{WE}$ goes LOW.

AutoStore Operation

The CY14B256L stores data to nvSRAM using one of three storage operations:

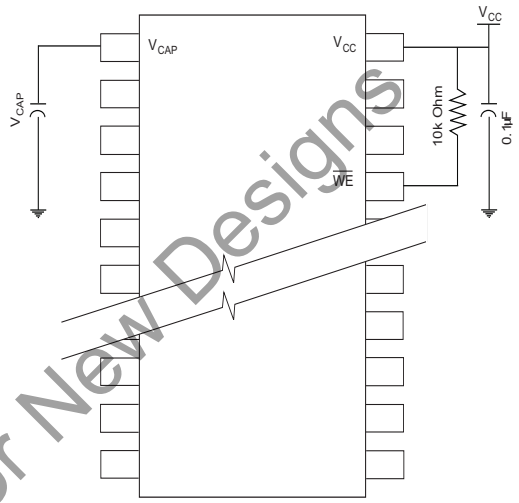
1. Hardware store activated by $\overline{HSB}$
2. Software store activated by an address sequence
3. AutoStore on device power down

AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14B256L.

During normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC}. A STORE operation is initiated with power provided by the V_{CAP} capacitor.

Figure 2 shows the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. Refer to the DC Electrical Characteristics on page 8 for the size of V_{CAP}. The voltage on the V_{CAP} pin is driven to 5V by a charge pump internal to the chip. A pull up is placed on $\overline{WE}$ to hold it inactive during power up.

Figure 2. AutoStore Mode



To reduce unnecessary nonvolatile stores, AutoStore and Hardware Store operations are ignored, unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place. An optional pull-up resistor is shown connected to $\overline{HSB}$. The $\overline{HSB}$ signal is monitored by the system to detect if an AutoStore cycle is in progress.

Hardware STORE ($\overline{HSB}$) Operation

The CY14B256L provides the $\overline{HSB}$ pin for controlling and acknowledging the STORE operations. The $\overline{HSB}$ pin is used to request a hardware STORE cycle. When the $\overline{HSB}$ pin is driven LOW, the CY14B256L conditionally initiates a STORE operation after t_{DELAY}. An actual STORE cycle only begins if a WRITE to the SRAM takes place since the last STORE or RECALL cycle. The $\overline{HSB}$ pin also acts as an open drain driver that is internally driven LOW to indicate a busy condition, while the STORE (initiated by any means) is in progress.

SRAM READ and WRITE operations, that are in progress when $\overline{HSB}$ is driven LOW by any means, are given time to complete before the STORE operation is initiated. After $\overline{HSB}$ goes LOW, the CY14B256L continues SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM READ operations take place. If a WRITE is in progress when $\overline{HSB}$ is pulled LOW, it allows a time, t_{DELAY} to complete. However, any SRAM WRITE cycles requested after $\overline{HSB}$ goes LOW are inhibited until $\overline{HSB}$ returns HIGH.

If $\overline{HSB}$ is not used, it is left unconnected.

Hardware RECALL (Power Up)

During power up or after any low power condition (V_{CC} < V_{SWITCH}), an internal RECALL request is latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete.

Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. The CY14B256L software STORE cycle is initiated by executing sequential CE controlled READ cycles from six specific address locations in exact order. During the STORE cycle, an erase of the previous nonvolatile data is first performed followed by a program of the nonvolatile elements. When a STORE cycle is initiated, input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence. If they intervene, the sequence is aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following READ sequence is performed:

1. Read address 0x0E38, Valid READ
2. Read address 0x31C7, Valid READ
3. Read address 0x03E0, Valid READ
4. Read address 0x3C1F, Valid READ
5. Read address 0x303F, Valid READ
6. Read address 0x0FC0, Initiate STORE cycle

The software sequence is clocked with CE controlled READs or OE controlled READs. When the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. It is important that READ cycles and not WRITE cycles are used in the sequence. It is not necessary that OE is LOW for a valid sequence. After the t_{STORE} cycle time is fulfilled, the SRAM is again activated for READ and WRITE operation.

Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of CE controlled READ operations is performed:

1. Read address 0x0E38, Valid READ
2. Read address 0x31C7, Valid READ
3. Read address 0x03E0, Valid READ
4. Read address 0x3C1F, Valid READ
5. Read address 0x303F, Valid READ
6. Read address 0x0C63, Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared, and then the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is once again ready for READ and WRITE operations. The RECALL operation does not alter the data in the nonvolatile elements. The nonvolatile data can be recalled an unlimited number of times.

Data Protection

The CY14B256L protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and WRITE operations. The low voltage condition is detected when V_{CC} is less than V_{SWITCH}. If the CY14B256L is in a WRITE mode (both CE and WE are low) at power up after a RECALL or after a STORE, the WRITE is inhibited until a negative transition on CE or WE is detected. This protects against inadvertent writes during power up or brown out conditions.

Noise Considerations

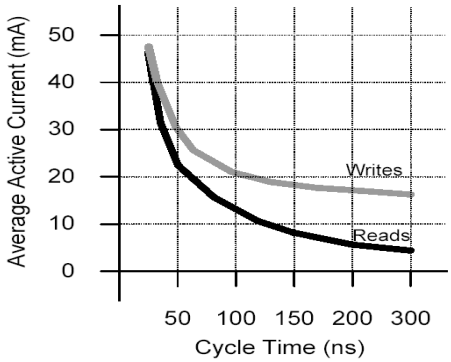
The CY14B256L is a high speed memory. It must have a high frequency bypass capacitor of approximately 0.1 µF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high speed CMOS ICs, careful routing of power, ground, and signals reduce circuit noise.

Low Average Active Power

CMOS technology provides the CY14B256L the benefit of drawing significantly less current when it is cycled at times longer than 50 ns. Figure 3 shows the relationship between I_{CC} and READ or WRITE cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, VCC = 3.6V, 100% duty cycle on chip enable). Only standby current is drawn when the chip is disabled. The overall average current drawn by the CY14B256L depends on the following items:

- The duty cycle of chip enable
- The overall cycle rate for accesses
- The ratio of READs to WRITEs
- CMOS versus TTL input levels
- The operating temperature
- The V_{CC} level
- I/O loading

Figure 3. Current vs. Cycle Time



Preventing Store

Disable the AutoStore function by initiating an AutoStore Disable sequence. A sequence of READ operations is performed in a manner similar to the software STORE initiation. To initiate the AutoStore Disable sequence, perform the following sequence of CE controlled or OE controlled READ operations:

1. Read Address 0x0E38 Valid READ
2. Read Address 0x31C7 Valid READ
3. Read Address 0x03E0 Valid READ
4. Read Address 0x3C1F Valid READ
5. Read Address 0x303F Valid READ
6. Read Address 0x03F8 AutoStore Disable

Re-enable the AutoStore by initiating an AutoStore Enable sequence. A sequence of READ operations is performed in a manner similar to the software RECALL initiation. To initiate the AutoStore Enable sequence, perform the following sequence of CE controlled or OE controlled READ operations:

1. Read Address 0x0E38 Valid READ
2. Read Address 0x31C7 Valid READ
3. Read Address 0x03E0 Valid READ
4. Read Address 0x3C1F Valid READ
5. Read Address 0x303F Valid READ
6. Read Address 0x07F0 AutoStore Enable

If the AutoStore function is disabled or re-enabled, a manual STORE operation (Hardware or Software) is issued to save the AutoStore state through subsequent power down cycles. The part comes from the factory with AutoStore enabled.

Best Practices

nvSRAM products have been used effectively for over 15 years. While ease of use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The nonvolatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, and so on should always program a unique NV pattern (for example, complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power up boot firmware routines should rewrite the nvSRAM into the desired state. While the nvSRAM is shipped in a preset state, the best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently (program bugs, incoming inspection routines, and so on).
- If autostore is firmware disabled, it does not reset to "autostore enabled" on every power down event captured by the nvSRAM. The application firmware should re-enable or re-disable autostore on each reset sequence based on the behavior desired.
- The V_{CAP} value specified in this data sheet includes a minimum and a maximum value size. Best practice is to meet this requirement and not exceed the maximum V_{CAP} value because higher inrush currents may reduce the reliability of the internal pass transistor. Customers that want to use a larger V_{CAP} value to make sure there is extra store charge should discuss their V_{CAP} size selection with Cypress to understand any impact on the V_{CAP} voltage level at the end of a t_{RECALL} period.

Table 1. Hardware Mode Selection

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$A_{14} - A_0$	Mode	I/O	Power
H	X	X	X	Not Selected	Output High Z	Standby
L	H	L	X	Read SRAM	Output Data	Active
L	L	X	X	Write SRAM	Input Data	Active
L	H	L	0x0E38 0x31C7 0x03E0 0x3C1F 0x303F 0x03F8	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Disable	Output Data Output Data Output Data Output Data Output Data Output Data	Active[1, 2, 3]
L	H	L	0x0E38 0x31C7 0x03E0 0x3C1F 0x303F 0x07F0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Enable	Output Data Output Data Output Data Output Data Output Data Output Data	Active[1, 2, 3]
L	H	L	0x0E38 0x31C7 0x03E0 0x3C1F 0x303F 0x0FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Store	Output Data Output Data Output Data Output Data Output Data Output High Z	Active I_{CC2}[1, 2, 3]
L	H	L	0x0E38 0x31C7 0x03E0 0x3C1F 0x303F 0x0C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Recall	Output Data Output Data Output Data Output Data Output Data Output High Z	Active[1, 2, 3]

Notes
1. The six consecutive address locations are in the order listed. $\overline{WE}$ is HIGH during all six cycles to enable a nonvolatile cycle.
2. While there are 15 address lines on the CY14B256L, only the lower 14 lines are used to control software modes.
3. I/O state depends on the state of $\overline{OE}$. The I/O table shown is based on $\overline{OE}$ Low.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{CC} Relative to GND .....–0.5V to 4.1V

Voltage Applied to Outputs in High Z State ..... –0.5V to V_{CC} + 0.5V

Input Voltage.....–0.5V to Vcc + 0.5V

Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... –2.0V to V_{CC} + 2.0V

Package Power Dissipation Capability (T_A = 25°C) 1.0W

Surface Mount Lead Soldering Temperature (3 Seconds) ..... +260°C

DC output Current (1 output at a time, 1s duration) .... 15 mA

Static Discharge Voltage..... > 2001V (MIL-STD-883, Method 3015)

Latch Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	2.7V to 3.6V
Industrial	-40°C to +85°C	2.7V to 3.6V

DC Electrical Characteristics

Over the operating range (V_{CC} = 2.7V to 3.6V) [4]

Parameter	Description	Test Conditions		Min	Max	Unit
I_{CC1}	Average V_{CC} Current	t_{RC} = 25 ns t_{RC} = 35 ns t_{RC} = 45 ns Dependent on output loading and cycle rate. Values obtained without output loads. I_{OUT} = 0 mA.	Commercial		65 55 50	mA mA
			Industrial		70 60 55	mA mA mA
I_{CC2}	Average V_{CC} Current during STORE	All Inputs Do Not Care, V_{CC} = Max Average current for duration t_{STORE}			3	mA
I_{CC3}	Average V_{CC} Current at t_{RC}= 200 ns, 5V, 25°C Typical	$\overline{WE} \geq (V_{CC} – 0.2V)$. All other inputs cycling. Dependent on output loading and cycle rate. Values obtained without output loads.			10	mA
I_{CC4}	Average V_{CAP} Current during AutoStore Cycle	All Inputs Do Not Care, V_{CC} = Max Average current for duration t_{STORE}			3	mA
I_{SB}	V_{CC} Standby Current	$\overline{CE} \geq (V_{CC} – 0.2V)$. All others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} – 0.2V)$. Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.			3	mA
I_{IX}	Input Leakage Current	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$		-1	+1	µA
I_{OZ}	Off State Output Leakage Current	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$, $\overline{CE}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$		-1	+1	µA
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			V_{SS} – 0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OUT} = –2 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OUT} = 4 mA			0.4	V
V_{CAP}	Storage Capacitor	Between V_{CAP} pin and Vss, 6V rated.		17	120	uF

Data Retention and Endurance

Parameter	Description	Min	Unit
$DATA_R$	Data Retention at 55°C	20	Years
NV_C	Nonvolatile STORE Operations	200	K

Note

4. The $\overline{HSB}$ pin has I_{OUT} = –10 µA for V_{OH} of 2.4 V. This parameter is characterized but not tested.

Capacitance

In the following table, the capacitance parameters are listed.[5]

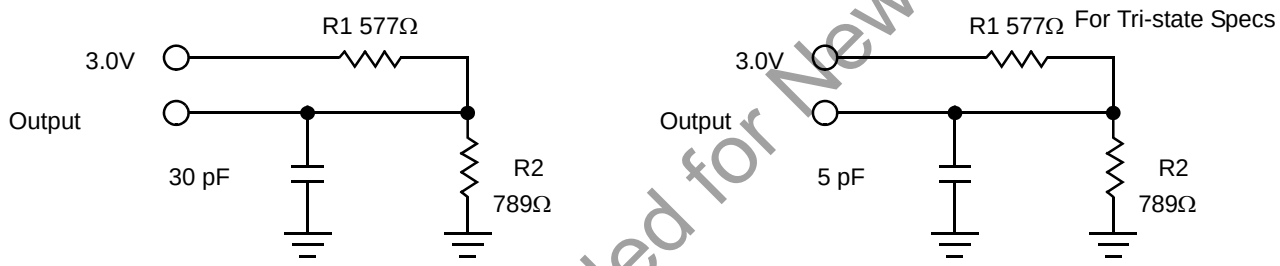
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 0 to 3.0V	7	pF
C_{OUT}	Output Capacitance		7	pF

Thermal Resistance

In the following table, the thermal resistance parameters are listed.[5]

Parameter	Description	Test Conditions	32-SOIC	48-SSOP	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	42.36	44.26	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		21.41	25.56	°C/W

Figure 4. AC Test Loads



AC Test Conditions

Input Pulse Levels ..... 0V to 3V
Input Rise and Fall Times (10% - 90%) ..... ≤5 ns
Input and Output Timing Reference Levels 1.5V

Note
5. These parameters are guaranteed by design and are not tested.

AC Switching Characteristics

SRAM Read Cycle

Parameter		Description	25 ns		35 ns		45 ns		Unit
Cypress Parameter	Alt		Min	Max	Min	Max	Min	Max	
t_{ACE}	t_{ELQV}	Chip Enable Access Time		25		35		45	ns
t_{RC} [6]	t_{AVAV}, t_{ELEH}	Read Cycle Time	25		35		45		ns
t_{AA} [7]	t_{AVQV}	Address Access Time		25		35		45	ns
t_{DOE}	t_{GLQV}	Output Enable to Data Valid		12		15		20	ns
t_{OHA} [7]	t_{AXQX}	Output Hold After Address Change	3		3		3		ns
t_{LZCE} [8]	t_{ELQX}	Chip Enable to Output Active	3		3		3		ns
t_{HZCE} [8]	t_{EHQZ}	Chip Disable to Output Inactive		10		13		15	ns
t_{LZOE} [8]	t_{GLQX}	Output Enable to Output Active	0		0		0		ns
t_{HZOE} [8]	t_{GHQZ}	Output Disable to Output Inactive		10		13		15	ns
t_{PU} [5]	t_{ELICCH}	Chip Enable to Power Active	0		0		0		ns
t_{PD} [5]	t_{EHICCL}	Chip Disable to Power Standby		25		35		45	ns

Switching Waveforms

Figure 5. SRAM Read Cycle 1: Address Controlled [6, 7, 9]

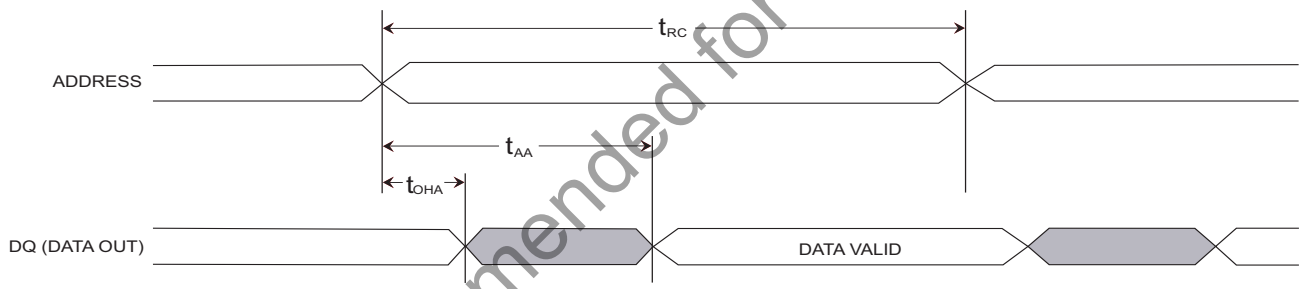
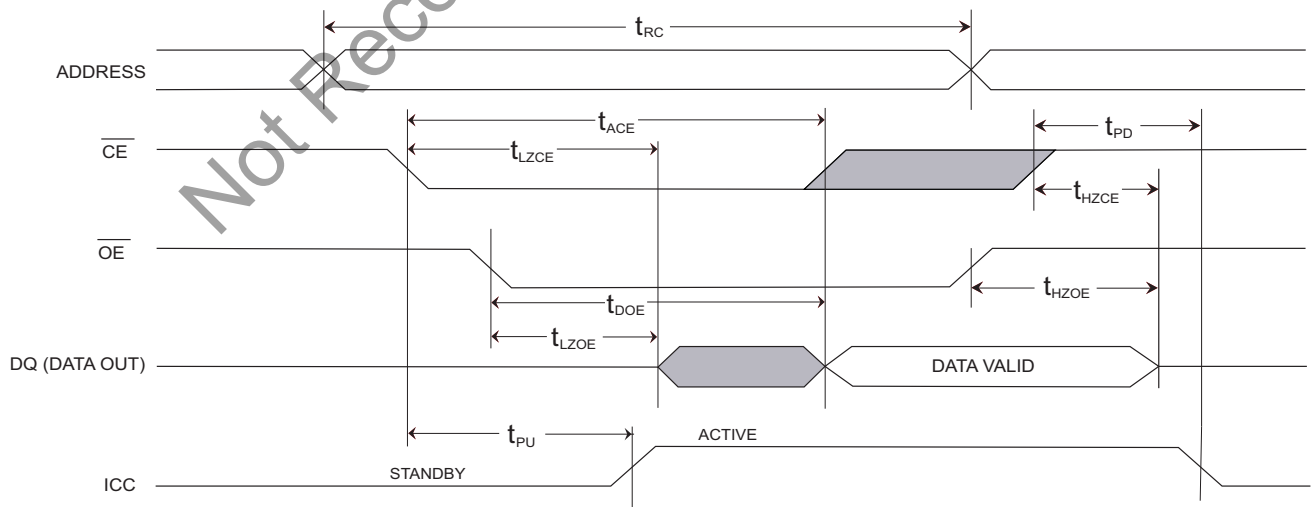


Figure 6. SRAM Read Cycle 2: $\overline{CE}$ Controlled [6, 9]



Notes
6. $\overline{WE}$ must be HIGH during SRAM Read cycles.
7. Device is continuously selected with $\overline{CE}$ and $\overline{OE}$ both Low.
8. Measured ±200 mV from steady state output voltage.
9. $\overline{HSB}$ must remain HIGH during SRAM Read and Write Cycles.

SRAM Write Cycle

Parameter		Description	25 ns		35 ns		45 ns		Unit
Cypress Parameter	Alt		Min	Max	Min	Max	Min	Max	
t_{WC}	t_{AVAV}	Write Cycle Time	25		35		45		ns
t_{PWE}	t_{WLWH}, t_{WLEH}	Write Pulse Width	20		25		30		ns
t_{SCE}	t_{ELWH}, t_{ELEH}	Chip Enable To End of Write	20		25		30		ns
t_{SD}	t_{DVWH}, t_{DVEH}	Data Setup to End of Write	10		12		15		ns
t_{HD}	t_{WHDX}, t_{EHDX}	Data Hold After End of Write	0		0		0		ns
t_{AW}	t_{AVWH}, t_{AVEH}	Address Setup to End of Write	20		25		30		ns
t_{SA}	t_{AVWL}, t_{AVEL}	Address Setup to Start of Write	0		0		0		ns
t_{HA}	t_{WHAX}, t_{EHAX}	Address Hold After End of Write	0		0		0		ns
t_{HZWE} [8,10]	t_{WLQZ}	Write Enable to Output Disable		10		13		15	ns
t_{LZWE} [8]	t_{WHQX}	Output Active After End of Write	3		3		3		ns

Switching Waveforms

Figure 7. SRAM Write Cycle 1: $\overline{WE}$ Controlled [10, 11]

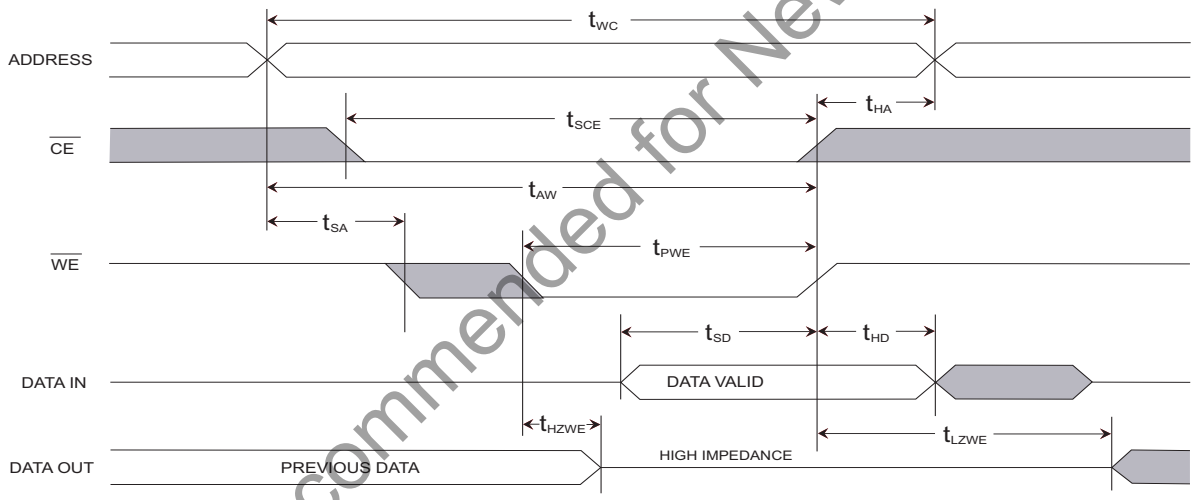
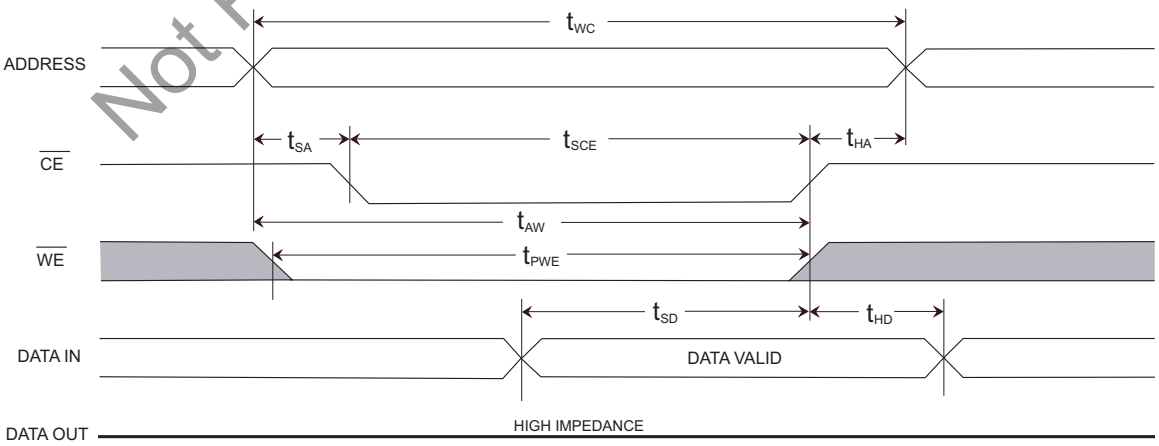


Figure 8. SRAM Write Cycle 2: $\overline{CE}$ Controlled [10, 11]



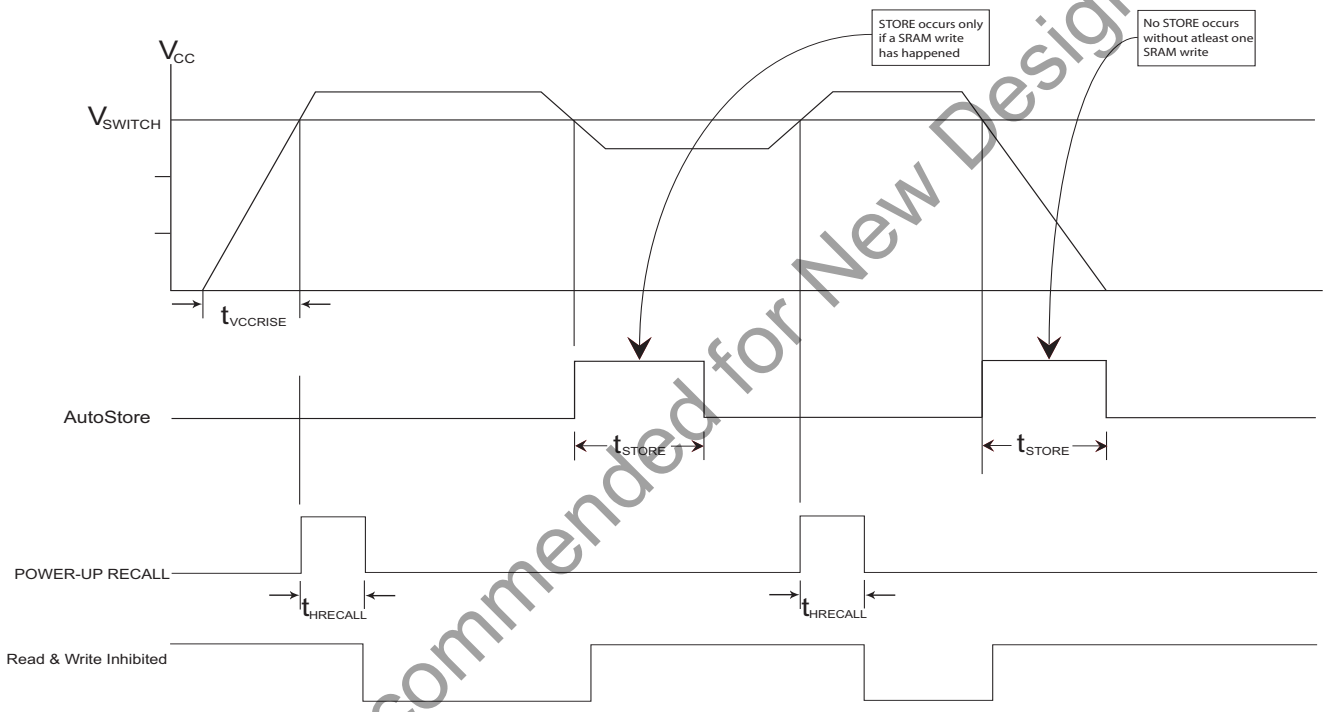
Notes
10. If $\overline{WE}$ is Low when $\overline{CE}$ goes Low, the outputs remain in the high impedance state.
11. $\overline{CE}$ or $\overline{WE}$ must be greater than V_{IH} during address transitions.

AutoStore or Power Up RECALL

Parameter	Alt	Description	CY14B256L		Unit
			Min	Max	
$t_{HRECALL}$ [12]	$t_{RESTORE}$	Power up RECALL Duration		20	ms
t_{STORE} [13, 14]	t_{HLHZ}	STORE Cycle Duration		12.5	ms
V_{SWITCH}		Low Voltage Trigger Level		2.65	V
$t_{VCCRISE}$		V_{CC} Rise Time	150		µs

Switching Waveforms

Figure 9. AutoStore/Power Up RECALL



Note Read and Write cycles are ignored during STORE, RECALL, and while Vcc is below V_{SWITCH}

Notes
12. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.
13. If an SRAM WRITE has not taken place since the last nonvolatile cycle, no STORE will take place.
14. Industrial grade devices requires 15 ms max.

Software Controlled STORE/RECALL Cycle

The software controlled STORE/RECALL cycle follows. [15, 16]

Parameter	Alt	Description	25 ns		35 ns		45 ns		Unit
			Min	Max	Min	Max	Min	Max	
t_{RC}[16]	t_{AVAV}	STORE/RECALL Initiation Cycle Time	25		35		45		ns
t_{SA}	t_{AVEL}	Address Setup Time	0		0		0		ns
t_{CW}	t_{ELEH}	Clock Pulse Width	20		25		30		ns
t_{HA}	t_{GHAX}, t_{ELAX}	Address Hold Time	1		1		1		ns
t_{RECALL}		RECALL Duration		120		120		120	µs

Switching Waveforms

Figure 10. $\overline{CE}$ Controlled Software STORE/RECALL Cycle [16]

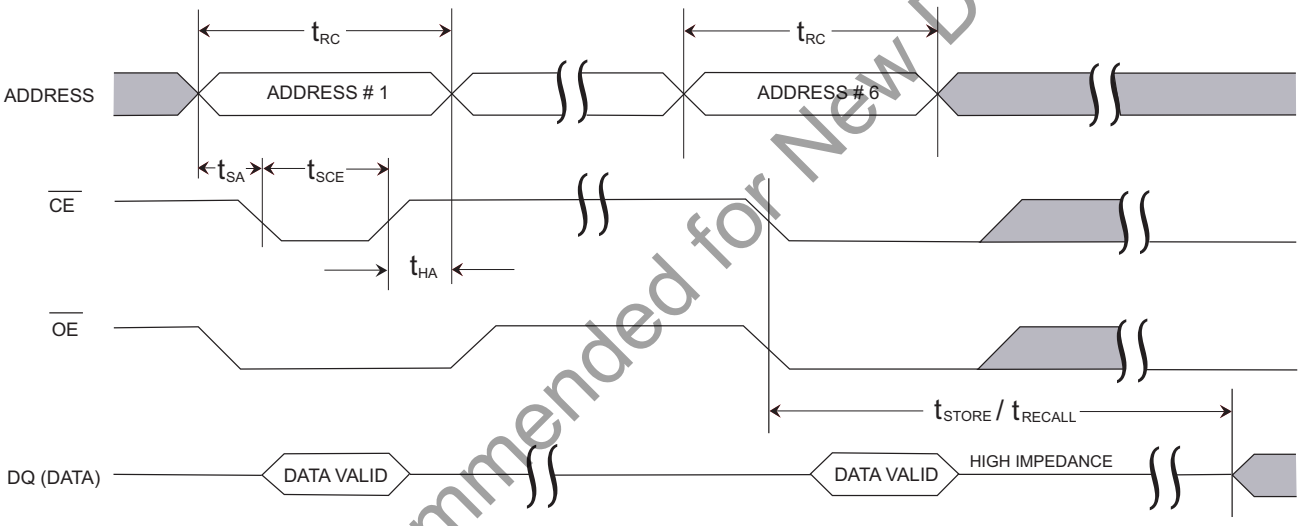
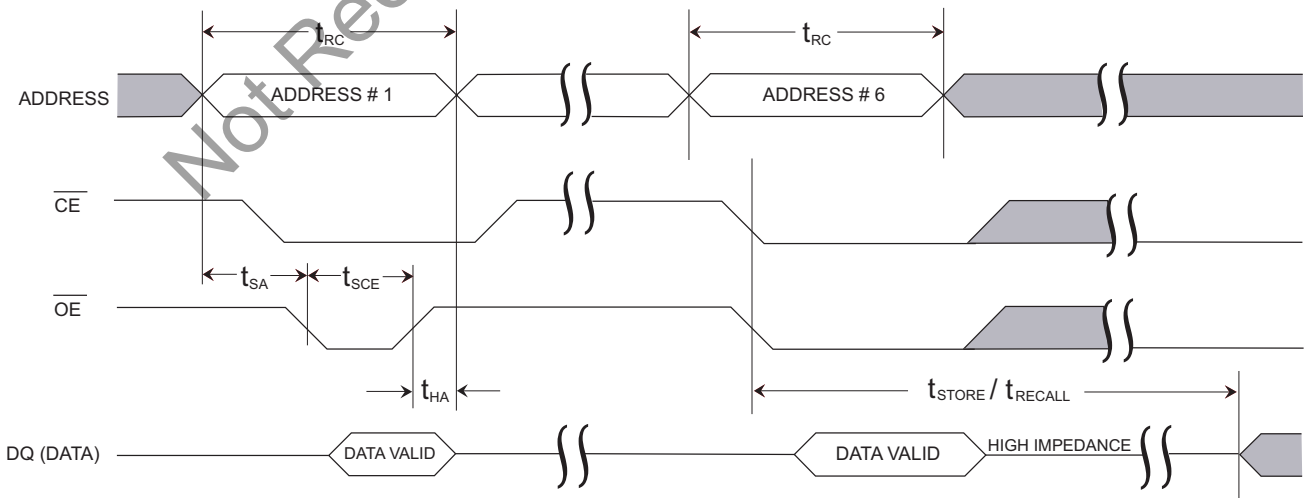


Figure 11. $\overline{OE}$ Controlled Software STORE/RECALL Cycle [16]



Notes

15. The software sequence is clocked on the falling edge of $\overline{CE}$ controlled READs or $\overline{OE}$ controlled READs.
16. The six consecutive addresses must be read in the order listed in the Mode Selection table. $\overline{WE}$ must be HIGH during all six consecutive cycles.

Hardware STORE Cycle

Parameter	Alt	Description	CY14B256L		Unit
			Min	Max	
t_{PHSB}	t_{HLHX}	Hardware STORE Pulse Width	15		ns
t_{DELAY} [17]	t_{HLQZ} , t_{BLQZ}	Time Allowed to Complete SRAM Cycle	1	70	µs
t_{SS} [18, 19]		Soft Sequence Processing Time		70	us

Switching Waveforms

Figure 12. Hardware STORE Cycle

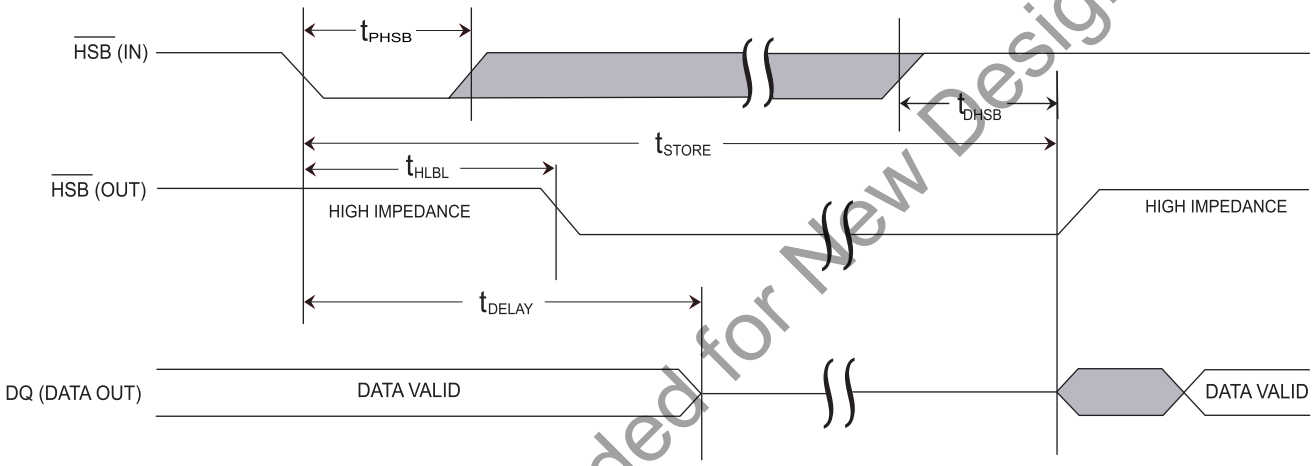
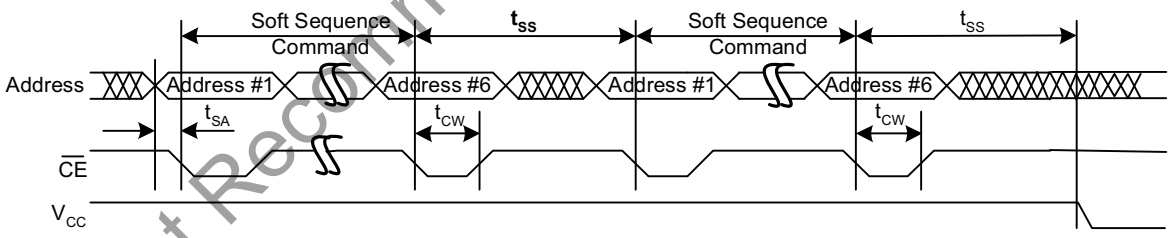


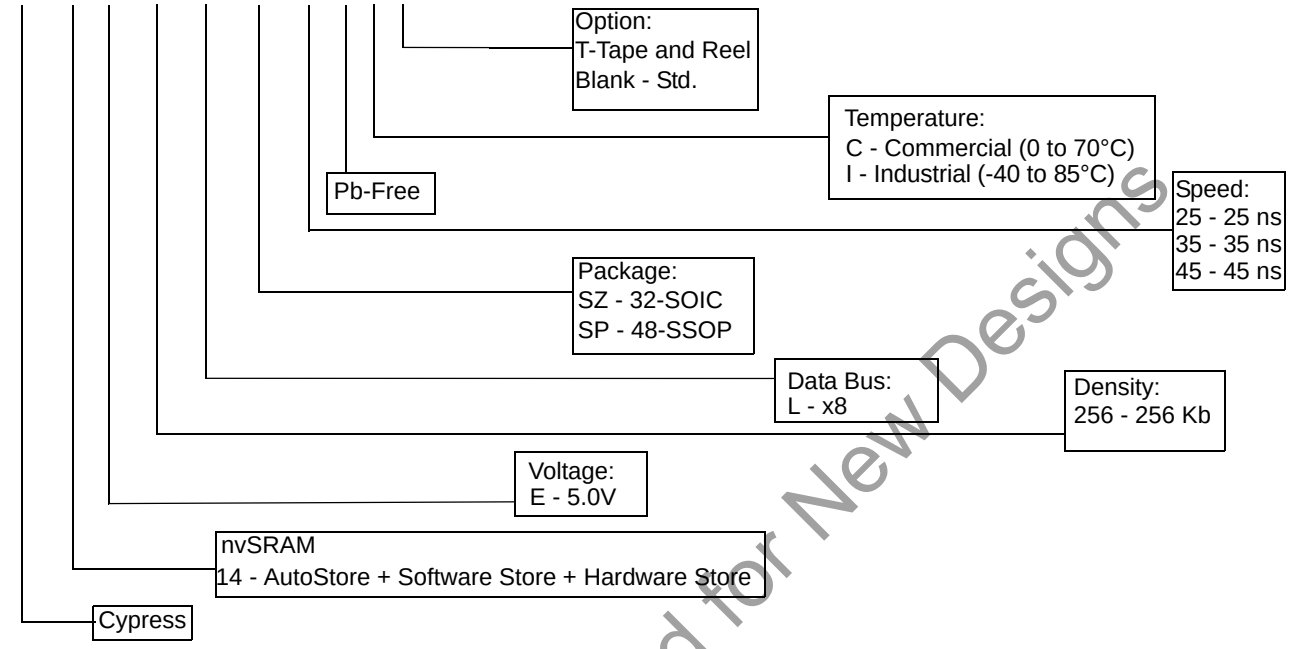
Figure 13. Soft Sequence Processing [18, 19]



Notes
17. Read and Write cycles in progress before $\overline{HSB}$ are given this amount of time to complete.
18. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain HIGH to effectively register command.
19. Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See specific command.

Part Numbering Nomenclature

CY 14 B 256 L- SZ 25 X C T



Ordering Information

These parts are not recommended for new designs.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY14B256L-SZ25XCT	51-85127	32-pin SOIC	Commercial
	CY14B256L-SZ25XC	51-85127	32-pin SOIC	
	CY14B256L-SP25XCT	51-85061	48-pin SSOP	
	CY14B256L-SP25XC	51-85061	48-pin SSOP	
	CY14B256L-SZ25XIT	51-85127	32-pin SOIC	Industrial
	CY14B256L-SZ25XI	51-85127	32-pin SOIC	
	CY14B256L-SP25XIT	51-85061	48-pin SSOP	
	CY14B256L-SP25XI	51-85061	48-pin SSOP	
35	CY14B256L-SZ35XCT	51-85127	32-pin SOIC	Commercial
	CY14B256L-SZ35XC	51-85127	32-pin SOIC	
	CY14B256L-SP35XCT	51-85061	48-pin SSOP	
	CY14B256L-SP35XC	51-85061	48-pin SSOP	
	CY14B256L-SZ35XIT	51-85127	32-pin SOIC	Industrial
	CY14B256L-SZ35XI	51-85127	32-pin SOIC	
	CY14B256L-SP35XIT	51-85061	48-pin SSOP	
	CY14B256L-SP35XI	51-85061	48-pin SSOP	

Ordering Information

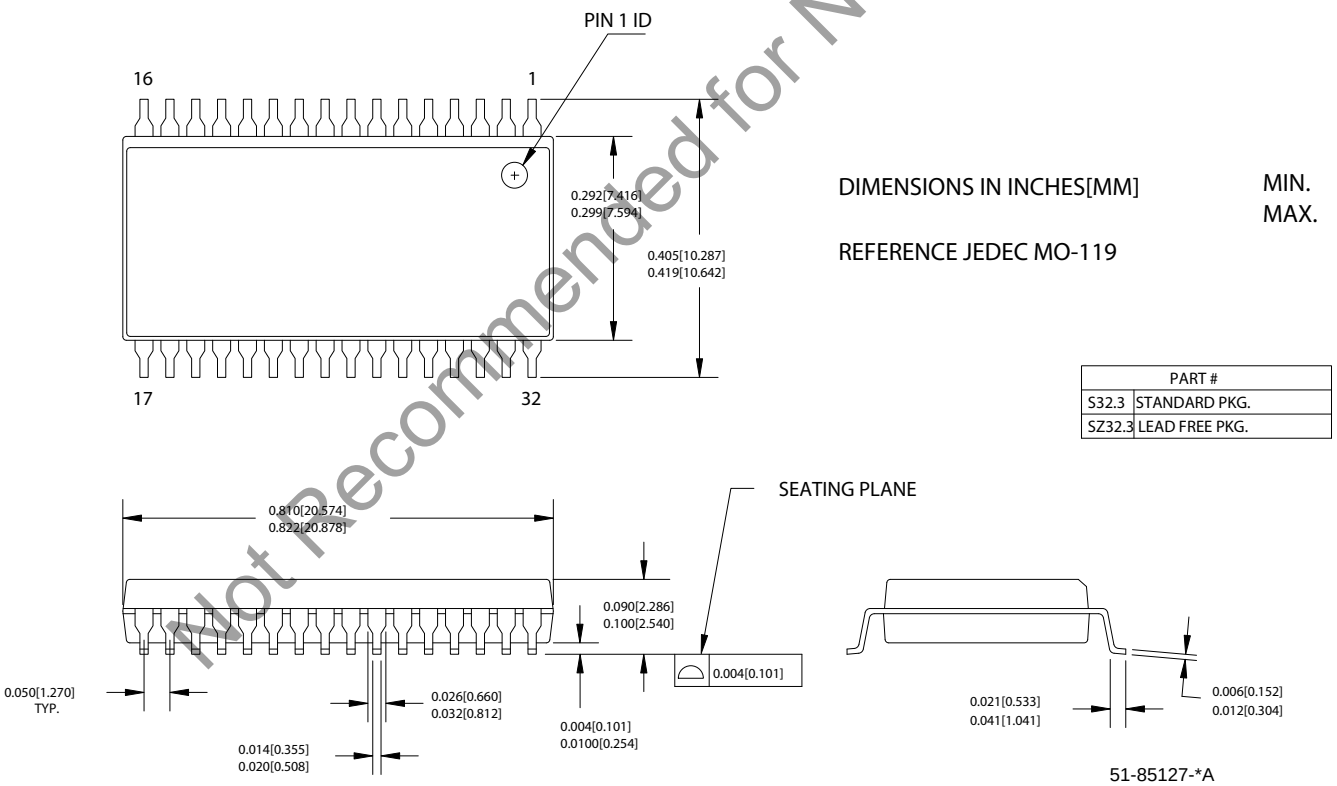
These parts are not recommended for new designs.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY14B256L-SZ45XCT	51-85127	32-pin SOIC	Commercial
	CY14B256L-SZ45XC	51-85127	32-pin SOIC	
	CY14B256L-SP45XCT	51-85061	48-pin SSOP	
	CY14B256L-SP45XC	51-85061	48-pin SSOP	
	CY14B256L-SZ45XIT	51-85127	32-pin SOIC	Industrial
	CY14B256L-SZ45XI	51-85127	32-pin SOIC	
	CY14B256L-SP45XIT	51-85061	48-pin SSOP	
	CY14B256L-SP45XI	51-85061	48-pin SSOP	

All parts are Pb-free. This table contains Final information. Contact your local Cypress sales representative for availability of these parts

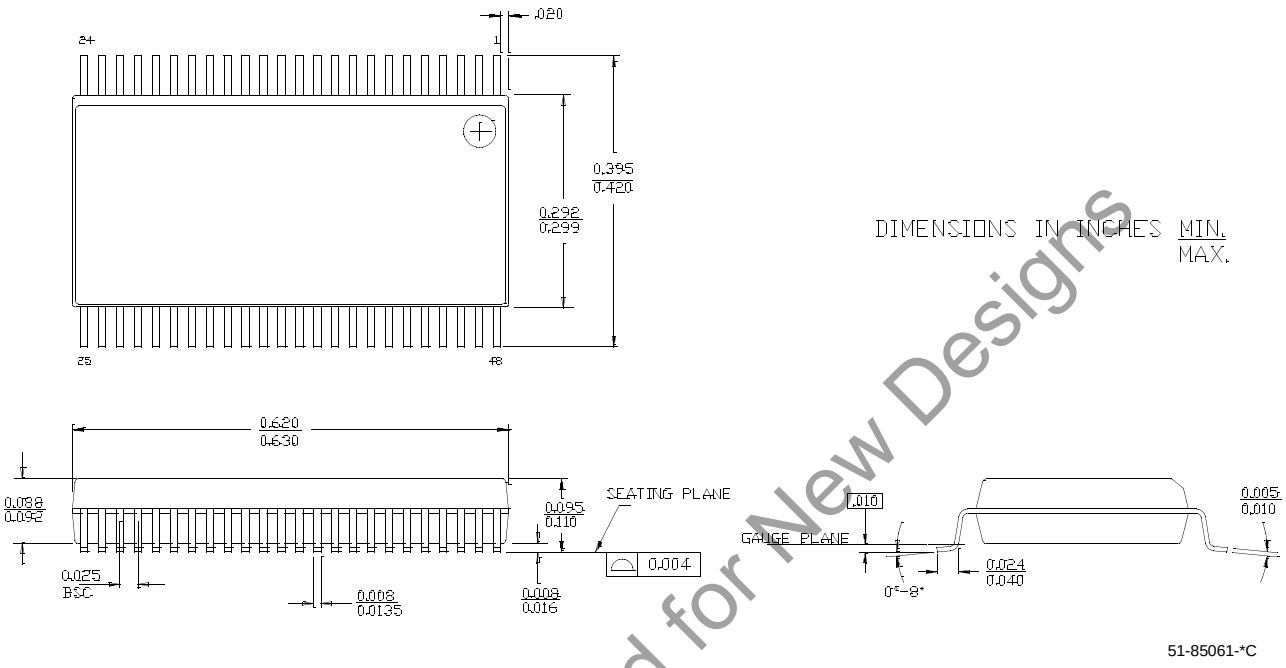
Package Diagrams

Figure 14. 32-Pin (300 Mil) SOIC (51-85127)



Package Diagrams (continued)

Figure 15. 48-Pin (300 mil) Shrunk Small Outline Package (51-85061)



Document History Page

Document Title: CY14B256L 256 Kbit (32K x 8) nvSRAM Document Number: 001-06422				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	425138	See ECN	TUP	New data sheet
*A	437321	See ECN	TUP	Show data sheet on External Web
*B	471966	See ECN	TUP	Changed $V_{IH(min)}$ from 2.2V to 2.0V Changed t_{RECALL} from 60 µs to 50 µs Changed Endurance from one million cycles to 500K cycles Changed Data Retention from 100 years to 20 years Added Soft Sequence Processing Time Waveform Updated Part Numbering Nomenclature and Ordering Information
*C	503277	See ECN	PCI	Changed from “Advance” to “Preliminary” Changed the term “Unlimited” to “Infinite” Changed endurance from 500K cycles to 200K cycles Device operation: Tolerance limit changed from + 20% to + 15% in the Features Section and Operating Range Table Removed Icc_1 values from the DC table for 25 ns and 35 ns industrial grade Changed $V_{SWITCH(min)}$ from 2.55V to 2.45V Added temperature specification to data retention - 20 years at 55°C Changed the max value of Vcap storage capacitor from 120 µF to 57 µF Updated Part Nomenclature Table and Ordering Information Table
*D	597004	See ECN	TUP	Removed $V_{SWITCH(min)}$ specification from the AutoStore/Power Up RECALL table Changed t_{GLAX} specification from 20 ns to 1 ns Added $t_{DELAY(max)}$ specification of 70 µs in the Hardware STORE Cycle table Removed t_{HLBL} specification Changed t_{SS} specification from 70 µs (min) to 70 µs (max) Changed $V_{CAP(max)}$ from 57 µF to 120 µF
*E	696097	See ECN	VKN	Added footnote 6 related to $\overline{HSB}$. Changed t_{GLAX} to t_{GHAX}
*F	1349963	See ECN	SFV	Changed from Preliminary to Final. Updated Ordering Information Table
*G	2483006	See ECN	GVCH/PYRS	Changed tolerance from +15%, -10% to +20%, -10% Changed Operating voltage range from 2.7V-3.45V to 2.7V-3.6V.
*H	2625139	01/30/09	GVCH/PYRS	Updated “features” Updated $\overline{WE}$ pin description Added data retention at 55°C Added best practices Added I_{CC1} spec for 25ns and 35ns access speed for industrial temperate Updated V_{IH} from Vcc+0.3 to Vcc+0.5 Removed footnote 4 and 5 Added Data retention and Endurance Table Added Thermal resistance values Changed parameter t_{AS} to t_{SA} Changed t_{RECALL} from 50us to 120us (Including t_{ss} of 70us) Renamed t_{GLAX} to t_{HA} Updated Figure 11 and 12 Renamed t_{HLHX} to t_{PHSB} Updated Figure 12 and 13
*I	2815609	11/26/09	GVCH	Added note in the Ordering Information table and watermark to state that the parts in this data sheet are not recommended for new designs. Added the Contents page.

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