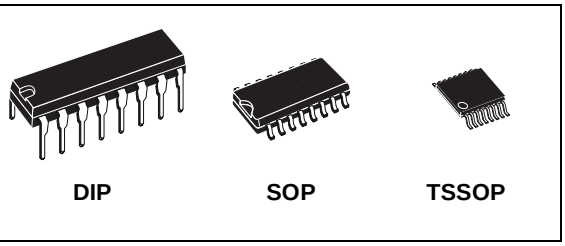
M74HC40103

8 STAGE PRESETTABLE SYNCHRONOUS DOWN COUNTER

- HIGH SPEED :
  f_{MAX} = 38MHz (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  I_{CC} =4µA(MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY:
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 4mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 40103



ORDER CODES

PACKAGE	TUBE	T & R
DIP	M74HC40103B1R	
SOP	M74HC40103M1R	M74HC40103RM13TR
TSSOP		M74HC40103TTR

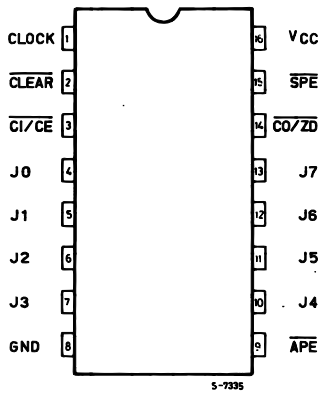
DESCRIPTION

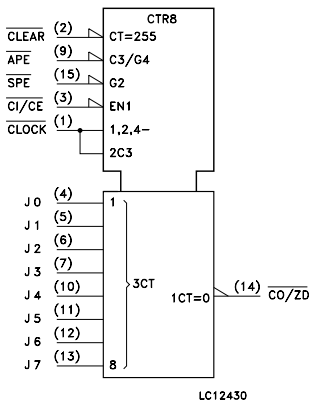
The M74HC40103 is an high speed CMOS 8-STAGE PRESETTABLE SYNCHRONOUS DOWN COUNTER fabricated with silicon gate C^2MOS technology.

The HC40103 consists of an 8 stage synchronous down counter with a single output which is active when the internal count is zero. The HC40103 contains a single 8-bit binary counter. This device has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the CARRY-OUT / ZERO DETECT output are active low logic. In normal operation the counter is decremented by one count on each positive transition of the CLOCK. Counting is inhibited when the CARRY-IN / COUNTER ENABLE ($\overline{CI/CE}$) input is high. The CARRY-OUT / ZERO-DETECT ($\overline{CO/ZD}$) output goes low when the count reaches zero if the $\overline{CI/CE}$ input is low, and remains low for one full clock period. When the SYNCHRONOUS PRESET-ENABLE ($\overline{SPE}$) input is low, data at the J input is clocked into the counter on the next positive clock transition regardless of the state of the $\overline{CI/CE}$ input.

When the ASYNCHRONOUS PRESET-ENABLE ($\overline{APE}$) input is low, data at the J inputs is asynchronously forced into the counter regardless of the state of the $\overline{SPE}$ $\overline{CI/CE}$ or CLOCK inputs. J input J0-J7 represent a singular 8-bit binary word. When the CLEAR, $\overline{CLR}$ input is low, the counter is asynchronously cleared to its maximum count

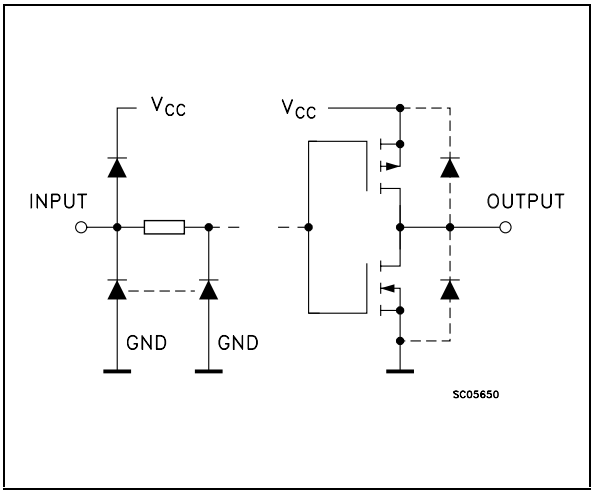
PIN CONNECTION AND IEC LOGIC SYMBOLS





(255_{10}) regardless of the state of any other input. The precedence relationship between control input is indicated in the truth table. If all control inputs are high at the time of zero count, the counters will jump to the maximum count giving a counting sequence of 256 clock pulses long. The HC40103 may be cascaded using the $\overline{CI/CE}$ input and the $\overline{CO/ZD}$ output, in either a synchronous or ripple mode. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

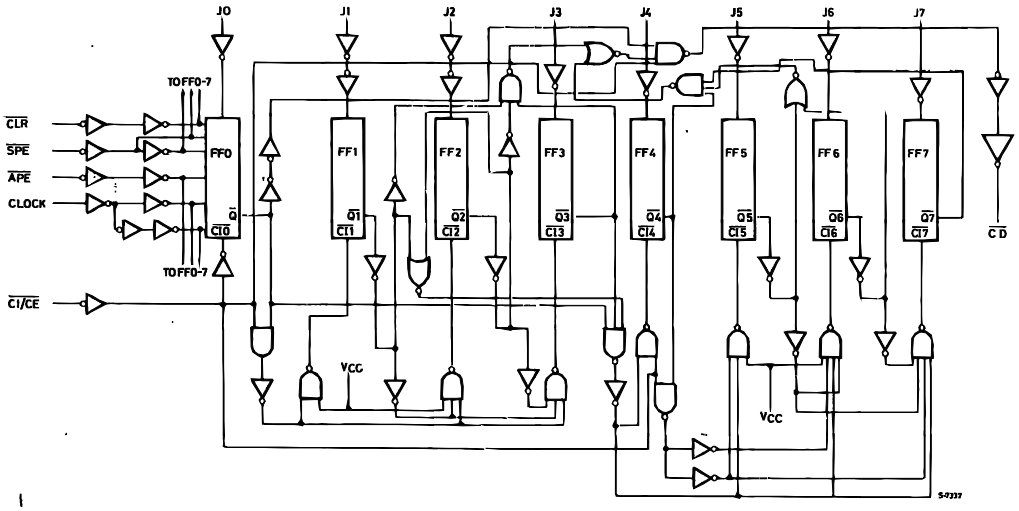
PIN No	SYMBOL	NAME AND FUNCTION
1	CLOCK	Clock Input (LOW to HIGH edge triggered)
2	$\overline{CLEAR}$	Asynchronous Master Reset Input (Active Low)
3	$\overline{CI/CE}$	Terminal Enable Input
4, 5, 6, 7, 10, 11, 12, 13	J0 to J9	Jam Inputs
9	$\overline{APE}$	Asynchronous Preset Enable Inputs(Active Low)
14	$\overline{CO/ZD}$	Terminal Count Output (Active Low)
15	$\overline{SPE}$	Synchronous Preset Enable Input (Active Low)
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

TRUTH TABLE

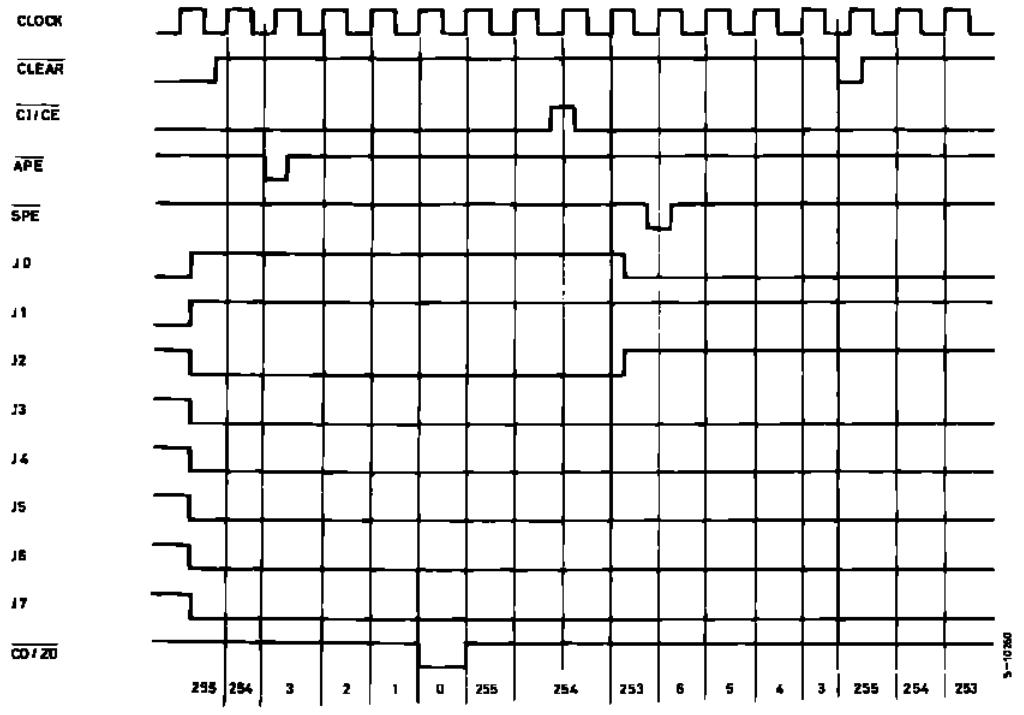
CONTROL INPUTS				MODE	FUNCTIONAL DESCRIPTION
$\overline{CLEAR}$	$\overline{APE}$	$\overline{SPE}$	$\overline{CI/CE}$		
H	H	H	H	COUNT INHIBIT	EVEN IF CLOCK IS GIVEN, NO COUNT IS MADE
H	H	H	L	REGULAR COUNT	DOWN COUNT AT RISING EDGE OF CLOCK
H	H	L	X	SYNCHRONOUS PRESET	DATA OF PI TERMINAL IS PRESET AT RISING EDGE OF CLOCK
H	L	X	X	ASYNCHRONOUS PRESET	DATA OF PI TERMINAL IS ASYNCHRONOUSLY PRESET TO CLOCK
L	X	X	X	CLEAR	COUNTER IS SET TO MAXIMUM COUNT

X : Don't Care
Maximum Count is "255"

LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	I_O=20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O=4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O=5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND			4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6ns)

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CK}$ - $\overline{CO/ZD}$)	2.0			96	185		230		280	ns
		4.5			24	37		46		56	
		6.0			20	31		39		47	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{APE}$ - $\overline{CO/ZD}$)	2.0			116	225		280		340	ns
		4.5			29	45		56		68	
		6.0			25	38		48		57	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CL}$ - $\overline{CO/ZD}$)	2.0			104	200		250		300	ns
		4.5			26	40		50		60	
		6.0			22	34		43		51	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CI/CE}$ - $\overline{CO/ZD}$)	2.0			48	95		120		145	ns
		4.5			12	19		24		29	
		6.0			10	16		20		24	

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	2.0		4	8		3		2.6		MHz
		4.5		20	32		16		13		
		6.0		24	38		19		15		
t_W	Clock Pulse Width HIGH or LOW	2.0		150	20		195		235		ns
		4.5		30	7		36		45		
		6.0		25	5		32		40		
t_W	CLEAR Pulse Width LOW	2.0		115	35		140		175		ns
		4.5		20	12		28		35		
		6.0		19	10		24		30		
t_W	Preset Enable Pulse Width APE, LOW	2.0		115	31		140		175		ns
		4.5		20	11		28		35		
		6.0		19	9		24		30		
t_{REM}	Removal time CLEAR to CLOCK or APE to CLOCK	2.0		47	12		62		70		ns
		4.5		9	4		12		13		
		6.0		8	3		10		11		
t_{SETUP}	Set Up Time SPE to CLOCK	2.0		70	20		90		110		ns
		4.5		13	7		16		20		
		6.0		11	5		15		16		
t_{SETUP}	Set Up Time CI/CE to CLOCK	2.0		140	40		175		205		ns
		4.5		27	14		36		42		
		6.0		23	12		31		36		
t_{SETUP}	Set Up Time Jn to CLOCK	2.0		72	20		92		105		ns
		4.5		14	8		18		20		
		6.0		12	6		15		18		
t_{hold}	Hold Time SPE to CLOCK	2.0		-14	0		0		0		ns
		4.5		-5	0		0		0		
		6.0		-4	0		0		0		
t_{hold}	Hold Time CI/CE to CLOCK	2.0		-30	0		0		0		ns
		4.5		-11	0		0		0		
		6.0		-9	0		0		0		
t_{hold}	Hold Time Jn to CLOCK	2.0		-17	0		0		0		ns
		4.5		-6	0		0		0		
		6.0		-5	0		0		0		

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	5.0			5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0			60						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

FUNCTIONAL DESCRIPTION

This device is an 8-stage presettable synchronous down counter. Carry Out/Zero Detect ($\overline{CO/ZD}$) is output at the "L" level for the period of 1 bit when the readout becomes "0". This device adopts 8-bit-binary counter decimal notation, making setting up to 255 counts possible.

COUNT OPERATION

At the "H" level of control input of $\overline{CLEAR}$, $\overline{SPE}$ and $\overline{APE}$, the counter carriers out down count operation one by one at the rise of pulse given to CLOCK input. Count operation can be inhibited by setting Carry Input/Clock Enable $\overline{CI/CE}$ to the "H" level.

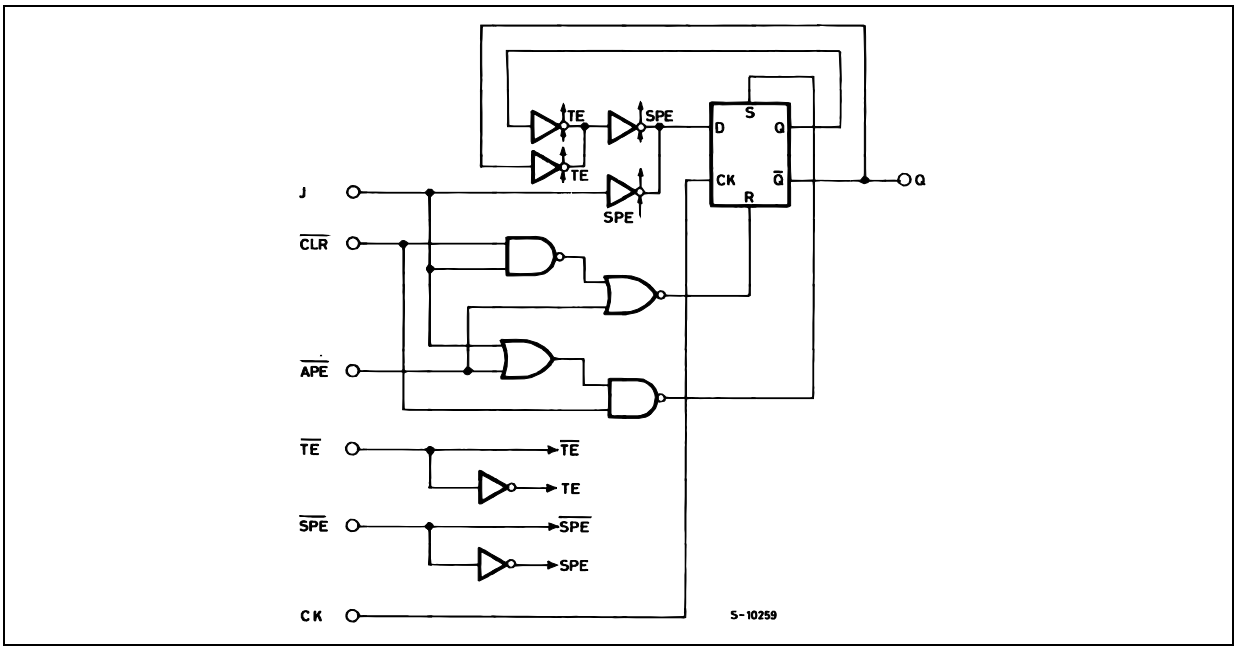
$\overline{CO/ZD}$ is output at the "L" level when the readout becomes "0" but is not output even if the readout becomes "0" when $\overline{CI/CE}$ is at the "H" level, thus maintaining the "H" level.

Synchronous cascade operation can be carried out by using $\overline{CI/CE}$ input and $\overline{CO/ZD}$ output.

The contents of count jump to maximum count (255) if clock is given when the readout is "0". Therefore, operation of 256-frequency division is carried out when clock input alone is given without various kinds of preset operation.

PRESET AND RESET OPERATION

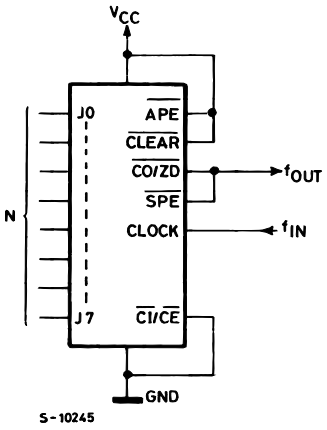
When Clear ($\overline{CLEAR}$) input is set to the "L" level, the readout is set to the maximum count independently of other inputs. When Asynchronous Preset Enable ($\overline{APE}$) input is set to the "L" level, readouts given on J0 to J7 can be preset asynchronously to the counter independently of inputs other than $\overline{CLEAR}$ input. When Synchronous Preset Enable ($\overline{SPE}$) is set to the "L" level the readouts given on J0 to J7 can be preset to counter synchronously with the rise of clock. As to these operation mode, refer to the truth table.



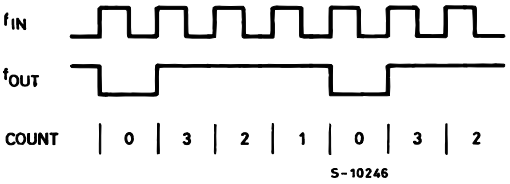
INPUTS						OUTPUT
$\overline{CLEAR}$	$\overline{APE}$	$\overline{SPE}$	J	$\overline{TE}$	CLOCK	$\overline{Qn+1}$
L	X	X	X	X	X	L
H	L	X	L	X	X	L
H	L	X	H	X	X	H
H	H	L	L	X	⌐¯	L
H	H	L	H	X	⌐¯	H
H	H	L	X	X	¯⌐	$\overline{Q}n$
H	H	H	X	L	¯⌐	Qn
H	H	H	X	H	X	$\overline{Q}n$

TYPICAL APPLICATIONS

PROGRAMMABLE DIVIDE-BY-N COUNTER

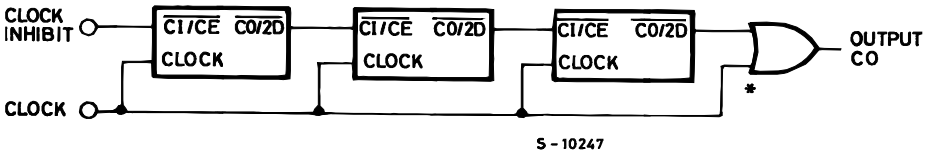


$f_{OUT} = f_{IN} / (N+1)$
Timing Chart when N = "3"
($J0, J1 = V_{CC}$, J2-J7 = GND



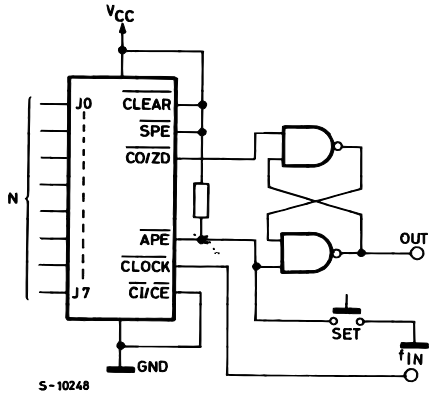
HC40103 ... 1/2 to 1/256 are dividable

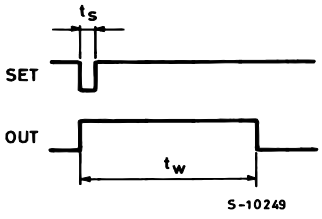
PARALLEL CARRY CASCADING



* At synchronous cascade connection, huzzerd occurs at C0 output after its second stage when digit place changes, due to delay arrival. Therefore, take gate from HC32 or the like, not from C0 output at the rear stage directly

PROGRAMMABLE TIMER

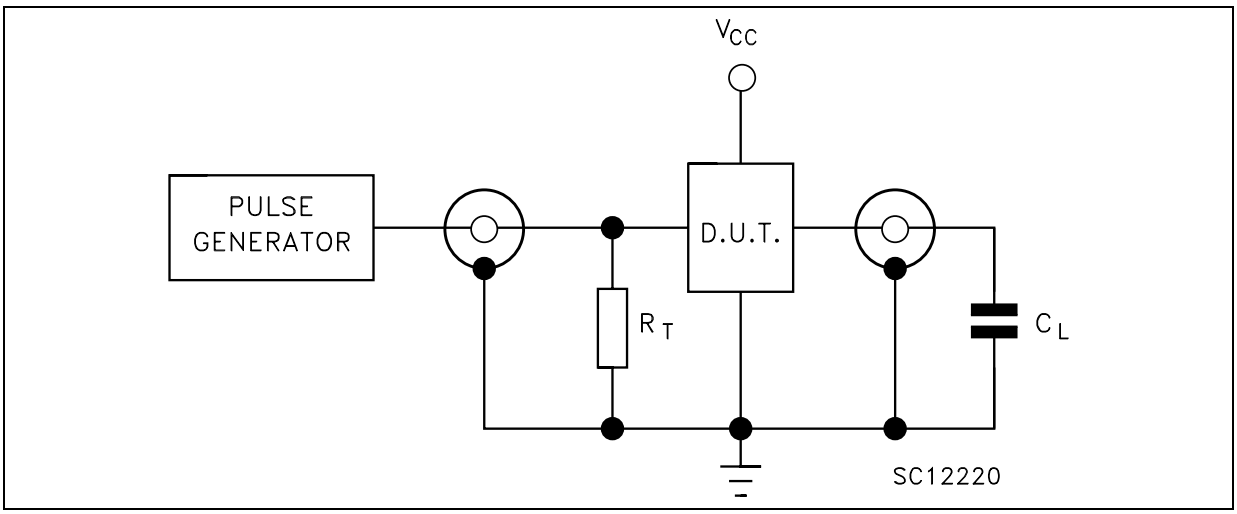




$$t_W = \left(\frac{N}{f_{IN}} + t_S\right)$$

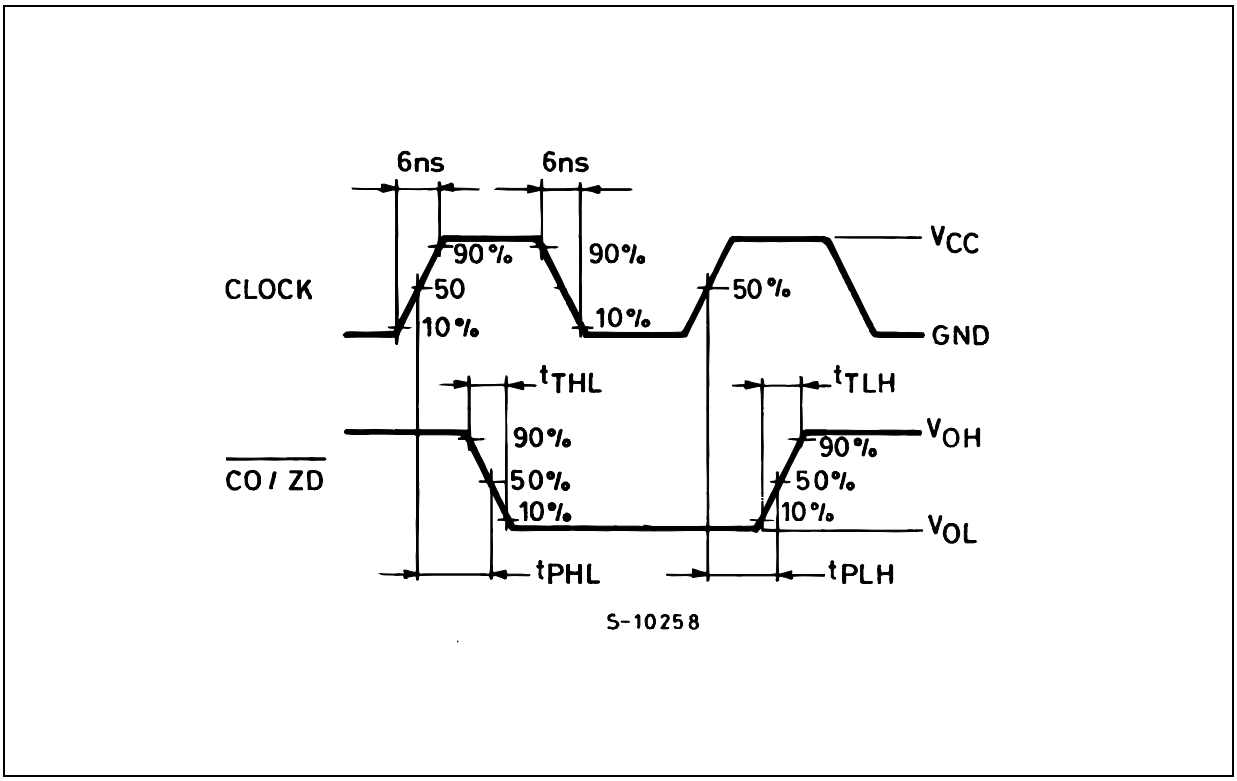
The above formula does not take into account the phase of clock input. Therefore, the real pulse width is the distance between the above formula-$1/f_{IN}$ ~ The above formula

TEST CIRCUIT

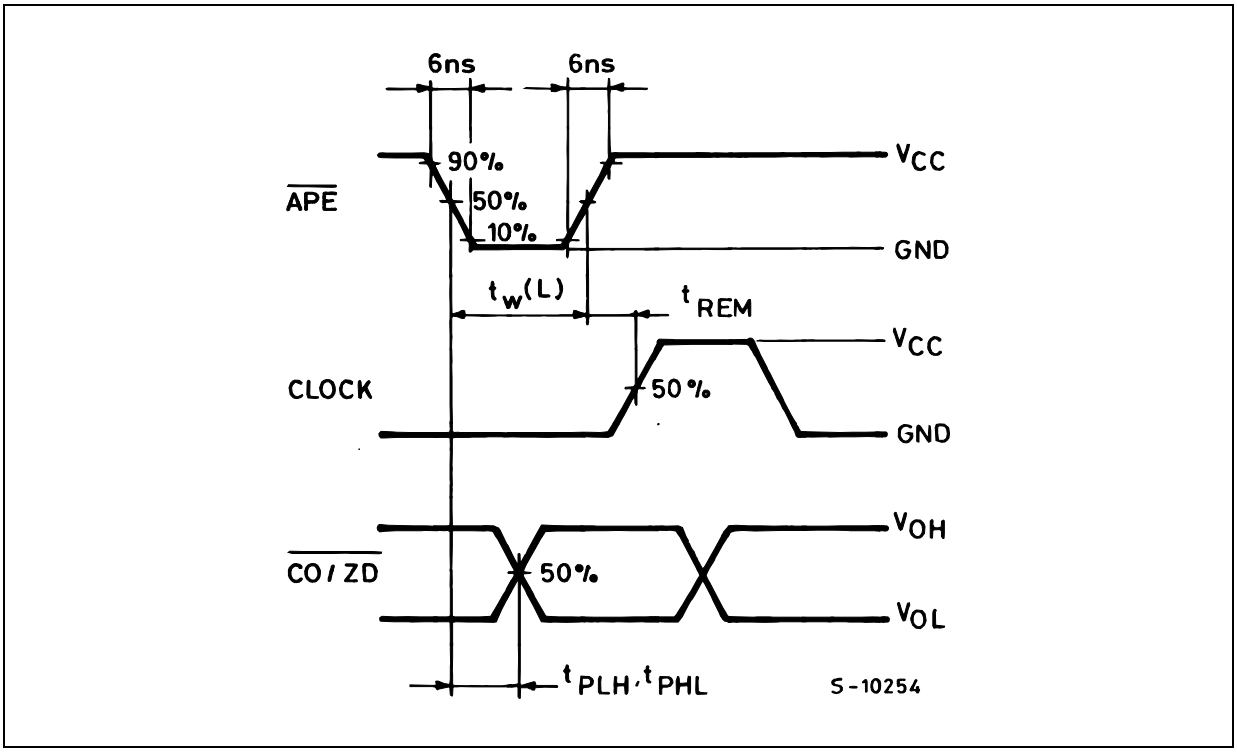


C_L = 50pF or equivalent (includes jig and probe capacitance)
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

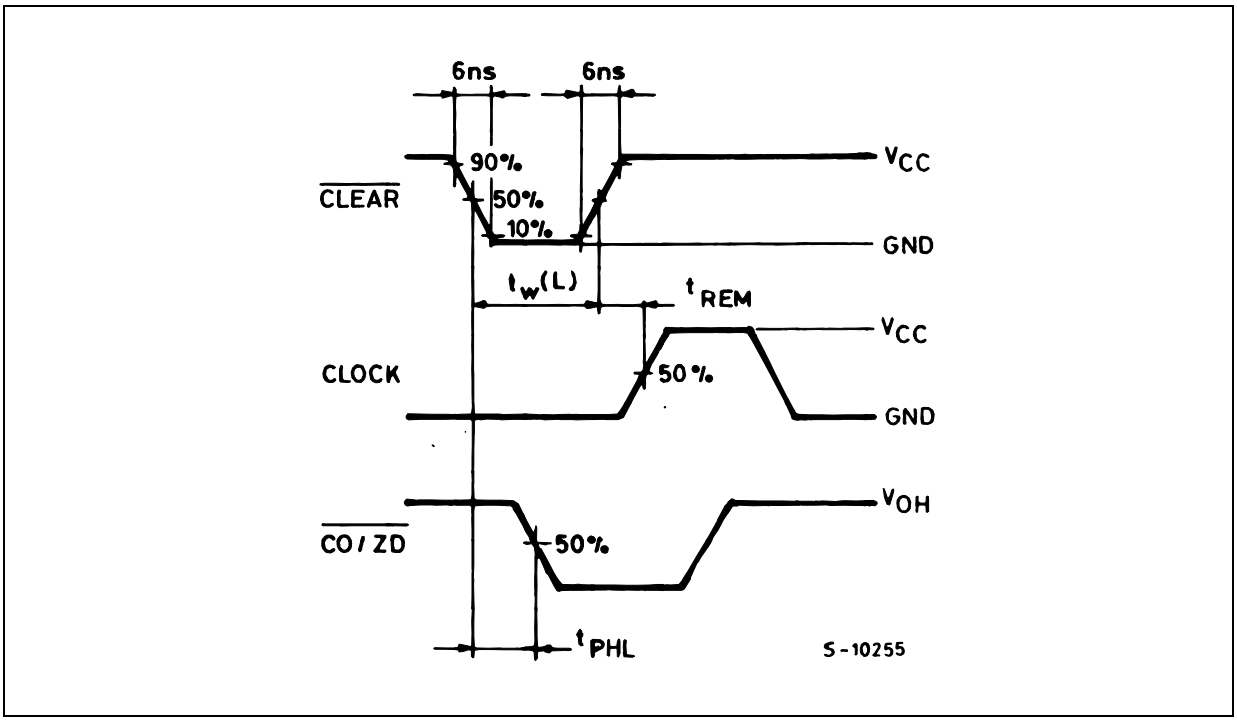
WAVEFORM 1 : PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



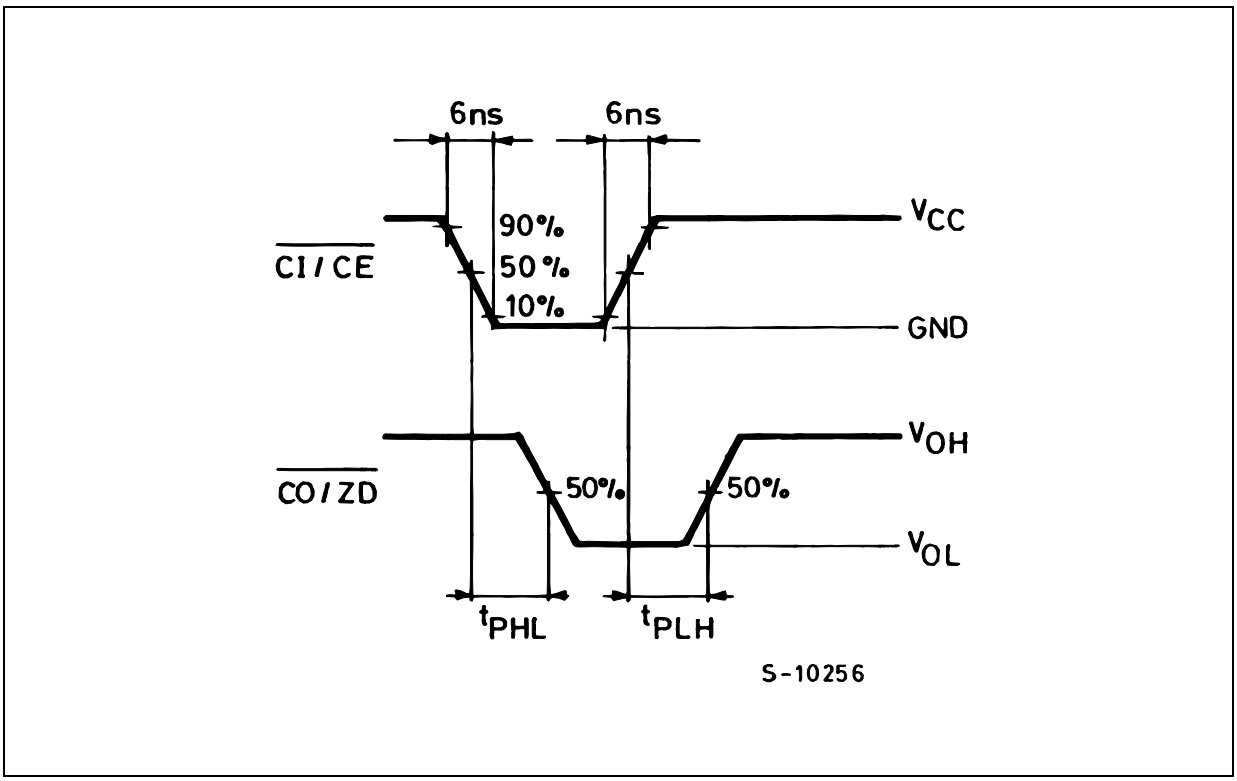
WAVEFORM 2 : PROPAGATION DELAY, MINIMUM PULSE WIDTH AND REMOVAL TIME
(f=1MHz; 50% duty cycle)



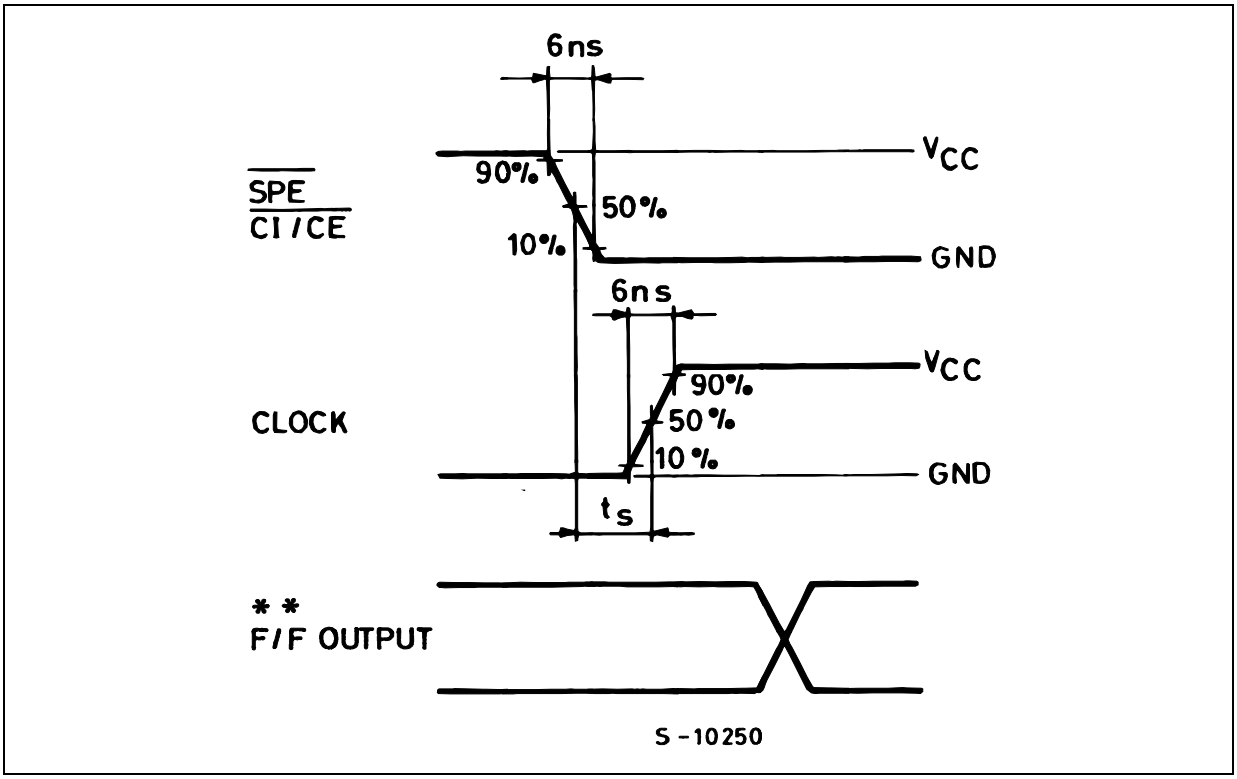
WAVEFORM 3 : PROPAGATION DELAY, MINIMUM PULSE WIDTH AND REMOVAL TIME
(f=1MHz; 50% duty cycle)



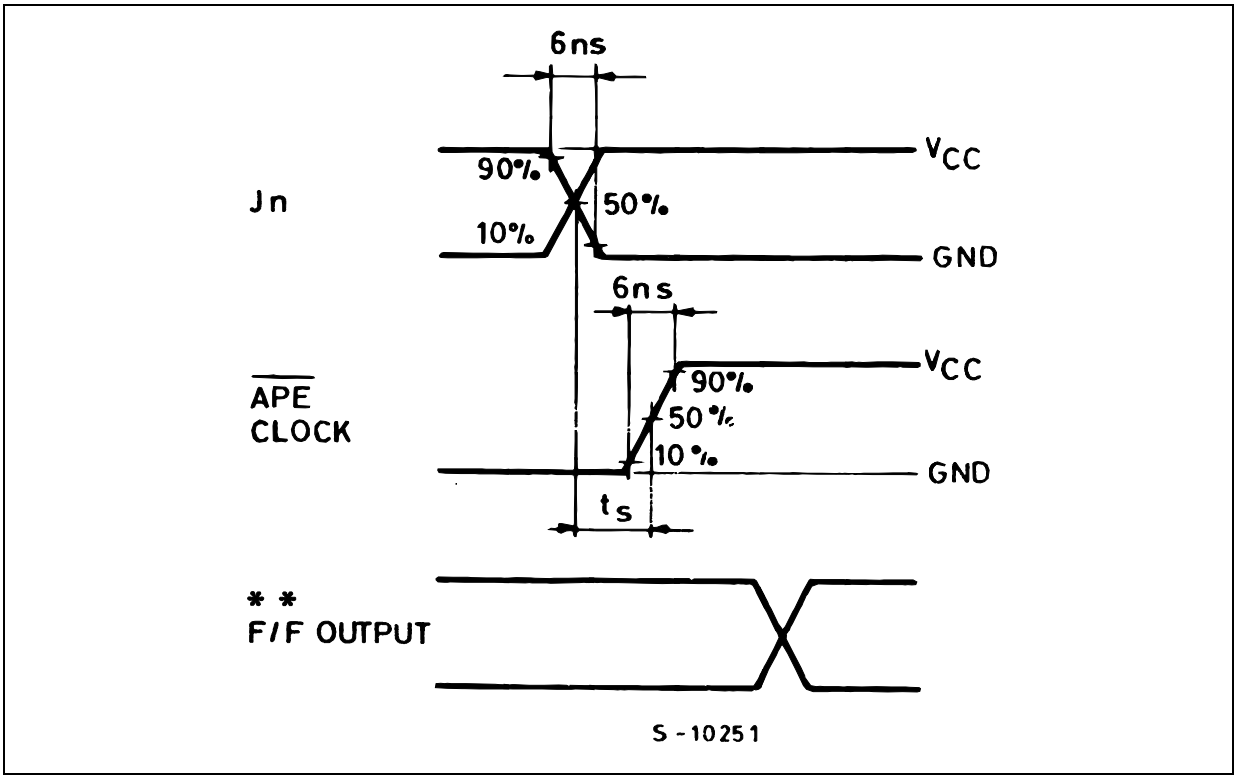
WAVEFORM 4 : PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



WAVEFORM 5 : MINIMUM SETUP TIME (f=1MHz; 50% duty cycle)

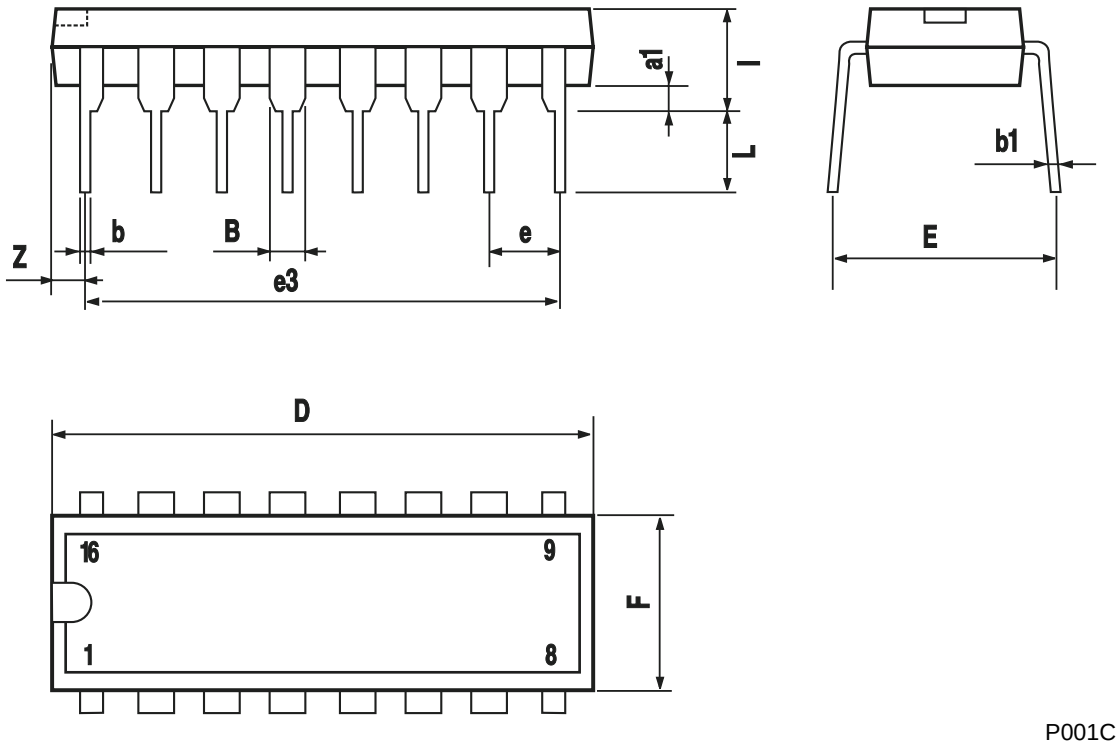


WAVEFORM 6 : MINIMUM SETUP TIME (f=1MHz; 50% duty cycle)



Plastic DIP-16 (0.25) MECHANICAL DATA

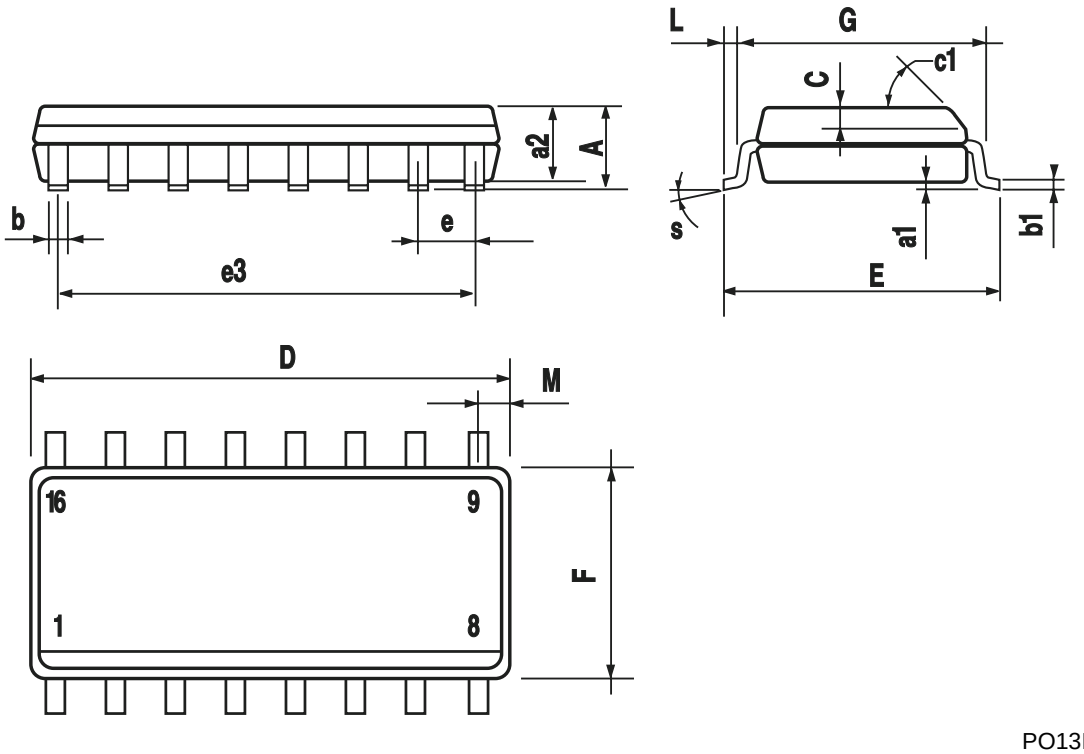
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030