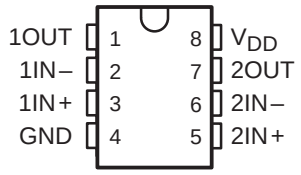
- **Trimmed Input Offset Voltage:**
  10 mV Max at 25°C, V_{DD} = 5 V
- **Input Offset Voltage Drift Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  –40°C to 150°C . . . 4 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends to the Negative Rail**
- **Low Noise . . . 25 nV/√Hz Typ at f = 1 kHz**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

D OR P PACKAGE
(TOP VIEW)



description

The TLC2810Z dual operational amplifiers combine low offset voltage drift with high input impedance, low noise, and speeds approaching that of general-purpose JFET devices. In addition, the use of Texas Instruments silicon-gate LinCMOS technology assures offset stability that greatly exceeds the stability available with conventional metal-gate processes.

The high input impedance, low bias current, and high slew rate make the TLC2810Z ideal for applications that have previously been reserved for JFET and NFET products. These advantages, in combination with an upper operating temperature of 150°C, make the TLC2810Z an ideal choice for precision, extremely high-temperature applications.

In general, many features associated with bipolar technology are available on the TLC2810Z without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are designed easily with the TLC2810Z.

The TLC2810Z package options include a small-outline version for high-density system applications.

The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up at 25°C. The TLC2810Z incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD 883C, Method 3015.2. However, care should be exercised in handling the TLC2810Z as exposure to ESD may result in the degradation of the device parametric performance. Additional care should be exercised to prevent V_{DD} supply line transients under power conditions. Transients of greater than 20 V can trigger the ESD-protection structure, inducing a low-impedance path to GND. Should this condition occur, the sustained current supplied to the device must be limited to 100 mA or less. Failure to do so can result in a latched condition and device failure.

The TLC2810Z is characterized for operation over the extended temperature range from –40°C to 150°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (D)†	PLASTIC DIP (P)	
–40°C to 150°C	TLC2810ZD	TLC2810ZP	TLC2810Y

† The D packages are available taped and reeled. Add R suffix to the device type when ordering (e.g., TLC2810ZDR).

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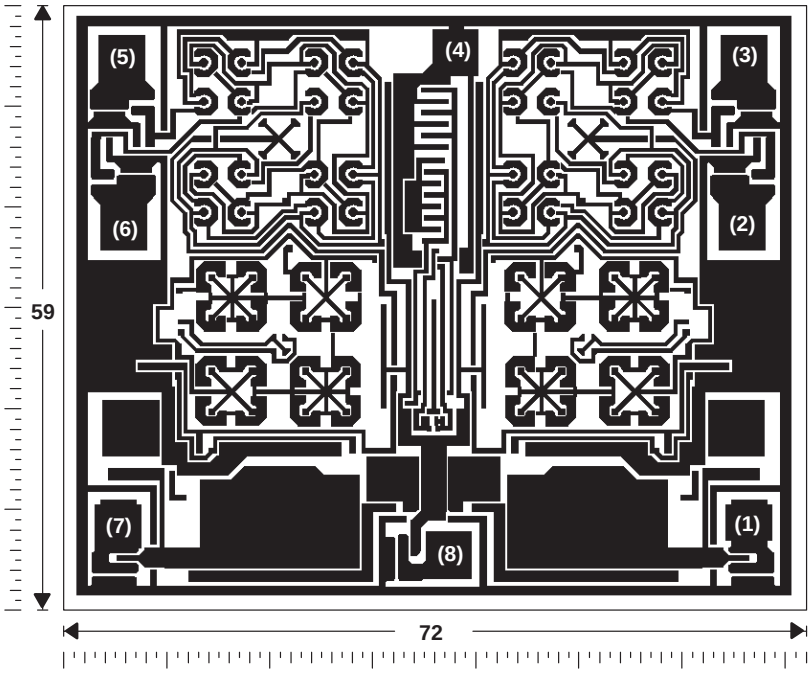
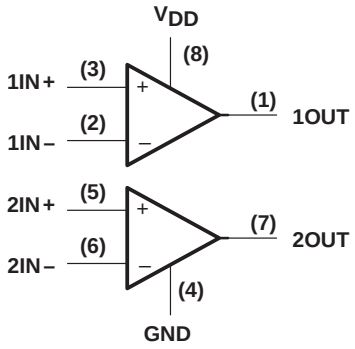
TLC2810Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC2810Z. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

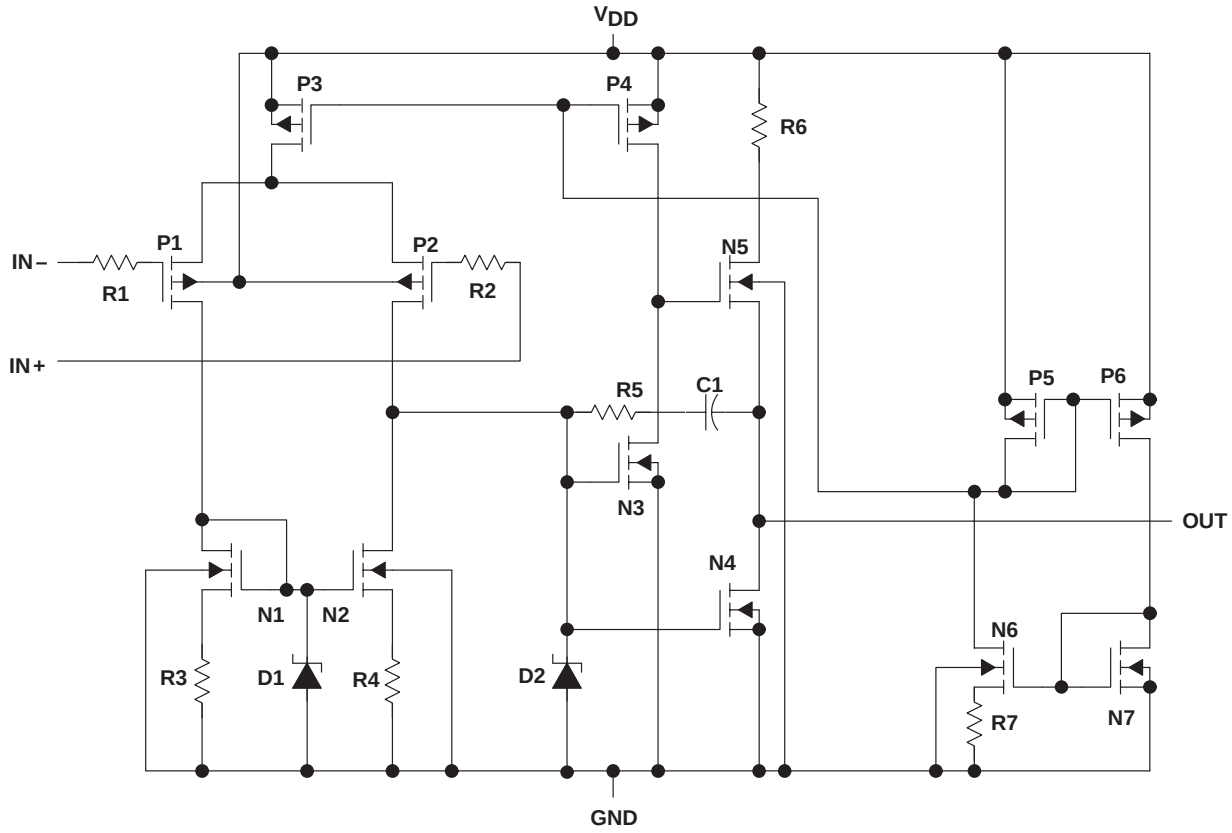
$T_J$max = 165°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



COMPONENT COUNT †	
Transistors	26
Diodes	4
Resistors	14
Capacitors	2

† Includes both amplifiers

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 16 V
Differential input voltage, V_{ID} (see Note 2) . . . . . $\pm V_{DD}$
Input voltage range, V_I (any input) . . . . . –0.3 V to V_{DD}
Input current, I_I . . . . . ±2 mA
Output current, I_O (each output) . . . . . ±30 mA
Total current into V_{DD} . . . . . 45 mA
Total current out of GND . . . . . 45 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . –40°C to 150°C
Storage temperature range . . . . . –65°C to 165°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN–.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application selection).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING	$T_A = 150°C$ POWER RATING
D	812 mV	5.8 mW/°C	551 mW	348 mW	232 mW	87 mW
P	1120 mV	8.0 mW/°C	760 mW	480 mW	320 mW	120 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V, T_A = 25°C	–0.2	3.5	V
Input voltage, V_I	V_{DD} = 5 V	–0.2	3.5	V
Operating free-air temperature, T_A		–40	150	°C

electrical characteristics, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLC2810Z			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.8	10	mV
			Full range			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 150°C		3.5		μV/°C
I_{IO}	Input offset current (see Note 4)	V_{IC} = 1 V, V_O = 1 V	25°C		2.4	100	pA
			150°C		5.2	30	nA
I_{IB}	Input bias current (see Note 4)	V_{IC} = 1 V, V_O = 1 V	25°C		7	100	pA
			150°C		50	150	nA
V_{ICR}	Common-mode input voltage range (see Note 5)	R_S = 50 Ω	25°C	−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	3.2	3.8		V
			Full range	3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		80	150	mV
			Full range			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, V_O = 0.25 V to 2 V, R_L = 10 kΩ	25°C	5	25		V/mV
			Full range	4			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	90		dB
			Full range	60			
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 4 V to 16 V, V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω	25°C	65	75		dB
			Full range	60			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		1	3.2	mA
			Full range			4.4	

† Full range is −40°C to 150°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	TLC2810Z			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 26	$V_{I(PP)}$ = 1 V	25°C		3.6		V/μs
				150°C		2.8		
			$V_{I(PP)}$ = 2.5 V	25°C		2.2		
				150°C		2.1		
V_n	Equivalent input noise voltage	f =1 kHz, See Figure 27	R_S = 20 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	$V_O = V_{OH}$, R_L = 10 kΩ,	C_L = 20 pF, See Figure 26	25°C		320		kHz
				150°C		200		
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 28	C_L = 20 pF,	25°C		1.7		MHz
				150°C		0.8		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 28	25°C		46°		
				150°C		40°		

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLC2810Y MIN	TLC2810Y TYP	TLC2810Y MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 1 V, R_S = 50 Ω	V_O = 1 V,			10	mV
I_{IO}	Input offset current (see Note 4)					100	pA
I_{IB}	Input bias current (see Note 4)					100	pA
V_{ICR}	Common-mode input voltage range (see Note 5)	R_S = 50 Ω		–0.2 to 4			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, I_{OH} = –1 mA	V_{ID} = 100 mV,	3.2			V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, I_{OL} = 1 mA	V_{ID} = –100 mV,			150	mV
A_{VD}	Large-signal differential voltage amplification	V_O = 0.25 V to 2 V, V_{IC} = 1 V	R_L = 10 kΩ,	5			V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, R_S = 50 Ω	V_{IC} = V_{ICR}min,	65			dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4 V to 16 V, V_O = 1 V,	V_{IC} = 1 V, R_S = 50 Ω	65			dB
I_{DD}	Supply current	V_O = 1 V, No load	V_{IC} = 1 V,			3.2	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC2810Y MIN	TLC2810Y TYP	TLC2810Y MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 26	$V_{I(PP)}$ = 1 V		3.6		V/μs
			$V_{I(PP)}$ = 2.5 V		2.9		
V_n	Equivalent input noise voltage	f =1 kHz, See Figure 27	R_S = 20 Ω,		25		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 26		320		kHz
B_1	Unity-gain bandwidth	V_I = 10 mV, See Figure 28	C_L = 20 pF,		1.7		MHz
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF,	f = B_1, See Figure 28		46°		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1
α_{VIO}	Input offset voltage temperature coefficient	Distribution	2
V_{OH}	High-level output voltage	vs Output current vs Supply voltage vs Free-air temperature	3 4 5
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	6 7 8 9
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	10 11 21
I_{IB}/I_{IO}	Input bias and offset current	vs Free-air temperature	12
V_{IC}	Common-mode input voltage	vs Supply voltage	13
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	14 15
SR	Slew rate	vs Supply voltage vs Free-air temperature	16 17
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	18
B_1	Gain-bandwidth product	vs Free-air temperature vs Supply voltage	19 20
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature vs Load capacitance	22 23 24
V_n	Equivalent input noise voltage	vs Frequency	25
	Phase shift	vs Frequency	21

TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLC2810Z
INPUT OFFSET VOLTAGE**

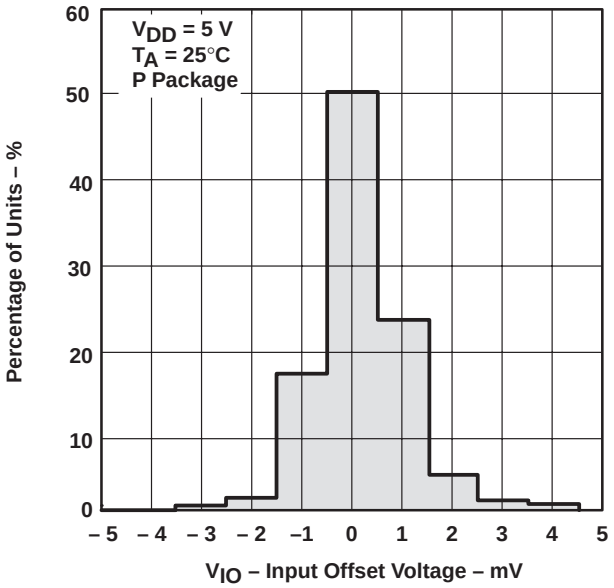


Figure 1

**DISTRIBUTION OF TLC2810Z
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

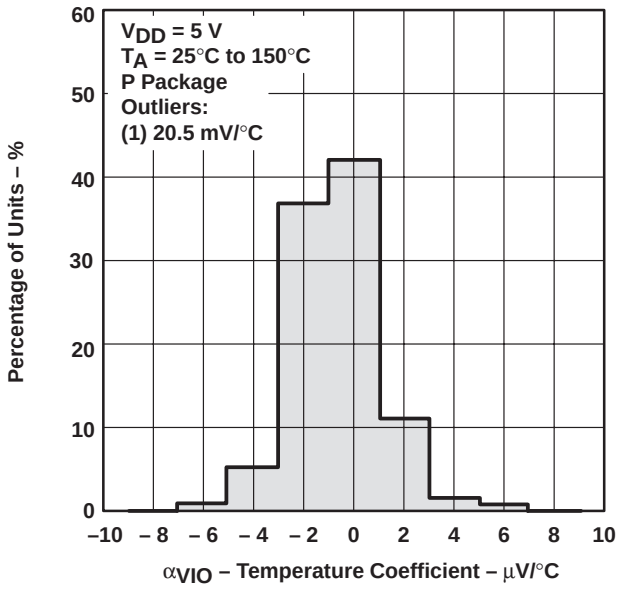


Figure 2

**HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

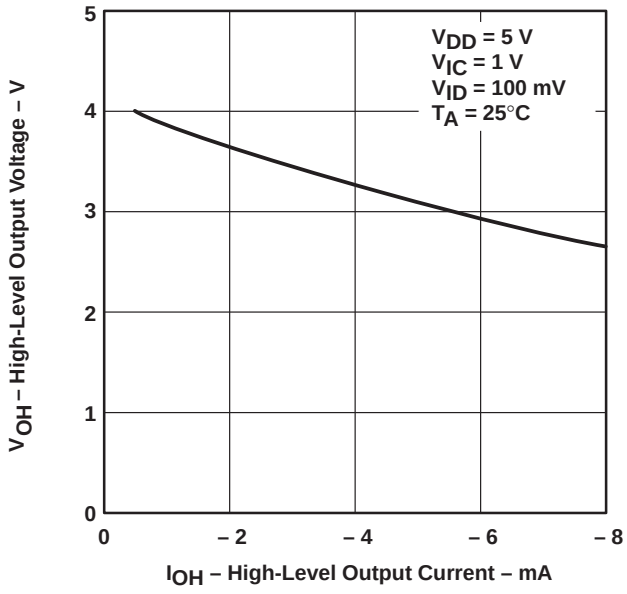


Figure 3

**HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE**

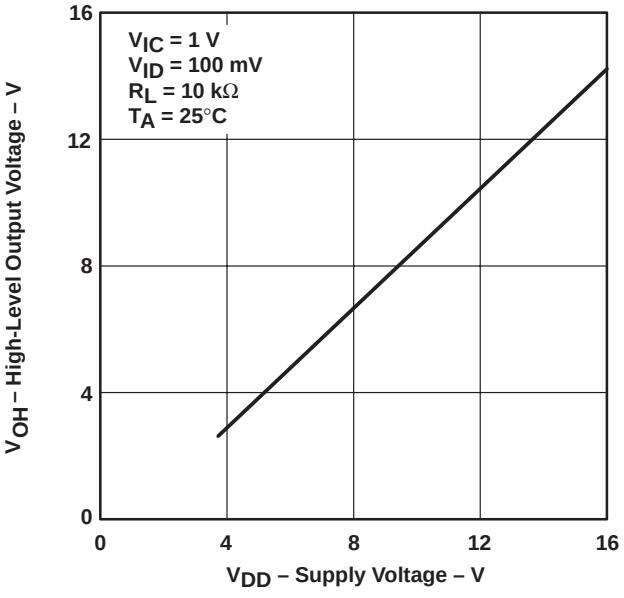


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

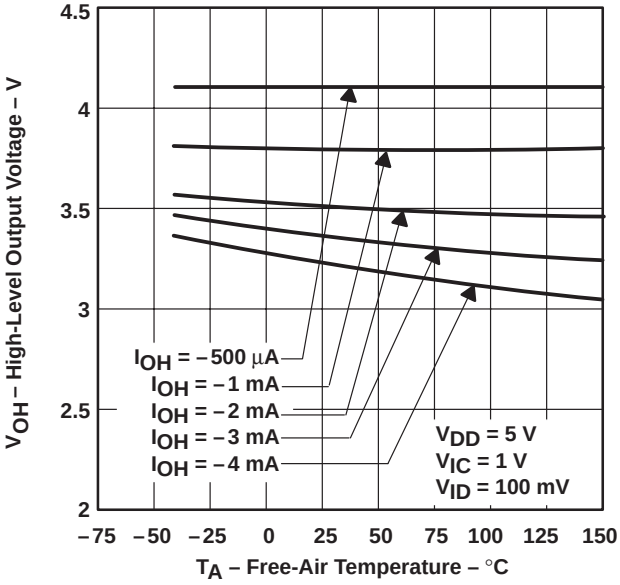


Figure 5

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

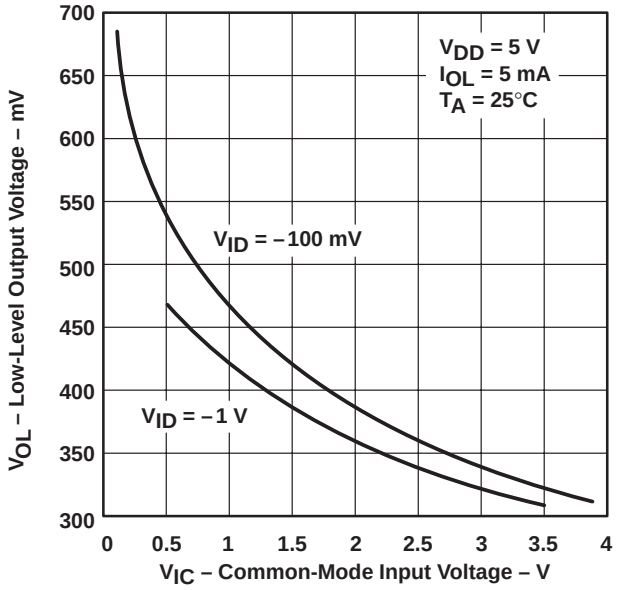


Figure 6

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

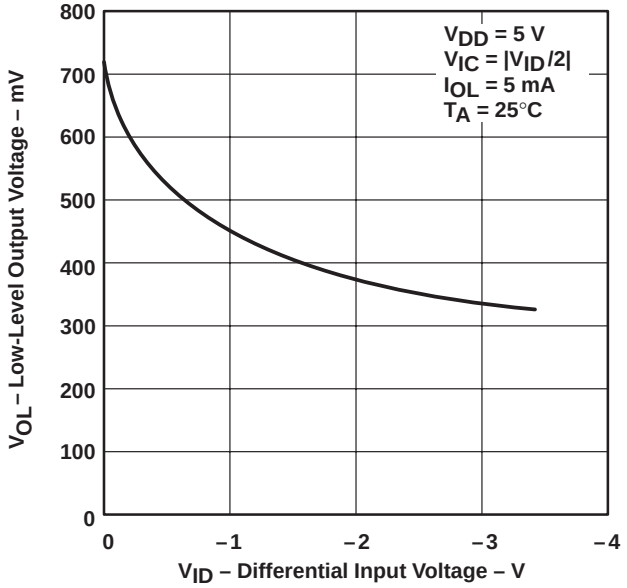


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

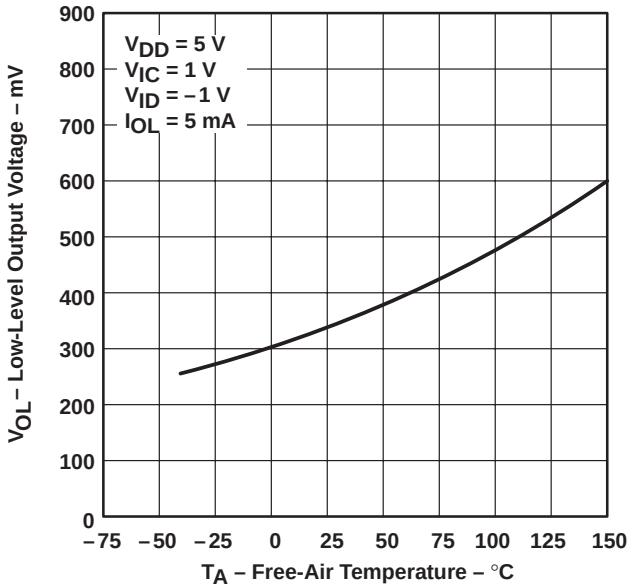


Figure 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

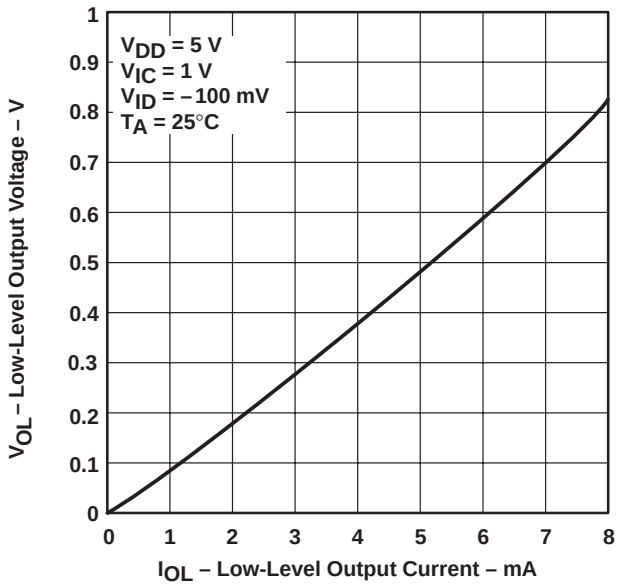


Figure 9

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

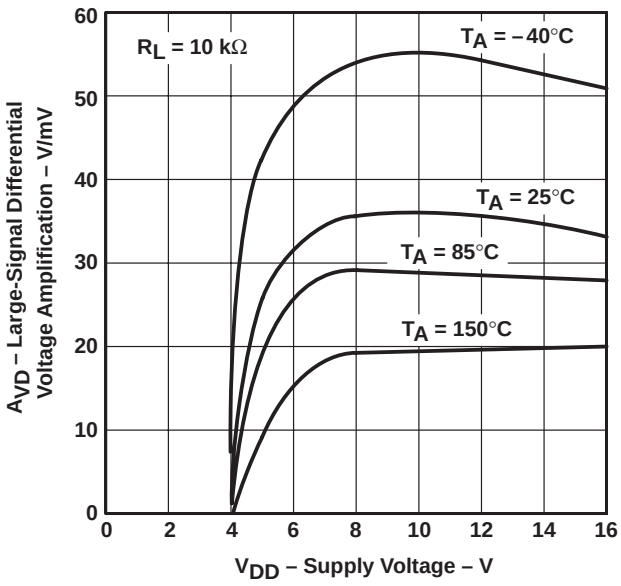


Figure 10

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

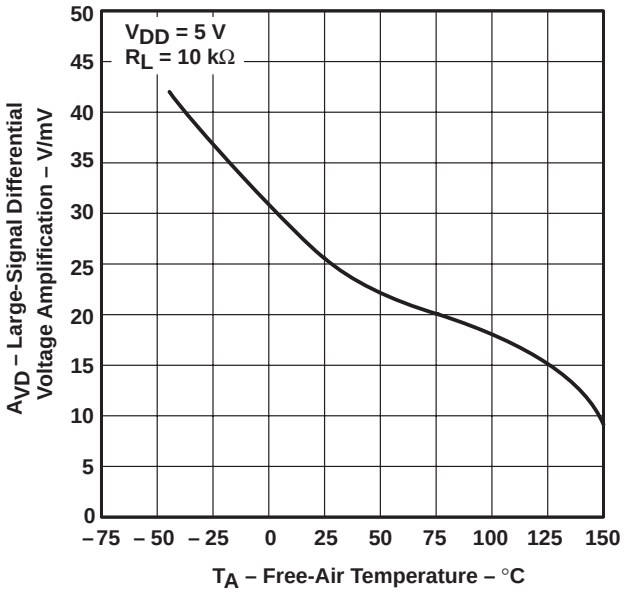
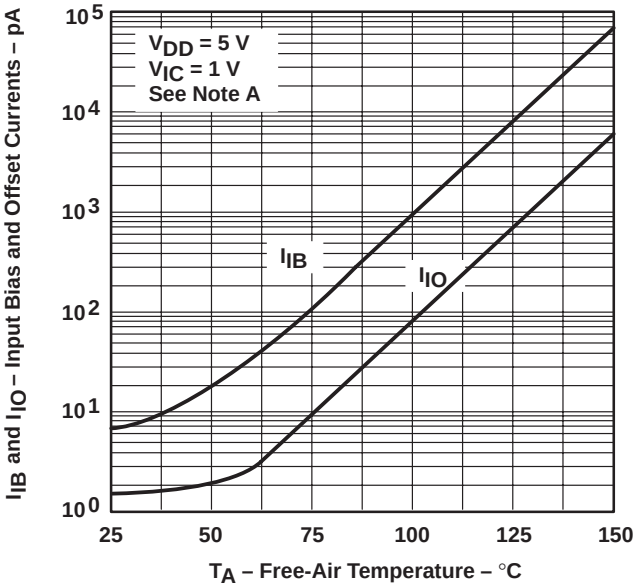


Figure 11

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 12

TYPICAL CHARACTERISTICS

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

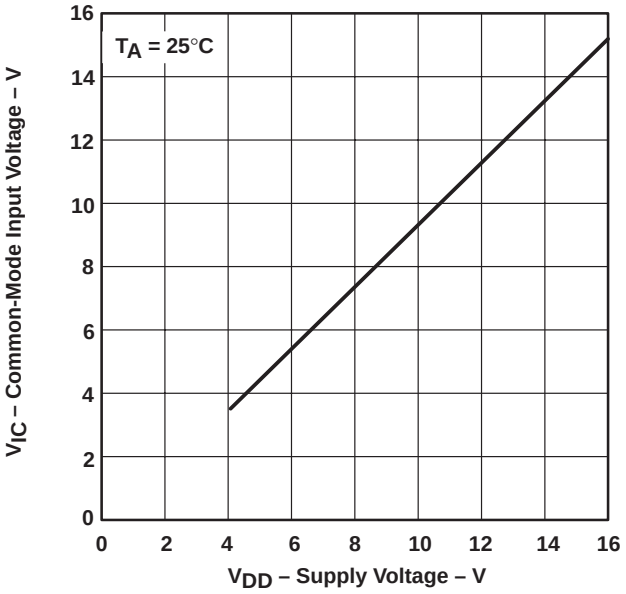


Figure 13

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

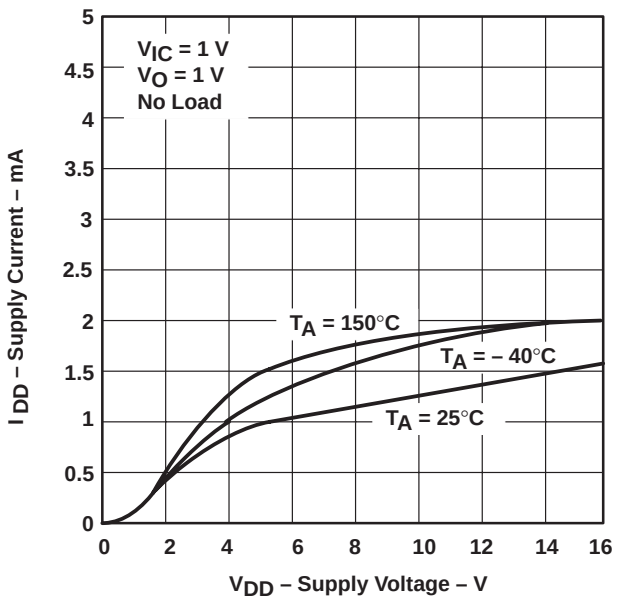


Figure 14

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

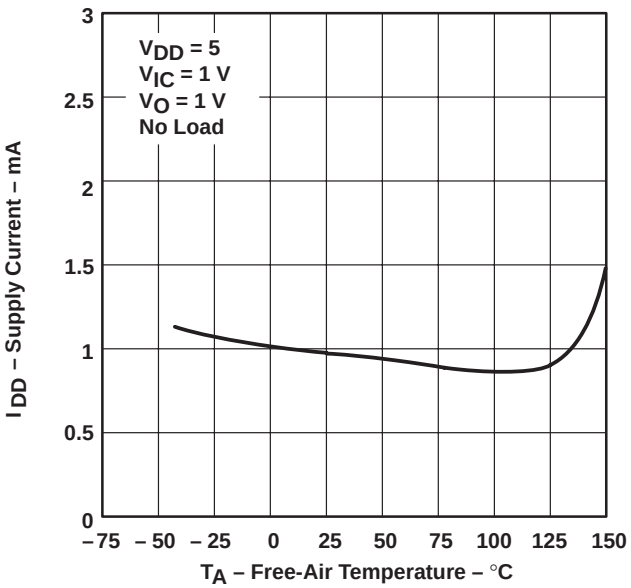


Figure 15

SLEW RATE
vs
SUPPLY VOLTAGE

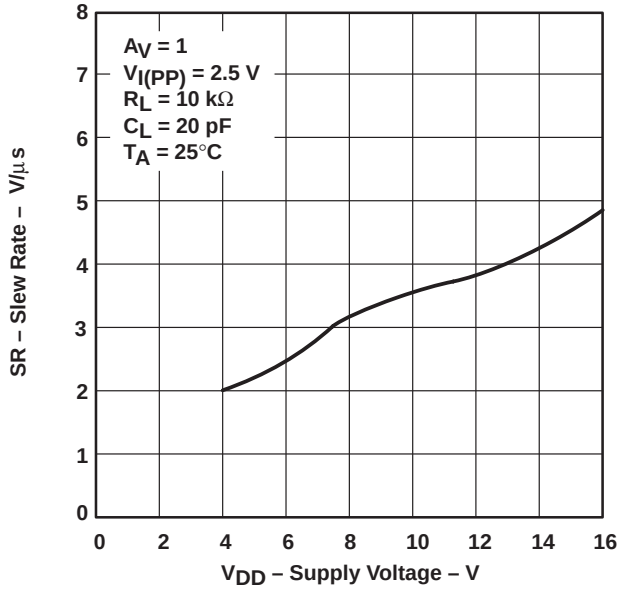


Figure 16

TYPICAL CHARACTERISTICS

SLEW RATE vs FREE-AIR TEMPERATURE

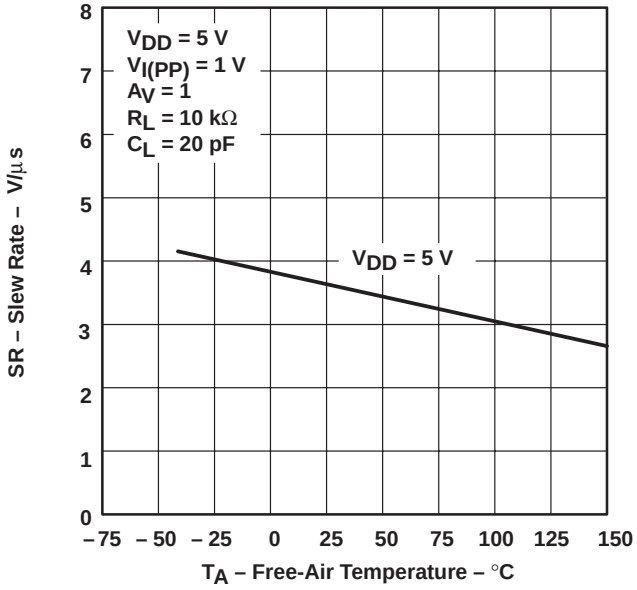


Figure 17

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

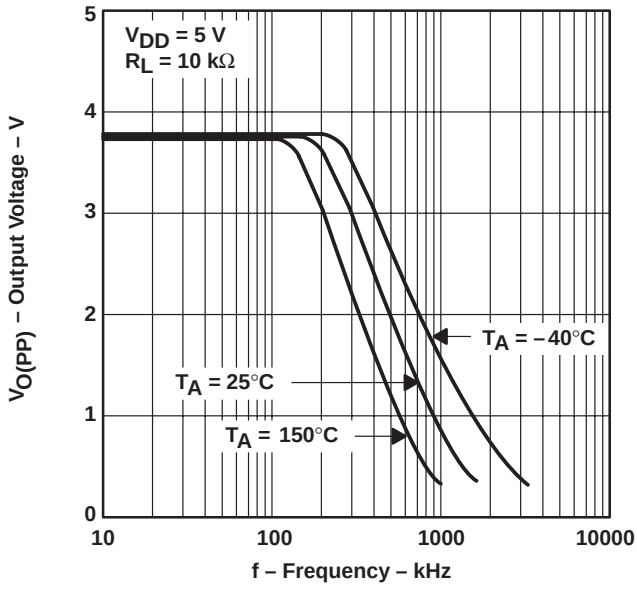


Figure 18

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

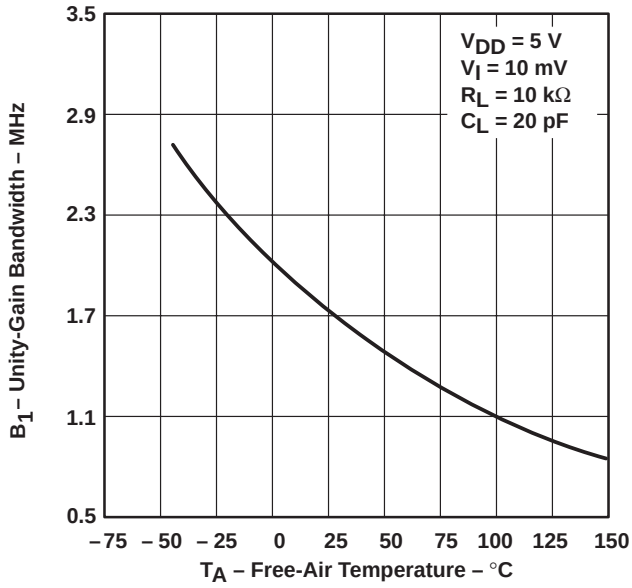


Figure 19

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

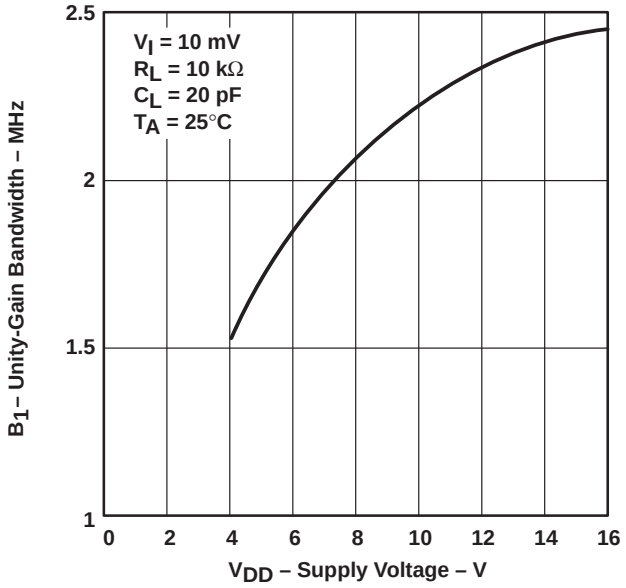


Figure 20

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

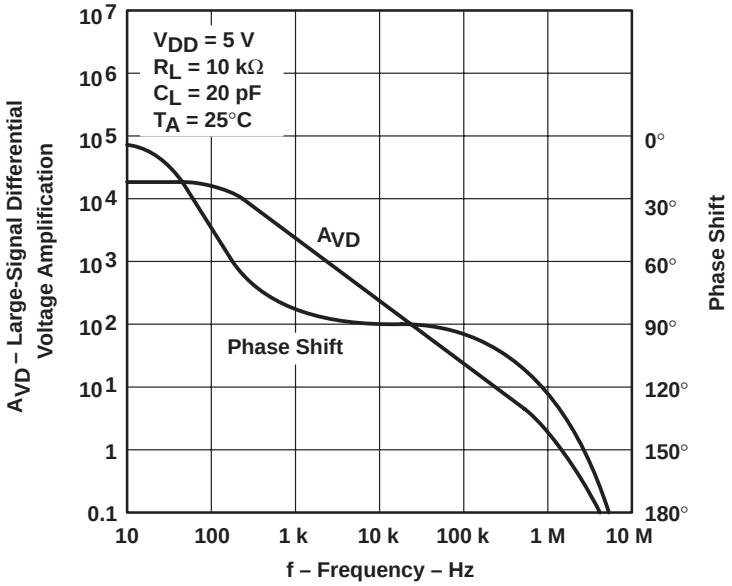


Figure 21

PHASE MARGIN vs SUPPLY VOLTAGE

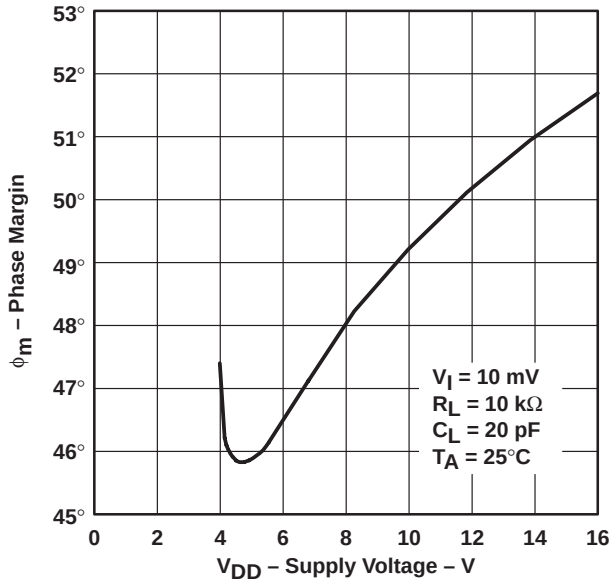


Figure 22

PHASE MARGIN vs FREE-AIR TEMPERATURE

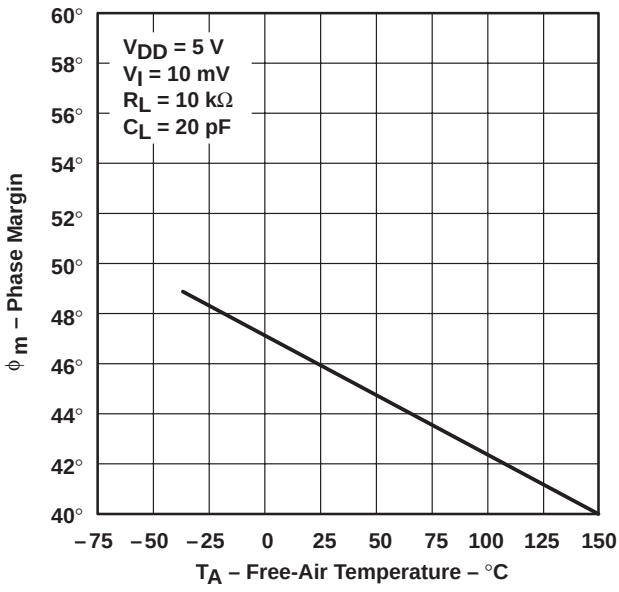


Figure 23

TYPICAL CHARACTERISTICS

PHASE MARGIN vs LOAD CAPACITANCE

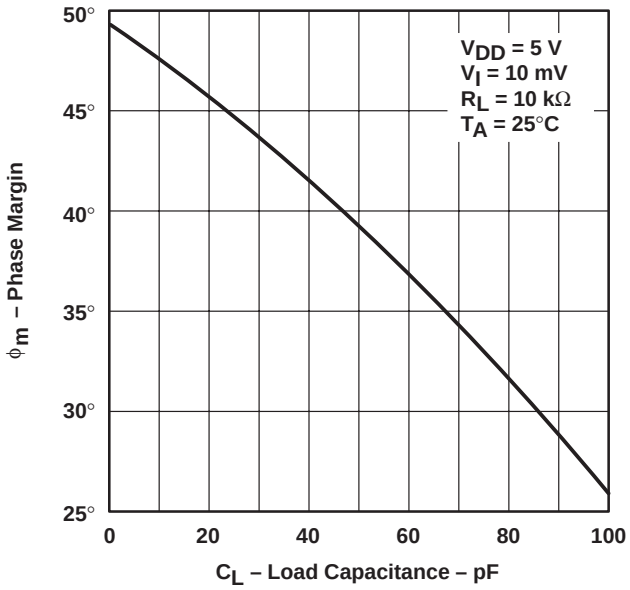


Figure 24

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

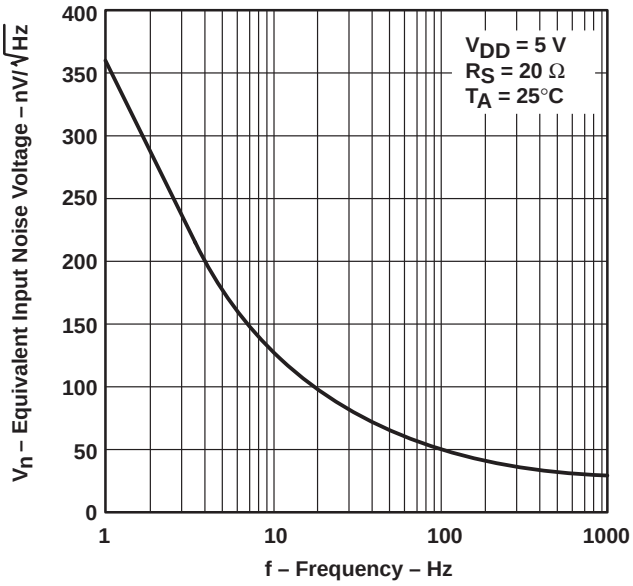


Figure 25

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC2810Z is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply and split-supply test circuits is shown below. The use of either circuit gives the same result.

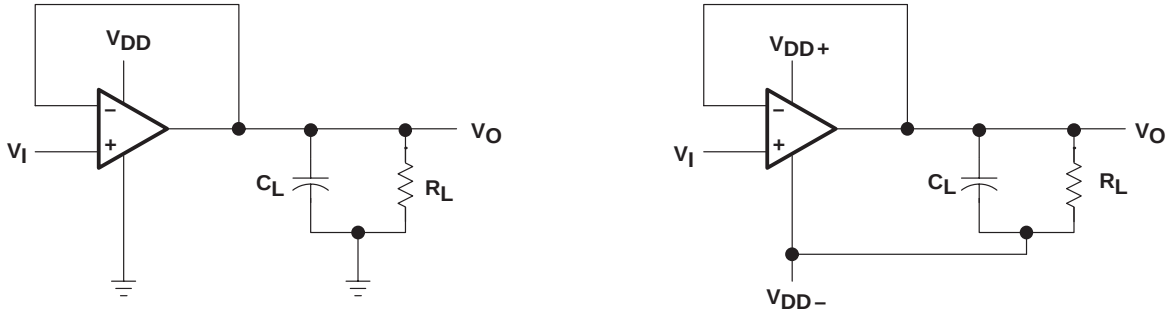


Figure 26. Unity-Gain Amplifier

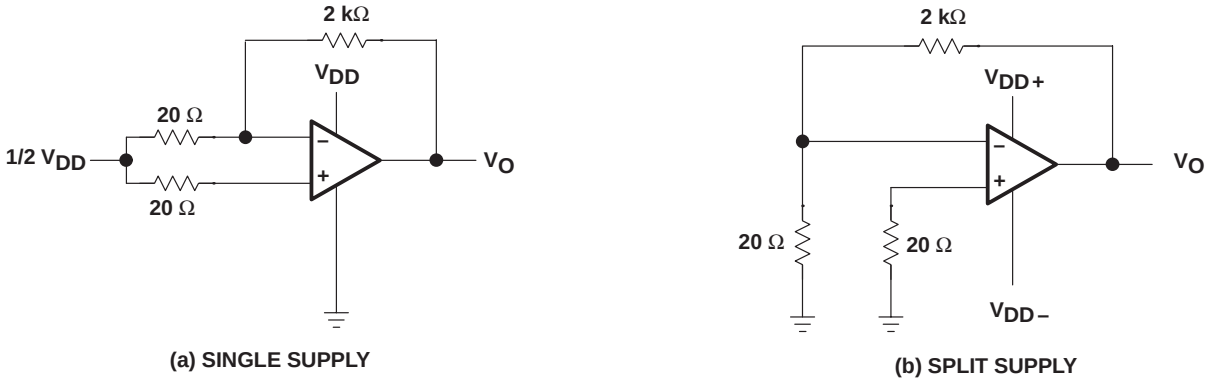


Figure 27. Noise-Test Circuit

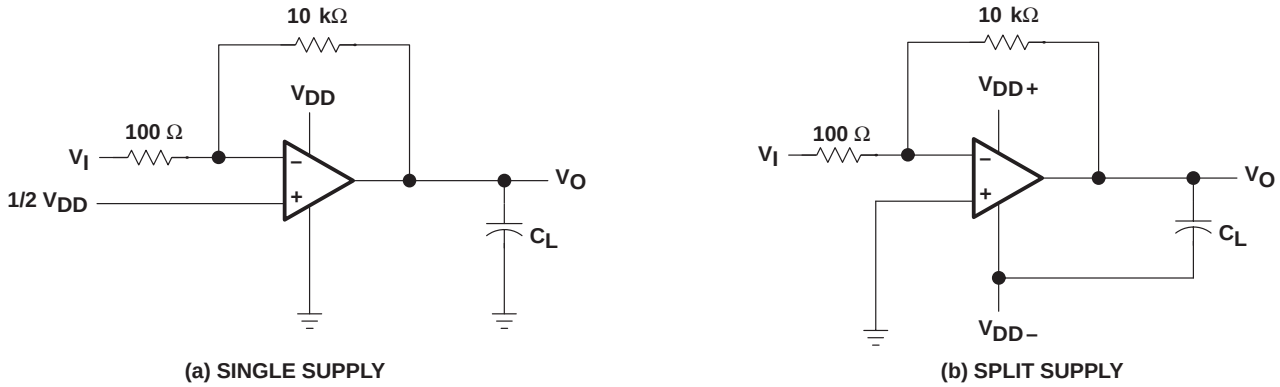


Figure 28. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC2810Z operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 29). Leakages that would otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading: therefore, an open-socket reading is not feasible using this method.

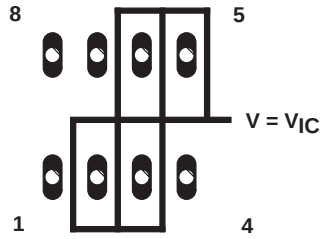


Figure 29. Isolation Metal Around Device Inputs (P package)

low-level output voltage

To obtain low-supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance that can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

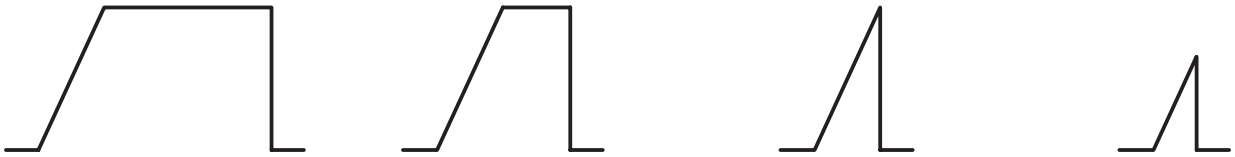
full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal

full-power response (continued)

input signal until the maximum frequency above which the output contains significant distortion is found. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 26. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 30). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) f = 100 Hz **(b) B_{OM} > f > 100 Hz** **(c) f = B_{OM}** **(d) f > B_{OM}**

Figure 30. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices; hence, CMOS devices require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced power supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLC2810Z performs well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 4 V, thus allowing operation with supply levels commonly available for TTL and CMOS.

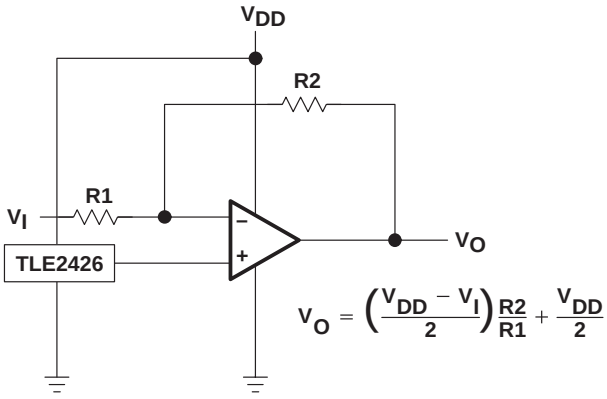


Figure 31. Inverting Amplifier With Voltage Reference

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual ground generator such as the TLE2426 (see Figure 31). The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power and is suitable for supply voltages of greater than 4 V.

The TLC2810Z works well in conjunction with digital logic. However, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 32). Otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate. However, RC decoupling may be necessary in high-frequency applications.

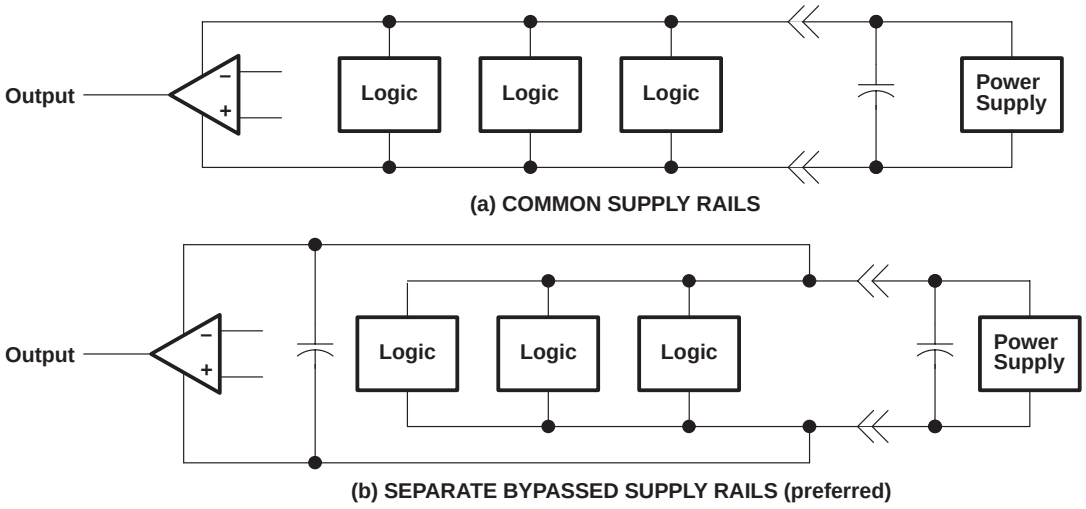


Figure 32. Common Versus Separate Supply Rails

APPLICATION INFORMATION

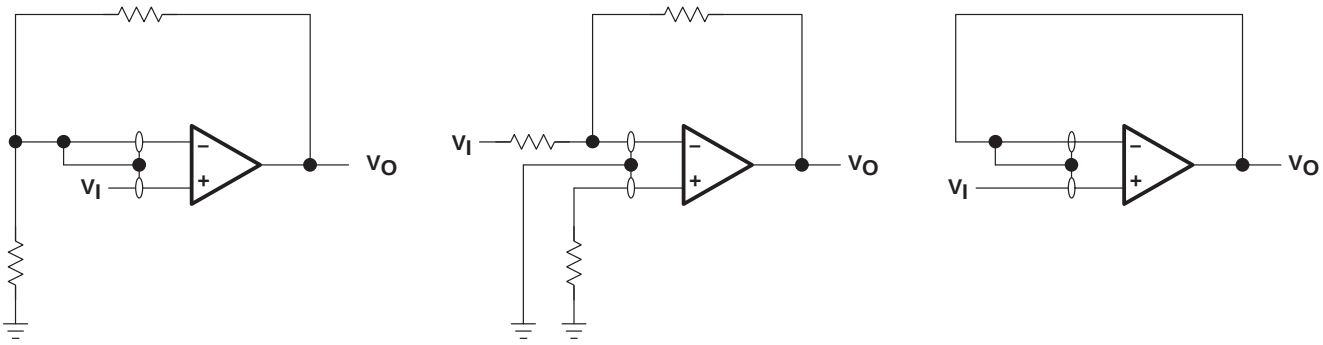
input characteristics

The TLC2810Z is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. The lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} –1 V at T_A = 25°C and at V_{DD}– 1.2 V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design give the TLC2810Z very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low-bias current requirements, the TLC2810Z is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 29 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 33).

Unused amplifiers should be connected as grounded voltage followers to avoid possible oscillation.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 33. Guard-Ring Schemes

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC2810Z results in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ since bipolar devices exhibit greater noise currents.

APPLICATION INFORMATION

feedback

Operational amplifier circuits nearly always employ feedback and, since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 34). The value of this capacitor is optimized empirically.

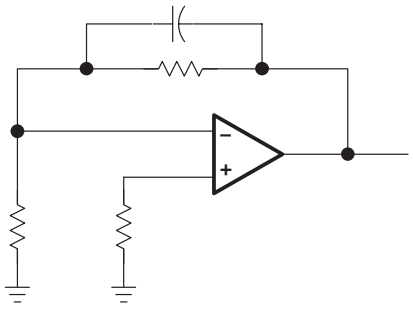


Figure 34. Compensation for Input Capacitance

electrostatic discharge protection

The TLC2810Z incorporates an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC2810Z inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not by design be forward biased. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

APPLICATION INFORMATION

output characteristics

The output stage of the TLC2810Z is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLC2810Z possesses excellent high-level output voltage and current capability, methods are available for boosting this capability if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 35). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor, N4 (see equivalent schematic), must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4, and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

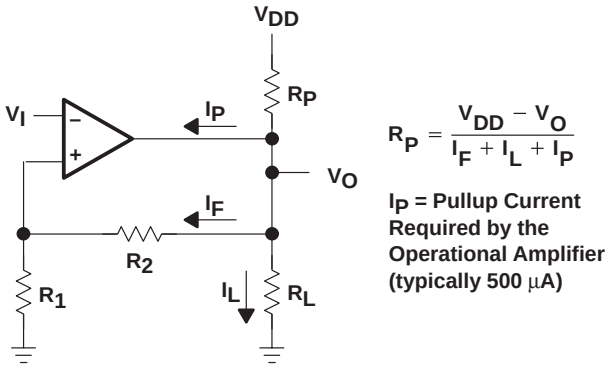


Figure 35. Resistive Pullup to Increase V_{OH}

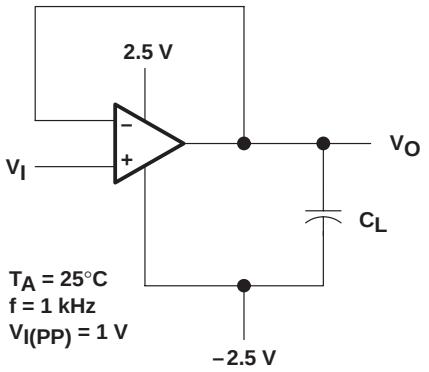
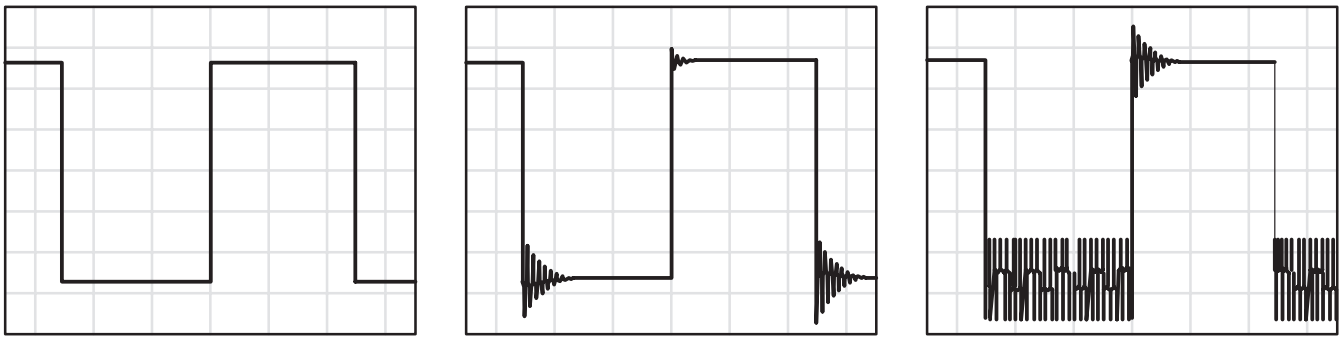


Figure 36. Test Circuit for Output Characteristics

All operating characteristics of the TLC2810Z are measured using a 20-pF load. The devices can drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 37). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.



(a) C_L = 20 pF, R_L = NO LOAD

(b) C_L = 130 pF, R_L = NO LOAD

(c) C_L = 150 pF, R_L = NO LOAD

Figure 37. Effect of Capacitive Loads

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