UNITRODE

UC1910
UC2910
UC3910

4-Bit DAC and Voltage Monitor

FEATURES

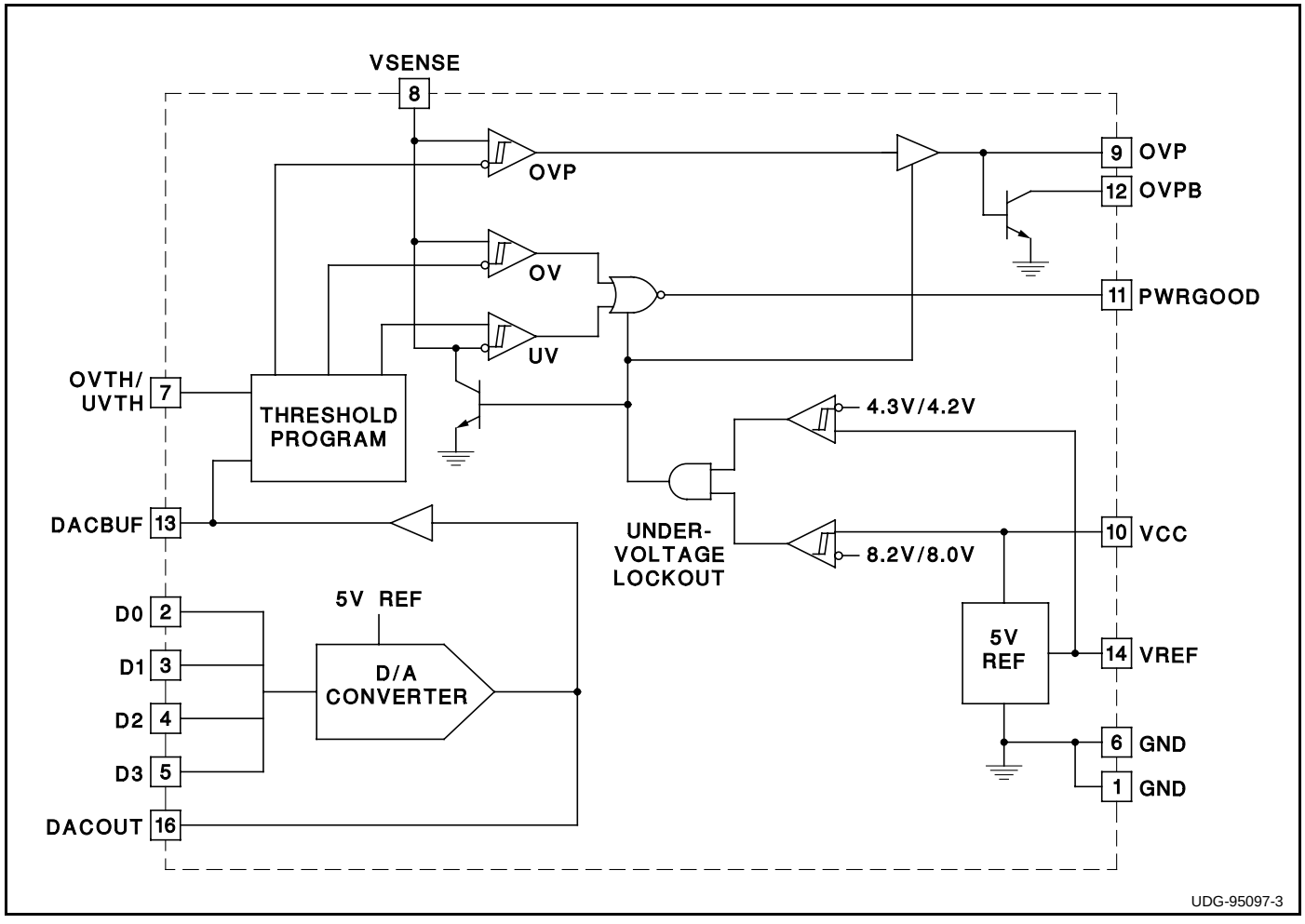
- Precision 5V Reference
- 4-Bit Digital-to-Analog (DAC) Converter
- 0.5% DAC/Reference Combined Error
- Programmable Undervoltage and Overvoltage Fault Windows
- Overvoltage Comparator with Complementary SCR Driver and Open Collector Outputs
- Undervoltage Lockout

DESCRIPTION

The UC3910 is a complete precision reference and voltage monitor circuit for Intel Pentium® Pro and other high-end microprocessor power supplies. It is designed for use in conjunction with the UC3886 PWM. The UC3910 together with the UC3886 converts 5VDC to an adjustable output ranging from 2.0VDC to 3.5VDC in 100mV steps with 1% DC system accuracy.

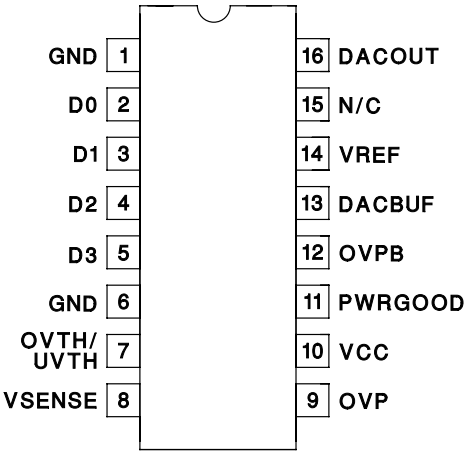
The UC3910 utilizes thin film resistors to ensure high accuracy and stability of its precision circuits. The chip includes a precision 5V voltage reference which is capable of sourcing 10mA to external circuitry. The output voltage of the DAC is derived from this reference, and the accuracy of the DAC/reference combination is 0.5%. Programmable window comparators monitor the supply voltage to indicate that it is within acceptable limits. The window is programmed as a percentage centered around the DAC output. An overvoltage protection comparator is set at a percentage 2 times larger than the programmed lower overvoltage level and drives an external SCR as well as provides an open collector output. Undervoltage lockout protection assures the correct logic states at the outputs during power-up and power-down.

BLOCK DIAGRAM



CONNECTION DIAGRAM

DIL-16, SOIC-16 (Top View)
J, N, or D Packages



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, VCC = 12V, VSENSE = 3.5V, $V_{OVTH/UVTH}$ = 1.26V, $V_{D0} = V_{D1} = V_{D2} = V_{D3}$ = 0V, 0°C < T_A < 70°C for the UC3910, –25°C < T_A < 80°C for the UC2910, –55°C < T_A < 125°C for the UC1910 $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout					
V_{IN} UVLO Turn-on Threshold		7	8	9	V
UVLO Threshold Hysteresis		50	200	500	mV
Supply Current					
I_{IN} Startup	VCC = 5V		2	3.5	mA
I_{IN}	VCC = 12V		10	12	mA
DAC/Reference					
DACOUT Voltage Accuracy	Line, Load, 0°C < T_A < 70°C (Note 1)	–0.9		0.9	%
	Line, Load, –55°C < T_A < 125°C	–1.5		1.5	%
D0-D3 Voltage High	D_X Pin Floating	4.6	4.85		V
D0-D3 Input Bias Current	D_X Pin Tied to GND	–140	–105		µA
VREF Output Voltage	I_{VREF} = 0mA, 0°C < T_A < 70°C	4.97	5	5.03	V
VREF Total Variation	Line, Load, 0°C < T_A < 70°C (Note 1)	4.96	5	5.04	V
	Line, Load, –55°C < T_A < 125°C	4.925	5	5.075	V
VREF Sourcing Current	VREF = 0V	10			mA
DAC Buffer					
Input Offset Voltage	I_{DACBUF} = –1mA, 0°C < T_A < 70°C	–25		25	mV
Output Sourcing Current		–12		–1	mA
Monitor Circuitry (Note 2)					
VSENSE UV Threshold Voltage	Code 0, Ratio = 0.45 (Note 3)	3.174	3.237	3.3	V
	Code 0, Ratio = 0.9	2.87	2.975	3.08	V
	Code 15, Ratio = 0.45	1.816	1.85	1.884	V
	Code 15, Ratio = 0.9	1.635	1.7	1.765	V
VSENSE OV Threshold Voltage	Code 0, Ratio = 0.45	3.7	3.763	3.826	V
	Code 0, Ratio = 0.9	3.92	4.025	4.13	V
	Code 15, Ratio = 0.45	2.116	2.15	2.184	V
	Code 15, Ratio = 0.9	1.635	2.3	2.365	V

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise specified, VCC = 12V, VSENSE = 3.5V, $V_{OVTH/UVTH}$ = 1.26V, $V_{D0} = V_{D1} = V_{D2} = V_{D3}$ = 0V, 0°C < T_A < 70°C for the UC3910, –25°C < T_A < 80°C for the UC2910, –55°C < T_A < 125°C for the UC1910 $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Monitor Circuitry (Note 2) (cont.)					
VSENSE OVP Threshold Voltage	Code 0, Ratio = 0.45	3.937	4.025	4.113	V
	Code 0, Ratio = 0.9	4.41	4.55	4.69	V
	Code 15, Ratio = 0.45	2.235	2.3	2.365	V
	Code 15, Ratio = 0.9	2.505	2.6	2.695	V
OV, UV Comparator Hysteresis	Code 0, Ratio = 0.9	70	88	120	mV
	Code 15, Ratio = 0.45	15	25	40	mV
OVP Comparator Hysteresis	Code 0, Ratio = 0.9	160	218	300	mV
	Code 15, Ratio = 0.45	40	62	85	mV
Input Common Mode Range	OV, UV, OVP Comparators	0		5	V
Propagation Delay	OV, UV Comparators			5	µs
	OVP Comparator			5	µs
PWRGOOD, OVP, OVPB Outputs					
PWRGOOD Voltage Low	$I_{PWRGOOD}$ = 10mA			0.4	V
OVP Sourcing Current	V_{OVP} = 1.4V	65			mA
OVPB Voltage Low	I_{OVPB} = 1mA			0.4	V

Note 1: "Line, Load" implies that the parameter is tested at all combinations of the conditions: 10.8V < VCC < 13.2V, –2mA < I_{VREF} < 0mA.

Note 2: These are the actual voltages on VSENSE which will cause the OVPB and PWRGOOD outputs to switch, assuming the DACOUT voltage is perfect. These limits apply for 0°C < T_A < 70°C.

Note 3: "Code 0" means pins D0 - D4 are all low; "Code 15" means they are all floating or high (See Table 1). "Ratio" is the divider ratio of the resistor string between DACBUF and OVTH/UVTH (See Figure 1).

PIN DESCRIPTIONS

D0-D3 (DAC Digital Input Control Codes): These are the DAC digital input control codes, with D0 representing the least significant bit (LSB) and D3, the most significant bit (MSB) (See Table 1). A bit is set low by being connected to GND; a bit is set high by floating it, or connecting it to a 3V to 5V voltage source. Each control pin is pulled up to approximately 4.8V by an internal 40µA current source.

DACBUF (Buffered DACOUT Voltage): This pin provides a buffered version of the DACOUT voltage to allow external programming of the OV/UV thresholds (see OVTH/UVTH below).

DACOUT (Digital-to-Analog Converter Output Voltage): This pin is the output of the 4-bit digital to analog (DAC) converter. Setting all input control codes low produces 3.5V at DACOUT; setting all codes high produces 2.0V at DACOUT. The LSB step size (i.e. resolution) is 100mV (See Table 1). The DACOUT source impedance is typically 3kΩ and must therefore drive a high impedance input. Bypass DACOUT at the driven input with a 0.01µF, low ESR, low ESL capacitor for best circuit noise immunity.

GND (Signal Ground): All voltages are measured with respect to GND. The two GND pins are connected together internally but should also be connected externally using a short PC board trace. Bypass capacitors on the VCC and VREF pins should be connected directly to the ground plane near one of the signal ground

Decimal Code	D3	D2	D1	D0	DACOUT Voltage
15	1	1	1	1	2.0
14	1	1	1	0	2.1
13	1	1	0	1	2.2
12	1	1	0	0	2.3
11	1	0	1	1	2.4
10	1	0	1	0	2.5
9	1	0	0	1	2.6
8	1	0	0	0	2.7
7	0	1	1	1	2.8
6	0	1	1	0	2.9
5	0	1	0	1	3.0
4	0	1	0	0	3.1
3	0	0	1	1	3.2
2	0	0	1	0	3.3
1	0	0	0	1	3.4
0	0	0	0	0	3.5

Table 1. Programming the DACOUT Voltage

PIN DESCRIPTIONS (cont.)

pins.

OVP (Overvoltage Comparator Output): This output pin drives an external SCR circuit with up to 65mA when the voltage on VSENSE rises above its nominal value by a percentage set by the voltage on the OVTH/UVTH pin (see below). The OVP comparator hysteresis is a function of both the DACBUF voltage and the OV/UV percentage programmed.

OVPB (Overvoltage Comparator Complementary Output): This output is a complement to the OVP output (see above) and provides an open collector capable of sinking 1mA when the voltage on VSENSE rises above its nominal value by a percentage set by the voltage on the OVTH/UVTH pin (see below).

OVTH/UVTH (Undervoltage and Lower Overvoltage Threshold Input): This pin is used to program the window thresholds for the OV and UV comparators. The OV-UV window is centered around the DACBUF voltage and can be programmed from ±5% to ±15% about DACBUF. Connect a resistor divider between DACBUF and GND to set the percentage. The threshold for the OVP comparator is internally set to a percentage 2 times larger than the programmed OV percentage; therefore, its range extends from 10% to 30% above DACBUF.

PWRGOOD (Undervoltage/Lower Overvoltage Output): This pin is an open collector output which is driven low to reset the microprocessor when VSENSE rises above or falls below its nominal value by a percentage programmed by OVTH/UVTH. The OV and UV comparators' hysteresis is a function of the DACBUF voltage and the OV/UV programmed percentage.

VCC (Positive Supply Voltage): This pin supplies power to the chip. Connect VCC to a stable voltage source of at least 9V and capable of sourcing at least 15mA. The OVP and PWRGOOD outputs are held low, the OVPB output is in a high impedance state, and the VSENSE pin is pulled low until VCC exceeds the upper undervoltage lockout threshold. This pin should be bypassed directly to the GND pin with a 0.1µF low ESR, low ESL capacitor.

VREF (Voltage Reference Output): This pin provides an accurate 5V reference, capable of delivering up to 10mA to external circuitry, and is internally short circuit current limited. For best reference stability, bypass VREF directly to the GND pin with a 0.1µF, low ESR, low ESL capacitor.

VSENSE (Output Voltage Sensing Input): This pin is the input to the OVP and PWRGOOD comparators and is connected to the system output voltage through a lowpass filter. When choosing the resistor value for this filter, make sure that no more than 500µA will flow

APPLICATION INFORMATION

The Overvoltage (OV), Undervoltage (UV) and Overvoltage Protection Voltage (OVP) threshold detection voltages are programmed as a percentage about the nominal DAC output voltage, DACOUT. Figure 1 illustrates how to program the UC3910 by setting a voltage divider, R_{DIV}, at the OVTH/UVTH pin. The voltage divider ratio is defined as

$$R_{DIV} = \frac{RS1}{RS1 + RS2}$$

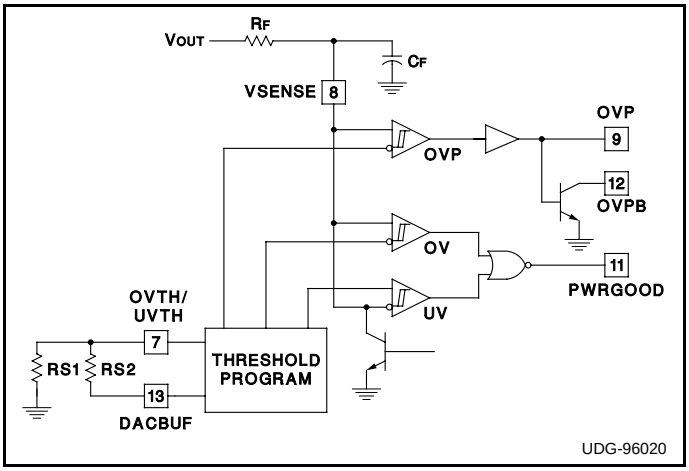


Figure 1. Setting the OV/UV/OVP Threshold Percentages

The UC3910 allows a ratio R_{DIV} at the OVTH/UVTH pin from 0.3 to 0.9, which corresponds to overvoltage and undervoltage percentage thresholds from 5% to 15% and an OVP percentage threshold from 10% to 30%. These thresholds are shown in Figure 2.

The OV, UV and OVP percentage thresholds are given by

$$\%V_{OV} = R_{DIV} \bullet 16.7$$
$$\%V_{UV} = -(R_{DIV} \bullet 16.7)$$
$$\%V_{OVP} = \%V_{OV} \bullet 2.0 = R_{DIV} \bullet 33.4$$

An R-C filter is added to the VSENSE pin to filter noise and ripple at the comparator inputs. An R-C filter frequency of $F_{SWITCH}/10$ is recommended. Choose the

APPLICATION INFORMATION (cont.)

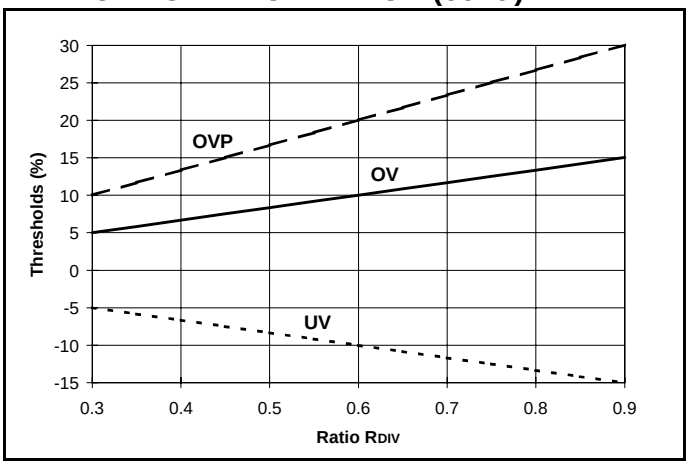


Figure 2. OV, UV and OVP Percentage Thresholds as a Function of the Divider Ratio RDIV

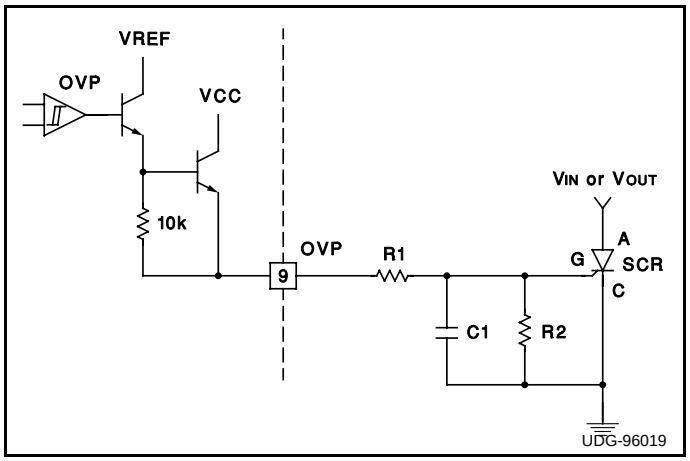


Figure 3. Driving and SCR Using the UC3910 OVP Signal

value of RF such that it limits the current into VSENSE to ≤ 0.5mA.

$$R_F \bullet C_F = \frac{1}{2 \bullet \pi \bullet \left(\frac{F_{SWITCH}}{10}\right)}$$

$$R_F \geq \frac{V_{OUT}}{0.5mA}$$

The Overvoltage Protection output, OVP, can be used to directly drive a crowbarring SCR, as shown in Figure 3.

A typical application is shown in Figure 4 using the UC3910 together with the UC3886 Average Current Mode PWM Controller IC for a power supply to drive Intel's Pentium®Pro processor.

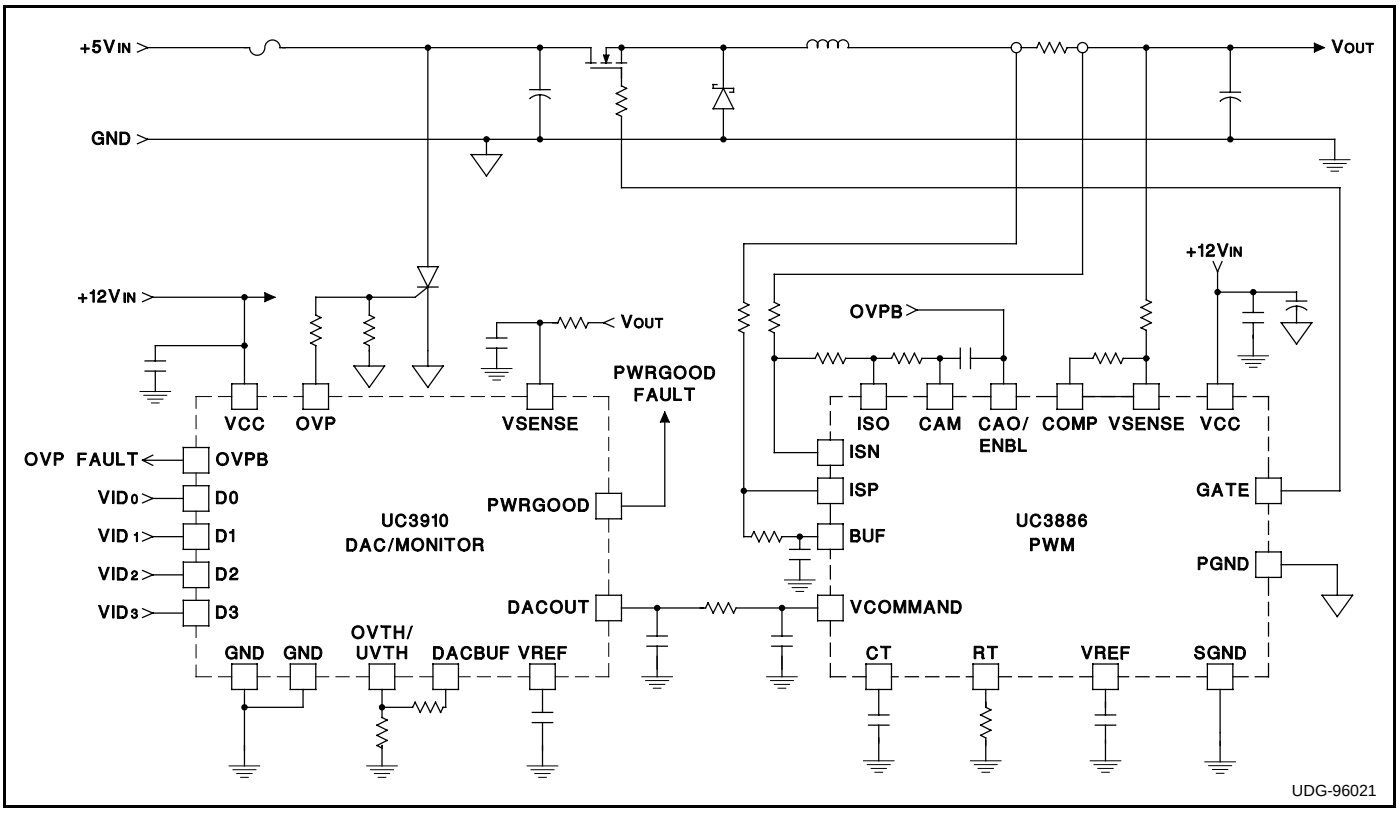


Figure 4. UC3910 Configured with the UC3886 for a Pentium® Pro DC/DC Converter

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UC3910D	NRND	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3910DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3910DTR	NRND	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3910DTRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3910N	NRND	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-NC-NC-NC
UC3910NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-NC-NC-NC

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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