



MOTOROLA
Semiconductors

BOX 20912 • PHOENIX, ARIZONA 85036

MC14011
MC14011B

QUAD 2-INPUT "NAND" GATE

The MC14011 and MC14011B are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14011B only)
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14011B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4011A and CD4011B

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to $V_{DD} + 0.5$	Vdc
DC Current Drain per Pin	I	10	mA dc
Operating Temperature Range	T_A	-55 to +125	°C
	CL/CP Device	-40 to +85	
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001 data sheet for complete characteristics for the non-B device.

See the MC14001B data sheet for complete characteristics of the B-Series device.

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NAND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632



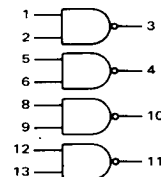
P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB	Suffix	Denotes
	L	Ceramic Package
	P	Plastic Package
	A	Extended Operating Temperature Range
	C	Limited Operating Temperature Range

Delete for Non-B Device

LOGIC DIAGRAM



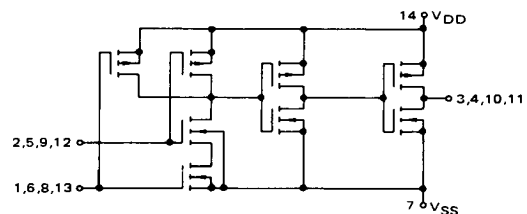
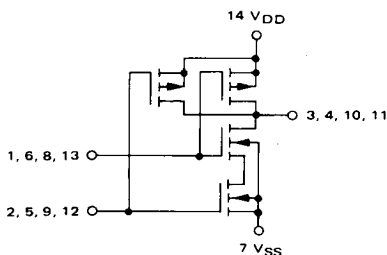
V_{DD} = Pin 14
 V_{SS} = Pin 7

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MC14011

CIRCUIT SCHEMATICS
(1/4 of Device Shown)

MC14011B



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper

operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).