



# CYPRESS

## CY29940

2.5V or 3.3V, 200-MHz, 1:18 Clock Distribution Buffer

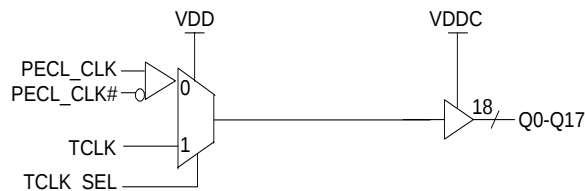
### Features

- 200-MHz clock support
- LVPECL or LVCMOS/LVTTL clock input
- LVCMOS/LVTTL compatible inputs
- 18 clock outputs: drive up to 36 clock lines
- 150 ps max. output-to-output skew
- Dual or single supply operation:
  - 3.3V core and 3.3V outputs
  - 3.3V core and 2.5V outputs
  - 2.5V core and 2.5V outputs
- Pin compatible with MPC940L, MPC9109
- Available in Commercial and Industrial temperature
- 32-pin LQFP package

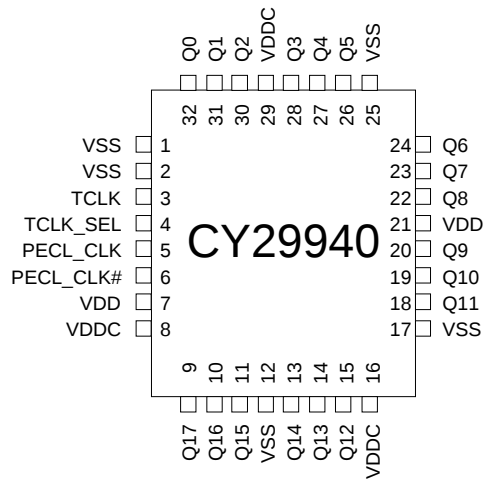
### Description

The CY29940 is a low-voltage 200-MHz clock distribution buffer with the capability to select either a differential LVPECL or a LVCMOS/LVTTL compatible input clock. The two clock sources can be used to provide for a test clock as well as the primary system clock. All other control inputs are LVCMOS/LVTTL compatible. The eighteen outputs are 2.5V or 3.3V LVCMOS/LVTTL compatible and can drive 50Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:36. Low output-to-output skews make the CY29940 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

### Block Diagram



### Pin Configuration



**Pin Description<sup>[1]</sup>**

| Pin                                                                               | Name      | PWR  | I/O   | Description                                                                                 |
|-----------------------------------------------------------------------------------|-----------|------|-------|---------------------------------------------------------------------------------------------|
| 5                                                                                 | PECL_CLK  |      | I, PU | PECL Input Clock                                                                            |
| 6                                                                                 | PECL_CLK# |      | I, PD | PECL Input Clock                                                                            |
| 3                                                                                 | TCLK      |      | I, PD | External Reference/Test Clock Input                                                         |
| 9, 10, 11, 13,<br>14, 15, 18, 19,<br>20, 22, 23, 24,<br>26, 27, 28, 30,<br>31, 32 | Q(17:0)   | VDDC | O     | Clock Outputs                                                                               |
| 4                                                                                 | TCLK_SEL  |      | I, PD | <b>Clock Select Input.</b> When LOW, PECL clock is selected and when HIGH TCLK is selected. |
| 8, 16, 29                                                                         | VDDC      |      |       | <b>3.3V or 2.5V Power Supply for Output Clock Buffers</b>                                   |
| 7, 21                                                                             | VDD       |      |       | <b>3.3V or 2.5V Power Supply</b>                                                            |
| 1, 2, 12, 17,<br>25                                                               | VSS       |      |       | <b>Common Ground</b>                                                                        |

**Note:**

1. PD = Internal Pull-Down, PU = Internal Pull-up.

## Maximum Ratings<sup>[2]</sup>

Maximum Input Voltage Relative to  $V_{SS}$ : .....  $V_{SS} - 0.3V$   
 Maximum Input Voltage Relative to  $V_{DD}$ : .....  $V_{DD} + 0.3V$   
 Storage Temperature: .....  $-65^{\circ}C$  to  $+150^{\circ}C$   
 Operating Temperature: .....  $-40^{\circ}C$  to  $+85^{\circ}C$   
 Maximum ESD Protection..... 2 kV  
 Maximum Power Supply: ..... 5.5V  
 Maximum Input Current: .....  $\pm 20$  mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{SS}$  or  $V_{DD}$ ).

**DC Parameters:**  $V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{DDC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$

| Parameter | Description                                  | Conditions                                      | Min.           | Typ. | Max.           | Unit.    |
|-----------|----------------------------------------------|-------------------------------------------------|----------------|------|----------------|----------|
| $V_{IL}$  | Input Low Voltage                            |                                                 | $V_{SS}$       |      | 0.8            | V        |
| $V_{IH}$  | Input High Voltage                           |                                                 | 2.0            |      | $V_{DD}$       | V        |
| $I_{IL}$  | Input Low Current <sup>[3]</sup>             |                                                 |                |      | -200           | $\mu A$  |
| $I_{IH}$  | Input High Current <sup>[3]</sup>            |                                                 |                |      | 200            | $\mu A$  |
| $V_{PP}$  | Peak-to-Peak Input Voltage<br>PECL_CLK       |                                                 | 500            |      | 1000           | mV       |
| $V_{CMR}$ | Common Mode Range <sup>[4]</sup><br>PECL_CLK | $V_{DD} = 3.3V$                                 | $V_{DD} - 1.4$ |      | $V_{DD} - 0.6$ | V        |
|           |                                              | $V_{DD} = 2.5V$                                 | $V_{DD} - 1.0$ |      | $V_{DD} - 0.6$ | V        |
| $V_{OL}$  | Output Low Voltage <sup>[5, 6, 7]</sup>      | $I_{OL} = 20$ mA                                |                |      | 0.5            | V        |
| $V_{OH}$  | Output High Voltage <sup>[5, 6, 7]</sup>     | $I_{OH} = -20$ mA, $V_{DDC} = 3.3V$             | 2.4            |      |                | V        |
|           |                                              | $I_{OH} = -20$ mA, $V_{DDC} = 2.5V$             | 1.8            |      |                | V        |
| $I_{DDQ}$ | Quiescent Supply Current                     |                                                 |                | 5    | 7              | mA       |
| $I_{DD}$  | Dynamic Supply Current                       | $V_{DD} = 3.3V$ , Outputs @ 150 MHz, $CL=15$ pF |                | 285  |                | mA       |
|           |                                              | $V_{DD} = 3.3V$ , Outputs @ 200 MHz, $CL=15$ pF |                | 335  |                |          |
|           |                                              | $V_{DD} = 2.5V$ , Outputs @ 150 MHz, $CL=15$ pF |                | 200  |                |          |
|           |                                              | $V_{DD} = 2.5V$ , Outputs @ 200 MHz, $CL=15$ pF |                | 240  |                |          |
| $Z_{out}$ | Output Impedance                             | $V_{DD} = 3.3V$                                 | 8              | 12   | 16             | $\Omega$ |
|           |                                              | $V_{DD} = 2.5V$                                 | 10             | 15   | 20             |          |
| $C_{in}$  | Input Capacitance                            |                                                 |                | 4    |                | pF       |

### Notes:

- Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
- Inputs have pull-up/pull-down resistors that effect input current.
- The  $V_{CMR}$  is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "High" input is within the  $V_{CMR}$  range and the input lies within the  $V_{PP}$  specification. Driving series or parallel terminated 50 $\Omega$  (or 50 $\Omega$  to  $V_{DD}/2$ ) transmission lines
- Outputs driving 50 $\Omega$  transmission lines.
- See Figure 1 & 2.
- 50% input duty cycle.

**AC Parameters**<sup>[8]</sup>:  $V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{DDC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ 

| Parameter      | Description                                              | Conditions                        | Min.      | Typ. | Max. | Units |
|----------------|----------------------------------------------------------|-----------------------------------|-----------|------|------|-------|
| $F_{max}$      | Input Frequency                                          |                                   |           |      | 200  | MHz   |
| $t_{PD}$       | PECL_CLK to Q Delay <sup>[5, 6, 11]</sup><br></ =150 MHz | $V_{DD} = 3.3V$<br>85°C           | $t_{PHL}$ | 2.0  | 3.2  | ns    |
|                |                                                          |                                   | $t_{PLH}$ | 2.1  | 3.4  |       |
|                |                                                          | $V_{DD} = 3.3V$<br>70°C           | $t_{PHL}$ | 1.9  | 3.1  |       |
|                |                                                          |                                   | $t_{PLH}$ | 2.0  | 3.2  |       |
|                |                                                          | $V_{DD} = 2.5V$<br>85°C           | $t_{PHL}$ | 2.5  | 5.2  |       |
|                |                                                          |                                   | $t_{PLH}$ | 2.6  | 5    |       |
| $t_{PD}$       | LVCMOS to Q Delay <sup>[5, 6, 11]</sup><br></ =150 MHz   | $V_{DD} = 3.3V$<br>85°C           | $t_{PHL}$ | 1.9  | 3    | ns    |
|                |                                                          |                                   | $t_{PLH}$ | 2.0  | 3.2  |       |
|                |                                                          | $V_{DD} = 3.3V$<br>70°C           | $t_{PHL}$ | 1.8  | 2.9  |       |
|                |                                                          |                                   | $t_{PLH}$ | 1.8  | 3.1  |       |
|                |                                                          | $V_{DD} = 2.5V$<br>85°C           | $t_{PHL}$ | 2.5  | 4    |       |
|                |                                                          |                                   | $t_{PLH}$ | 2.5  | 4    |       |
| $t_{PD}$       |                                                          | $V_{DD} = 2.5V$<br>70°C           | $t_{PHL}$ | 2.3  | 3.8  |       |
|                |                                                          |                                   | $t_{PLH}$ | 2.3  | 3.8  |       |
| $t_j$          | Total Jitter                                             | $V_{DD} = 3.3V @ 150MHz$          |           |      | 10   | ps    |
| $F_{outDC}$    | Output Duty Cycle <sup>[5, 6, 7]</sup>                   | $F_{CLK} < 134 MHz$               | 45        |      | 55   | %     |
|                |                                                          | $F_{CLK} > 134 MHz$               | 40        |      | 60   |       |
| $T_{skew}$     | Output-to-Output Skew <sup>[5, 6]</sup>                  | $V_{DD} = 3.3V$                   |           |      | 150  | ps    |
|                |                                                          | $V_{DD} = 2.5V$                   |           |      | 200  |       |
| $T_{skew(pp)}$ | Part-to-Part Skew <sup>[9]</sup>                         | PECL, $V_{DDC} = 3.3V$            |           |      | 1.4  | ns    |
|                |                                                          | PECL, $V_{DDC} = 2.5V$            |           |      | 2.2  |       |
| $T_{skew(pp)}$ | Part-to-Part Skew <sup>[9]</sup>                         | TCLK, $V_{DDC} = 3.3V$            |           |      | 1.2  | ns    |
|                |                                                          | TCLK, $V_{DDC} = 2.5V$            |           |      | 1.7  |       |
| $T_{skew(pp)}$ | Part to Part Skew <sup>[10]</sup>                        | PECL_CLK                          |           |      | 850  | ps    |
|                |                                                          | TCLK                              |           |      | 750  |       |
| $t_R/t_F$      | Output Clocks Rise/Fall Time <sup>[5, 6]</sup>           | 0.7V to 2.0V,<br>$V_{DDC} = 3.3V$ | 0.3       |      | 1.1  | ns    |
|                |                                                          | 0.5V to 1.8V,<br>$V_{DDC} = 2.5V$ | 0.3       |      | 1.2  |       |

**Notes:**

8. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
9. Across temperature and voltage ranges, includes output skew.
10. For a specific temperature and voltage, includes output skew
11. Parameters tested @ 150 MHz.

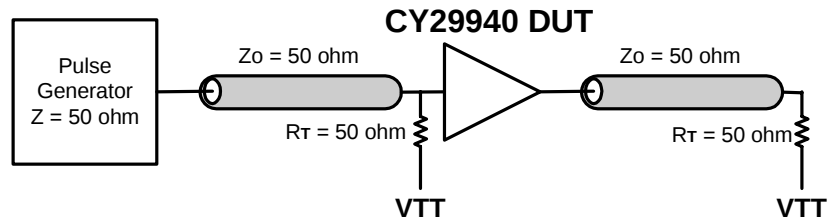


Figure 1. LVCMOS\_CLK CY29940 Test Reference for  $V_{CC} = 3.3V$  and  $V_{CC} = 2.5V$

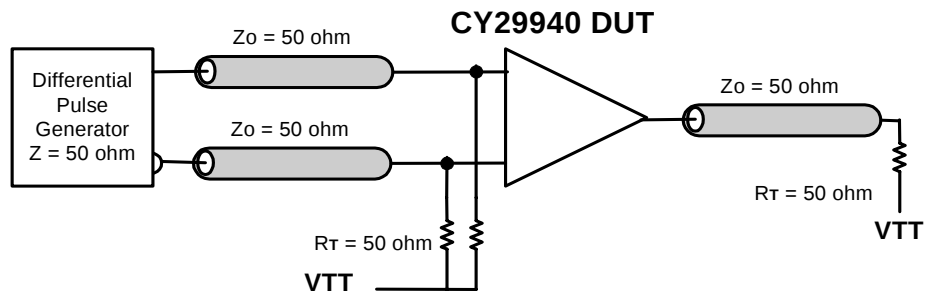


Figure 2. PECL\_CLK CY29940 Test Reference for  $V_{CC} = 3.3V$  and  $V_{CC} = 2.5V$

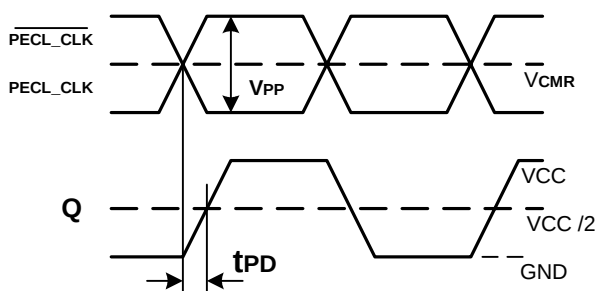


Figure 3. Propagation Delay (TPD) Test Reference

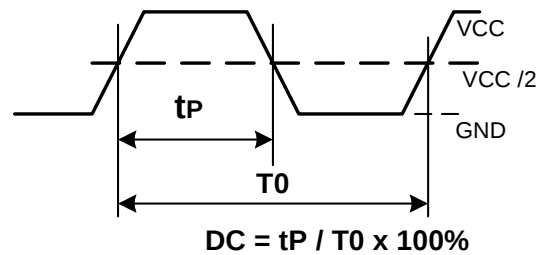


Figure 5. Output Duty Cycle (FoutDC)

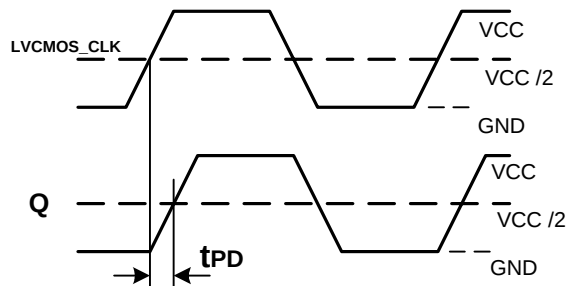


Figure 4. LVCMOS Propagation Delay (TPD) Test Reference

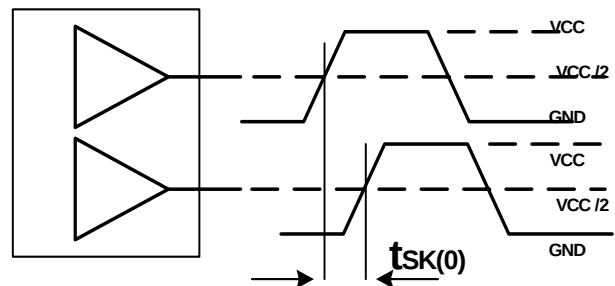


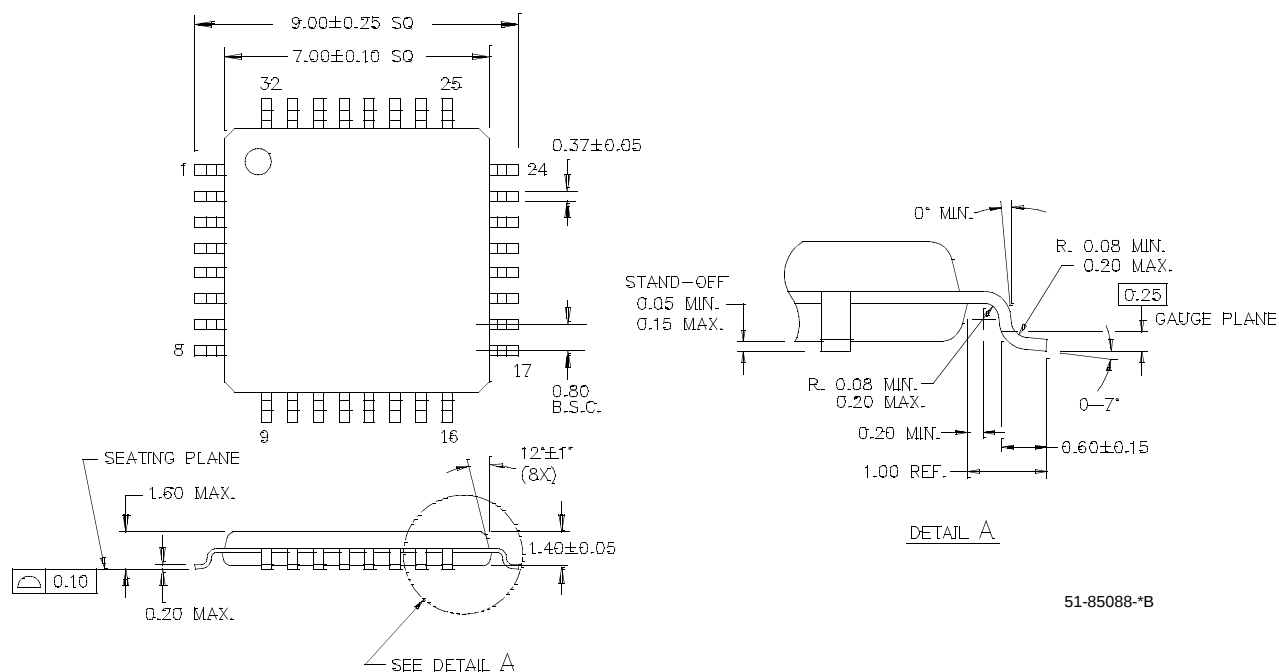
Figure 6. Output-to-Output Skew  $t_{sk}(0)$

## Ordering Information

| Part Number | Package Type                | Production Flow            |
|-------------|-----------------------------|----------------------------|
| CY29940AI   | 32 Pin LQFP                 | Industrial, -40°C to +85°C |
| CY29940AIT  | 32 Pin LQFP – Tape and Reel | Industrial, -40°C to +85°C |
| CY29940AC   | 32 Pin LQFP                 | Commercial, 0°C to 70°C    |
| CY29940ACT  | 32 Pin LQFP – Tape and Reel | Commercial, 0°C to 70°C    |

## Package Drawing and Dimensions

### 32-Lead Thin Plastic Quad Flatpack 7 x 7 x 1.4 mm A32.14



| Document Title: CY29940 2.5V or 3.3V, 200-MHz, 1:18 Clock Distribution Buffer<br>Document Number: 38-07283 |         |            |                 |                                                                                                                                                                                                                           |
|------------------------------------------------------------------------------------------------------------|---------|------------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| REV.                                                                                                       | ECN NO. | Issue Date | Orig. of Change | Description of Change                                                                                                                                                                                                     |
| **                                                                                                         | 111094  | 02/01/02   | BRK             | New data sheet                                                                                                                                                                                                            |
| *A                                                                                                         | 116776  | 08/15/02   | HWT             | Incorporate results of final characterization using corporate methods, added output impedance on page 3 and added output duty cycle on page 4.<br>Add commercial temperature range in the ordering information on page 6. |
| *B                                                                                                         | 122875  | 12/21/02   | RBI             | Add power up requirements to maximum rating information                                                                                                                                                                   |