Asynchronous Clear

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
′164	36 MHz	21 mW per bit
'LS164	36 MHz	10 mW per bit

#### description

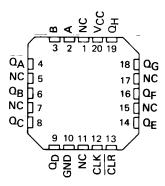
These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup-time requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

The SN54164 and SN54LS164 are characterized for operation over the full military temperature range of  $-55\,^{\circ}\text{C}$  to 125 $\,^{\circ}\text{C}$ . The SN74164 and SN74LS164 are characterized for operation from 0 $\,^{\circ}\text{C}$  to 70 $\,^{\circ}\text{C}$ .

SN54164, SN54LS164...J OR W PACKAGE SN74164...N PACKAGE SN74LS164...D OR N PACKAGE (TOP VIEW)

ΑC	1	U 14	vcc
в□	2	13	⊒αн
$a_A \Box$	3	12	$\Box a_{G}$
$\alpha_{B} \square$	4	11	ΩF
$a_{C} \square$	5	10	ΩE
$\sigma_{D} \square$	6	9	CLR
GND [	7	8	CLK
	_		

## SN54LS164 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

#### **FUNCTION TABLE**

L		OUTP	UTS			
CLEAR	CLOCK	Α	В	$\alpha_{A}$	αB	Q <sub>H</sub>
L	X	Х	Х	L	L	L
Н	L	×	Х	Q <sub>A0</sub>	$o_{B0}$	$\alpha_{H0}$
Н	1	н	Н	Н	$Q_{An}$	$Q_{Gn}$
н	1	L	X	L	$\mathbf{Q}_{An}$	$Q_{Gn}$
Н	1	Х	L	L	QAn	$Q_{Gn}$

H = high level (steady state), L = low level (steady state)

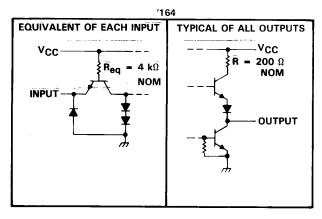
X = irrelevant (any input, including transitions)

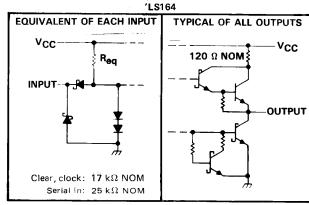
↑ = transition from low to high level.

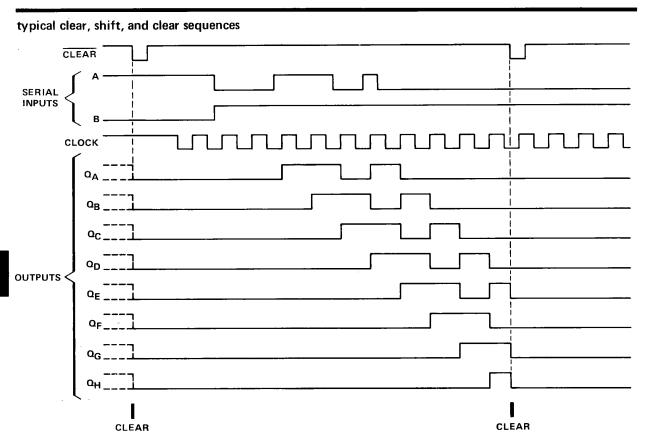
 ${
m Q}_{A0},\,{
m Q}_{B0},\,{
m Q}_{H0}$  = the level of  ${
m Q}_A,\,{
m Q}_B,\,{
m or}\,\,{
m Q}_H,$  respectively, before the indicated steady-state input conditions were established.

 ${\bf Q}_{An},\,{\bf Q}_{Gn}$  = the level of  ${\bf Q}_A$  or  ${\bf Q}_G$  before the most-recent  $\uparrow$  transition of the clock; indicates a one-bit shift.

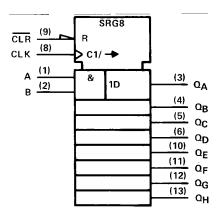
#### schematics of inputs and outputs





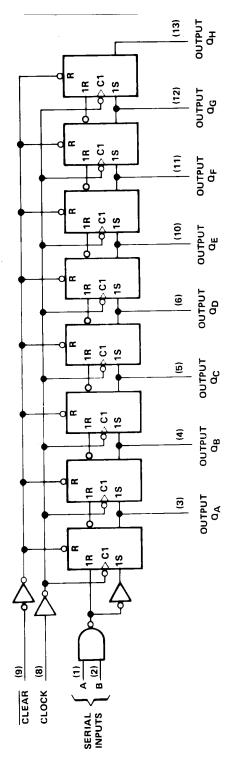


logic symbol†



 $<sup>^{\</sup>dagger}$ This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

## logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

## SN54164, SN74164 **8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS**

absolute maximum ratings over oprating free-air temperature range (unless otherwise noted)									
Input voltage	SN54164SN74164	-55°C to 125°C 0°C to 70°C							

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

		SN54164			SN74164			
	MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Supply voltage, VCC	4.5	5	5.5	4.75	5	5.25	V	
High-level output current, IOH			-400			-400	μΑ	
Low-level output current, IQL			8			8	mA	
Clock frequency, f <sub>clock</sub>	0		25	0		25	MHz	
Width of clock or clear input pulse, tw	20			20			ns	
Data setup time, t <sub>SU</sub> (see Figure 1)	15			15			ns	
Data setup time, t <sub>SU</sub> (Clear Inactive) (see Figure 1)	20			20			ns	
Data hold time, th (see Figure 1)	5			5			ns	
Operating free-air temperature, TA	- 55		125	0		70	°C	

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN5416	4	;	דומט		
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage			2			2			٧
VIL	Low-level input voltage					8.0			8.0	V .
VIK	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA	\ \ \		-	-1.5			-1.5	V
Voн	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> =400	μA	2.4	3.2		2.4	3.2		>
VOL	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 8 mA			0.2	0.4		0.2	0.4	V
<u> </u>	Input current at maximum input voltage	$V_{CC} = MAX, V_1 = 5.5 V,$				1			1	mA
T <sub>IH</sub>	High-level input current	$V_{CC} = MAX, V_1 = 2.4 V$				40			40	μA
111	Low-level input current	$V_{CC} = MAX$ , $V_I = 0.4 V$				-1.6			-1.6	mA
los	Short-circuit output current §	V <sub>CC</sub> = MAX		-10		-27.5	-9		-27.5	mA
F 33		V <sub>CC</sub> = MAX, V <sub>I(clock)</sub> =	0.4 V		30			30		mA
<sup>1</sup> CC	Supply current	See Note 2 V <sub>I(clock)</sub> =	2.4 V		37	54		37	54	]'''^

<sup>†</sup> For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: ICC is measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5 V, applied to clear.

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ} \text{ C}$

	PARAMETER	TEST CONDIT	IONS	MIN	TYP	MAX	UNIT
f <sub>max</sub>	Maximum clock frequency		C <sub>L</sub> = 15 pF	25	36		MHz
	Propagation delay time, high-to-low-level	1 i	C <sub>L</sub> = 15 pF		24	36	ns
<sup>t</sup> PHL	Q outputs from clear input	B 500 G	C <sub>L</sub> = 50 pF		28	42	1
	Propagation delay time, low-to-high-level	R <sub>L</sub> = 800 Ω, See Figure 1	C <sub>L</sub> = 15 pF	8	17	27	ns
<sup>t</sup> PLH	Q outputs from clock input		C <sub>L</sub> = 50 pF	10	20	30	] ""
	Propagation delay time, high-to-low-level		C <sub>L</sub> = 15 pF	10	21	32	ns
tPHL			C <sub>L</sub> = 50 pF	10	25	37	]



<sup>‡</sup> All typical values are at  $V_{CC}$  = 5 V,  $T_A$  = 25°C.

<sup>§</sup> Not more than two outputs should be shorted at a time.

## SN54LS164, SN74LS164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless other	rwise noted)
Supply voltage, VCC (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS164	-55°C to 125°C
SN74LS164	0°C to 70°C
Storage temperature range	$-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$
NOTE 1: Voltage values are with respect to network ground terminal.	

#### g.v.

#### recommended operating conditions

		S	SN54LS164			SN74LS164			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	٧	
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			0.8	V	
ЮН	High-level output current			<b>- 0.4</b>			- 0.4	mA	
loL	Low-level output current			4			8	mA	
fclock	Clock frequency	0		25	0		25	MHz	
tw	Width of clock or clear input pulse	20			20			ns	
t <sub>su</sub>	Data setup time (See Figure 1)	15			15			ns	
t <sub>su</sub>	Clear inactive setup time (See Figure 1)	20			20		_	ns	
th	Data hold time (See Figure 1)	5			5			ns	
TA	Operating free-air temperature	- 55		125	0		70	°C	

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

24244552	TEST CONDITIONS!	TEST COMPLETIONS T		SN54LS164			SN74LS164			
PARAMETER	TEST CONDITIONS†		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	UNIT	
VIK	$V_{CC} = MIN$ , $I_I = -18 \text{ mA}$	·			- 1.5			<b>- 1</b> .5	V	
V <sub>OH</sub>	$V_{CC} = MIN$ , $V_{IH} = 2 V$ , $V_{II}$ $I_{OH} = -0.4 \text{ mA}$	L = MAX,	2.5	3.5		2.7	3.5		>	
	$V_{CC} = MIN$ , $V_{IH} = 2 V$ ,	I <sub>OL</sub> = 4 mA		0.25	0.4		0.25	0.4	V	
$v_{OL}$	V <sub>IL</sub> = MAX	I <sub>OL</sub> = 8 mA					0.35	0.5	\	
l <sub>l</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V				0.1			0.1	mA	
IHI.	$V_{CC} = MAX$ , $V_I = 2.7 V$			20			20		μΑ	
ΙΙL	$V_{CC} = MAX$ , $V_I = 0.4 V$				-0.4			-0.4	mA	
los	V <sub>CC</sub> = MAX		- 20		- 100	- 20		- 100	mA	
lcc	V <sub>CC</sub> = MAX, See Note 3	_		16	27		16	27	mA	

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

#### switching characteristics, VCC = 5 V, TA = 25°C

	PARAMETER	TEST CONDITIONS MIN TYP N		MAX	UNIT	
fmax	Maximum clock frequency		25	36		MHz
tPHL	Propagation delay time, high-to-low-level Q outputs from clear input	$R_L = 2 k\Omega$ , $C_L = 15 pF$ ,		24	36	ns
tPLH	Propagation delay time, low-to-high-level Q outputs from clock input	See Figure 1		17	27	ns
tPHL	Propagation delay time, high-to-low-level Q outputs from clock input			21	32	ns



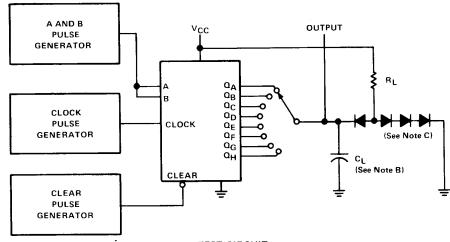
 $<sup>^{\</sup>ddagger}$ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25 °C.

<sup>&</sup>lt;sup>5</sup>Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

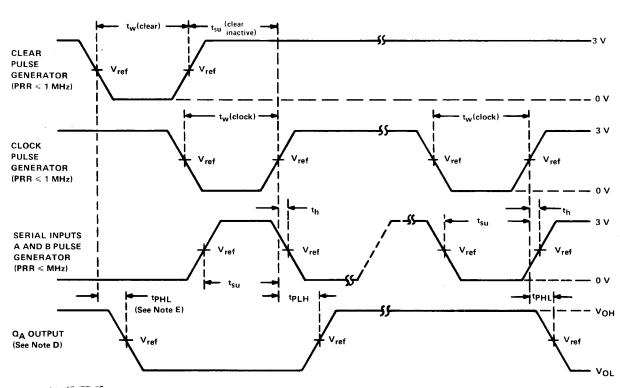
NOTE 3: I<sub>CC</sub> is measured with outputs open, serial inputs grounded, the clock input at 2.4 V, and a momentary ground, then 4.5 V applied to clear.

## SN54164, SN54LS164, SN74164, SN74LS164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

## PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



#### **VOLTAGE WAVEFORMS**

- NOTES: A. The pulse generators have the following characteristics: duty cycle  $\leq$  50%,  $Z_{out} \approx$  50  $\Omega$ ; for '164,  $t_r \leq$  10 ns,  $t_f \leq$  10 ns, and for LS164,  $t_r \leq$  15 ns,  $t_f \leq$  6 ns.
  - B. C<sub>L</sub> includes probe and jig capacitance.
  - C. All diodes are 1N3064 or equivalent.
  - D. QA output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
  - E. Outputs are set to the high level prior to the measurement of tpHL from the clear input.
  - F. For '164,  $V_{ref} = 1.5 \text{ V}$ ; for 'LS164,  $V_{ref} = 1.3 \text{ V}$ .

FIGURE 1-SWITCHING TIMES



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