

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for CDMA base station applications with frequencies from 1880 to 2025 MHz and GSM EDGE base station applications with frequencies from 1805 to 1880 MHz. Can be used in Class AB and Class C for all typical cellular base station modulation formats.

- Typical Doherty Single-Carrier W-CDMA Performance: $V_{DD} = 28$ Volts, $I_{DQA} = 400$ mA, $V_{GSB} = 1.3$ Vdc, $P_{out} = 20$ Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2025 MHz	16.0	44.3	7.8	-33.5

1880 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: $V_{DD} = 28$ Volts, $I_{DQA} = 400$ mA, $V_{GSB} = 1.3$ Vdc, $P_{out} = 20$ Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
1880 MHz	16.2	43.5	7.6	-30.8
1900 MHz	16.1	43.4	7.6	-32.6
1920 MHz	15.8	42.9	7.6	-34.6

GSM EDGE

- Typical GSM EDGE Performance: $V_{DD} = 28$ Volts, $I_{DQA} = I_{DQB} = 330$ mA, $P_{out} = 42$ Watts Avg.

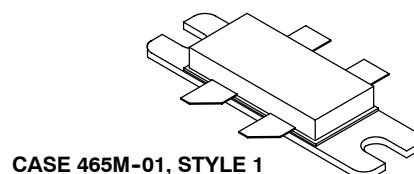
Frequency	G_{ps} (dB)	η_D (%)	SR1 @ 400 kHz (dBc)	SR2 @ 600 kHz (dBc)	EVM (% rms)
1805 MHz	17.1	43.8	-58.4	-74.4	3.0
1840 MHz	17.3	42.4	-60.0	-75.5	2.6
1880 MHz	17.1	41.7	-60.5	-75.3	2.4

Features

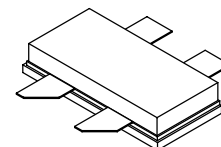
- Production Tested in a Symmetrical Doherty Configuration
- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

MRF8P20100HR3
MRF8P20100HSR3

1805-2025 MHz, 20 W AVG., 28 V
SINGLE W-CDMA
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465M-01, STYLE 1
NI-780-4
MRF8P20100HR3



CASE 465H-02, STYLE 1
NI-780S-4
MRF8P20100HSR3

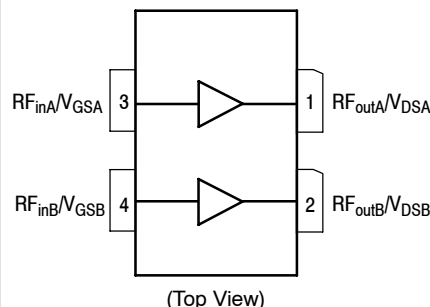


Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C
EDGE Operation @ $T_C = 25^\circ\text{C}$ (1) Derate above 25°C	EDGE	120 0.6	W (PEP) W (PEP)/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 74°C , 20 W CW, 2025 MHz 28 Vdc, $I_{DQA} = 400\text{ mA}$ 28 Vdc, $V_{GSB} = 1.3\text{ Vdc}$ Case Temperature 80°C , 42 W CW, 1805 MHz 28 Vdc, $I_{DQA} = I_{DQB} = 330\text{ mA}$	$R_{\theta JC}$	0.88 0.88 0.59	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2 (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc
On Characteristics (4)					
Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 75\text{ }\mu\text{Adc}$)	$V_{GS(th)}$	1.2	1.9	2.7	Vdc
Gate Quiescent Voltage ($V_{DD} = 28\text{ Vdc}$, $I_{DA} = 400\text{ mAdc}$, Measured in Functional Test)	$V_{GS(Q)}$	2.0	2.7	3.5	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 1\text{ Adc}$)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.
4. Each side of device measured separately.

(continued)

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests ^(1,2) (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQA} = 400\text{ mA}$, $V_{GSB} = 1.3\text{ Vdc}$, $P_{out} = 20\text{ W Avg.}$, $f = 2025\text{ MHz}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.					
Power Gain	G_{ps}	15.0	16.0	18.0	dB
Drain Efficiency	η_D	42.0	44.3	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.2	7.8	—	dB
Adjacent Channel Power Ratio	ACPR	—	-33.5	-31.0	dBc

Typical Performance ⁽²⁾ (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQA} = 400\text{ mA}$, $V_{GSB} = 1.3\text{ Vdc}$, 2010–2025 MHz Bandwidth

P_{out} @ 1 dB Compression Point, CW	P1dB	—	78	—	W
P_{out} @ 3 dB Compression Point, CW	P3dB	—	126	—	W
IMD Symmetry @ 20 W PEP, P_{out} where IMD Third Order Intermodulation $\cong 30\text{ dBc}$ (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD _{sym}	—	46	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW _{res}	—	53	—	MHz
Gain Flatness in 15 MHz Bandwidth @ $P_{out} = 20\text{ W Avg.}$	G_F	—	0.1	—	dB
Gain Variation over Temperature (-30°C to $+85^\circ\text{C}$)	ΔG	—	0.013	—	dB/ $^\circ\text{C}$
Output Power Variation over Temperature (-30°C to $+85^\circ\text{C}$)	ΔP_{1dB}	—	0.004	—	dBm/ $^\circ\text{C}$

Typical Broadband Performance — 1880 MHz ⁽²⁾ (In Freescale 1880 MHz Doherty Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQA} = 400\text{ mA}$, $V_{GSB} = 1.3\text{ Vdc}$, $P_{out} = 20\text{ W Avg.}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
1880 MHz	16.2	43.5	7.6	-30.8
1900 MHz	16.1	43.4	7.6	-32.6
1920 MHz	15.8	42.9	7.6	-34.6

Typical GSM EDGE Performance ⁽³⁾ (In Freescale Class AB Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Volts}$, $I_{DQA} = I_{DQB} = 330\text{ mA}$, $P_{out} = 42\text{ Watts Avg.}$, 1805–1880 MHz EDGE Modulation

Frequency	G_{ps} (dB)	η_D (%)	SR1 @ 400 kHz (dBc)	SR2 @ 600 kHz (dBc)	EVM (% rms)
1805 MHz	17.1	43.8	-58.4	-74.4	3.0
1840 MHz	17.3	42.4	-60.0	-75.5	2.6
1880 MHz	17.1	41.7	-60.5	-75.3	2.4

1. Part internally matched both on input and output.
2. Measurement made with device in a Symmetrical Doherty configuration.
3. Measurement made with device in quadrature combined configuration.

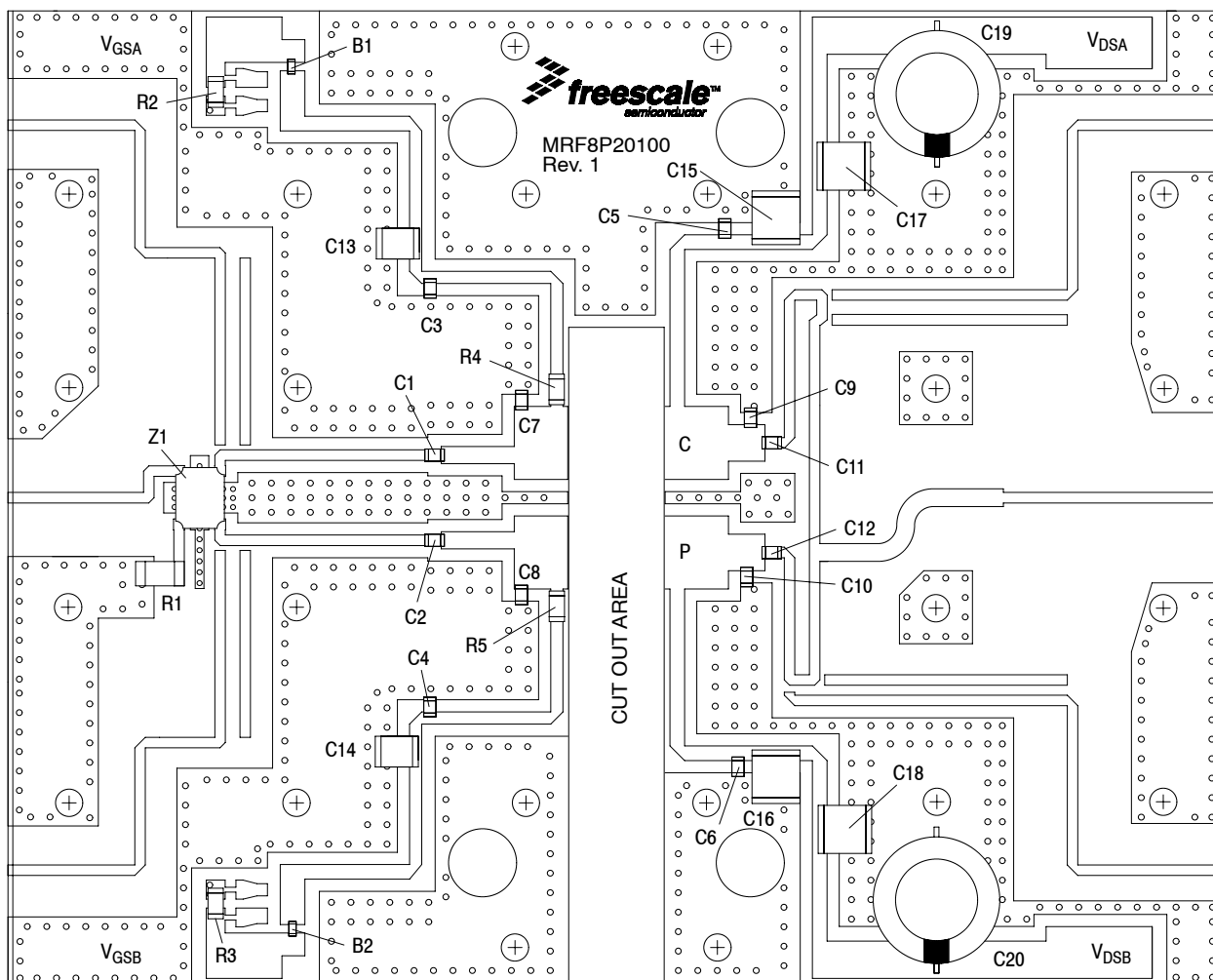


Figure 2. MRF8P20100HR3(HSR3) Test Circuit Component Layout

Table 5. MRF8P20100HR3(HSR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1, B2	RF Ferrite Beads	MPZ2012S300AT000	TDK
C1, C2, C3, C4, C5, C6	15 pF Chip Capacitors	ATC600F150JT250XT	ATC
C7, C8	0.3 pF Chip Capacitors	ATC600F0R3BT250XT	ATC
C9, C10	1.2 pF Chip Capacitors	ATC600F1R2BT250XT	ATC
C11, C12	10 pF Chip Capacitors	ATC600F100JT250XT	ATC
C13, C14	4.7 μ F, 50 V Chip Capacitors	C4532X5R1H475MT	TDK
C15, C16	10 μ F, 50 V Chip Capacitors	C5750X7R1H106KT	TDK
C17, C18	22 μ F, 50 V Chip Capacitors	C5750KF1H226ZT	TDK
C19, C20	220 μ F, 63 V Electrolytic Capacitors	MCGPR63V227M10X21	Multicomp
R1	50 Ω , 4 W Chip Resistor	ATCCW12010T0050GBK	ATC
R2, R3	10 K Ω , 1/4 W Chip Resistors	CRCW120612R0FKEA	Vishay
R4, R5	12 Ω , 1/4 W Chip Resistors	CRCW120612R0FKEA	Vishay
Z1	1900 MHz Band 90°, 3 dB Chip Hybrid Coupler	1P503S	Anaren
PCB	0.020", $\epsilon_r = 3.5$	RO4350B	Rogers

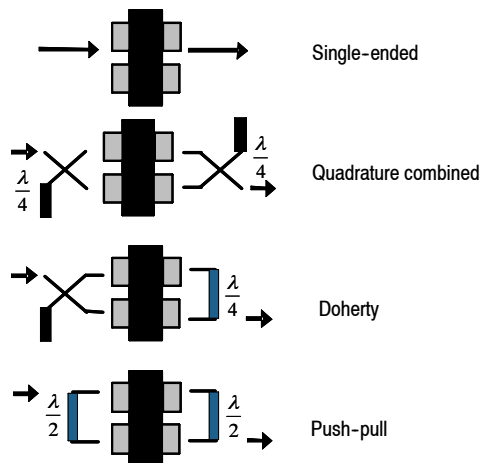


Figure 3. Possible Circuit Topologies

TYPICAL CHARACTERISTICS

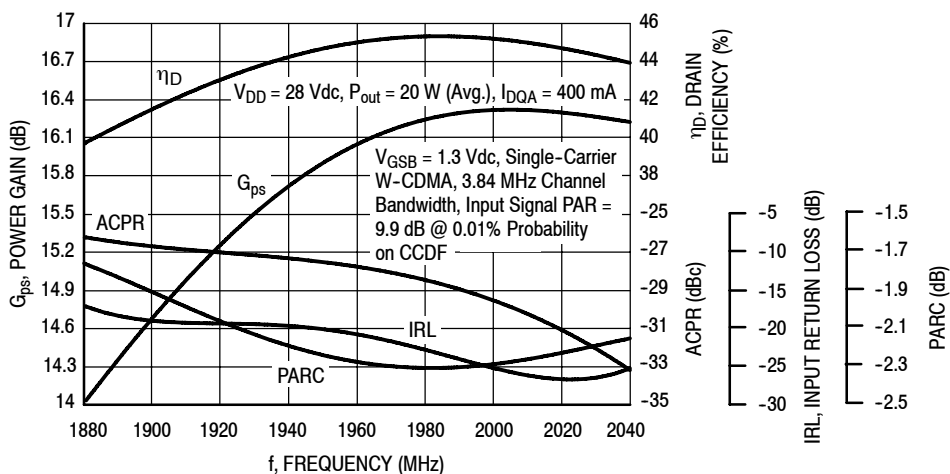


Figure 4. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 20$ Watts Avg.

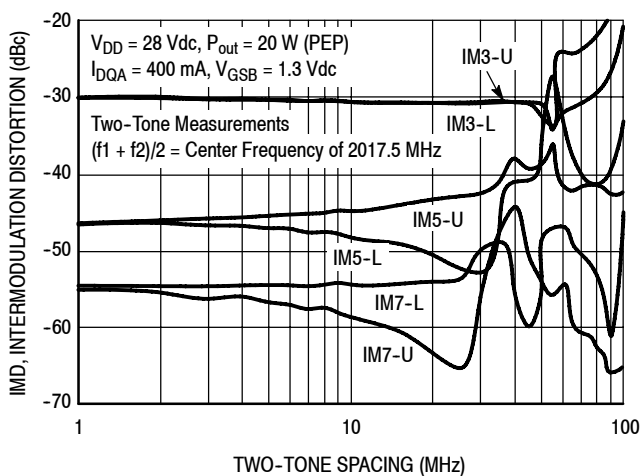


Figure 5. Intermodulation Distortion Products versus Two-Tone Spacing

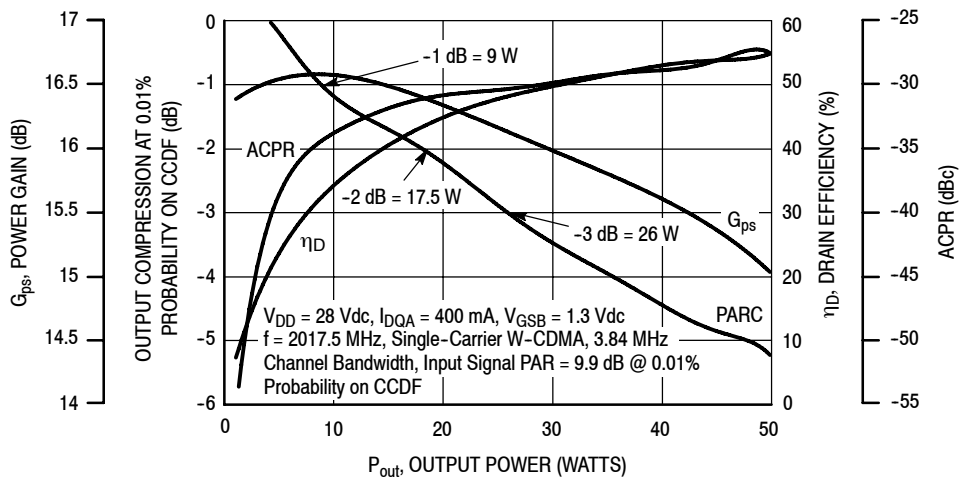


Figure 6. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

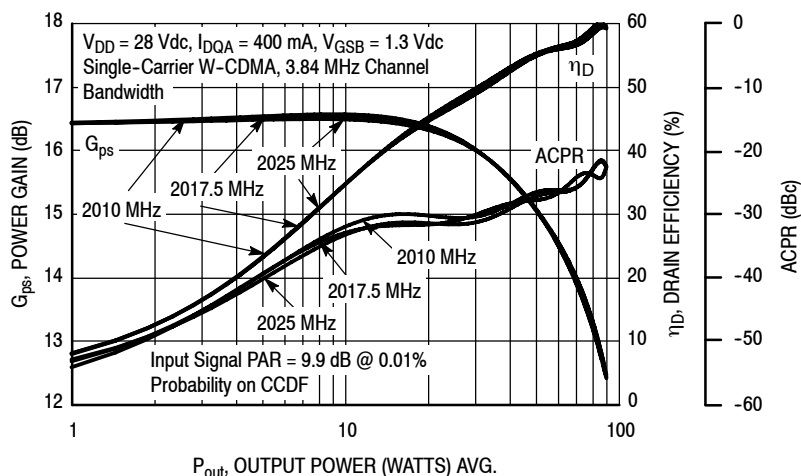


Figure 7. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

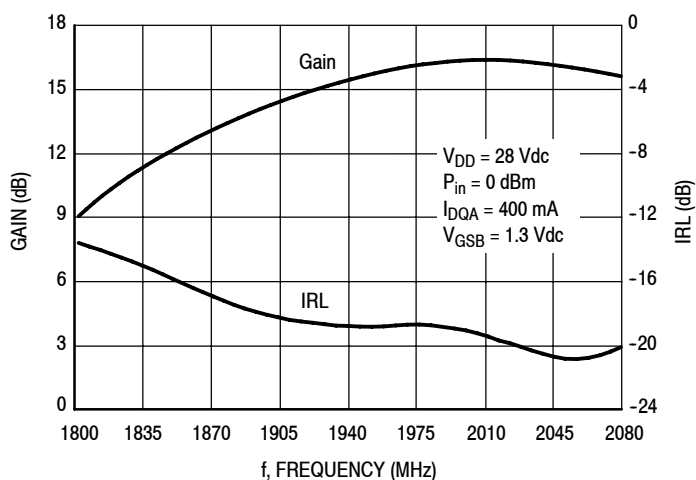


Figure 8. Broadband Frequency Response

W-CDMA TEST SIGNAL

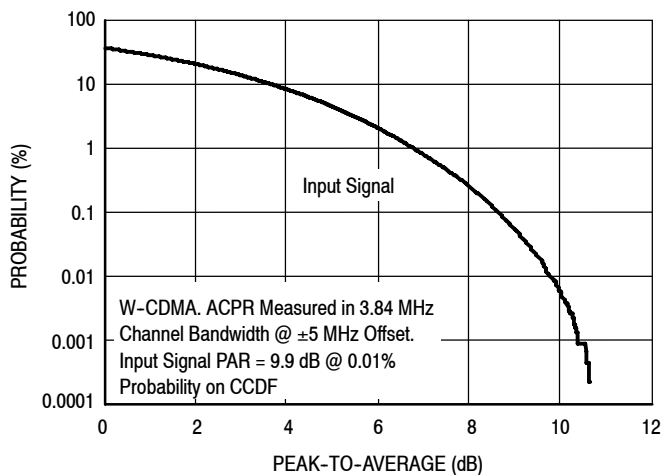


Figure 9. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal

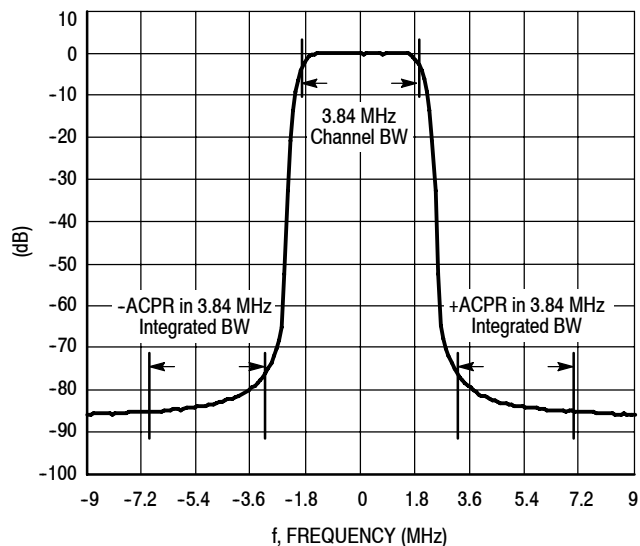


Figure 10. Single-Carrier W-CDMA Spectrum

$V_{DD} = 28 \text{ Vdc}$, $I_{DQA} = 400 \text{ mA}$, $V_{GSB} = 1.3 \text{ Vdc}$, $P_{out} = 20 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
1880	$3.23 - j10.1$	$6.35 - j5.32$
1900	$3.36 - j9.78$	$6.64 - j5.29$
1920	$3.42 - j9.61$	$6.86 - j5.42$
1940	$3.33 - j9.44$	$6.94 - j5.64$
1960	$3.22 - j9.16$	$6.99 - j5.82$
1980	$3.31 - j8.90$	$7.17 - j6.03$
2000	$3.48 - j8.87$	$7.33 - j6.46$
2020	$3.39 - j8.92$	$7.10 - j6.92$
2040	$3.13 - j8.58$	$6.64 - j6.97$

Note: Measured with Peaking side open.

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

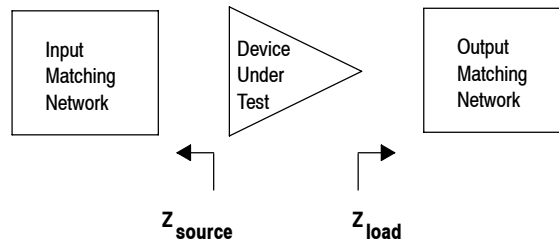


Figure 11. Series Equivalent Source and Load Impedance — Carrier Side

$V_{DD} = 28 \text{ Vdc}$, $I_{DQA} = 400 \text{ mA}$, $V_{GSB} = 1.3 \text{ Vdc}$, $P_{out} = 20 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
1880	$3.83 - j10.28$	$0.67 - j7.03$
1900	$3.88 - j10.00$	$0.68 - j6.71$
1920	$3.82 - j9.81$	$0.62 - j6.43$
1940	$3.61 - j9.59$	$0.48 - j6.11$
1960	$3.50 - j9.30$	$0.35 - j5.70$
1980	$3.58 - j9.10$	$0.35 - j5.32$
2000	$3.61 - j9.13$	$0.35 - j5.07$
2020	$3.43 - j9.10$	$0.21 - j4.75$
2040	$3.10 - j8.55$	$0.10 - j4.19$

Note: Measured with Carrier side open.

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

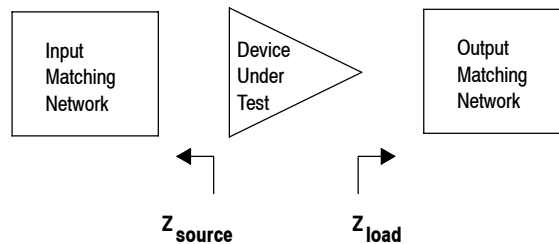
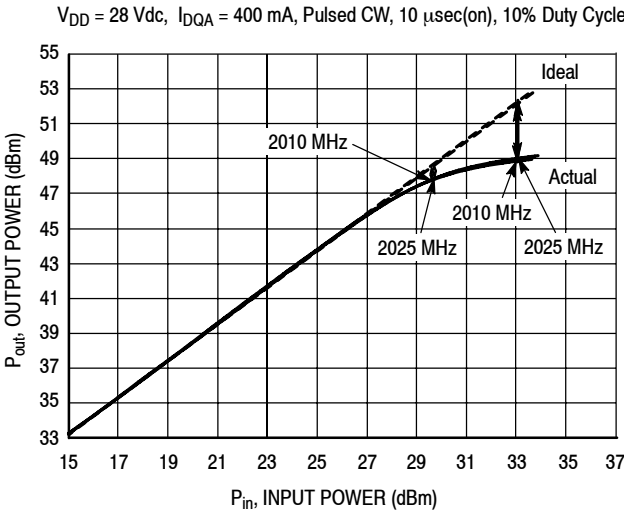


Figure 12. Series Equivalent Source and Load Impedance — Peaking Side

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS



f (MHz)	P1dB		P3dB	
	Watts	dBm	Watts	dBm
2010	62	47.9	76	48.8
2025	63	48.0	78	48.9

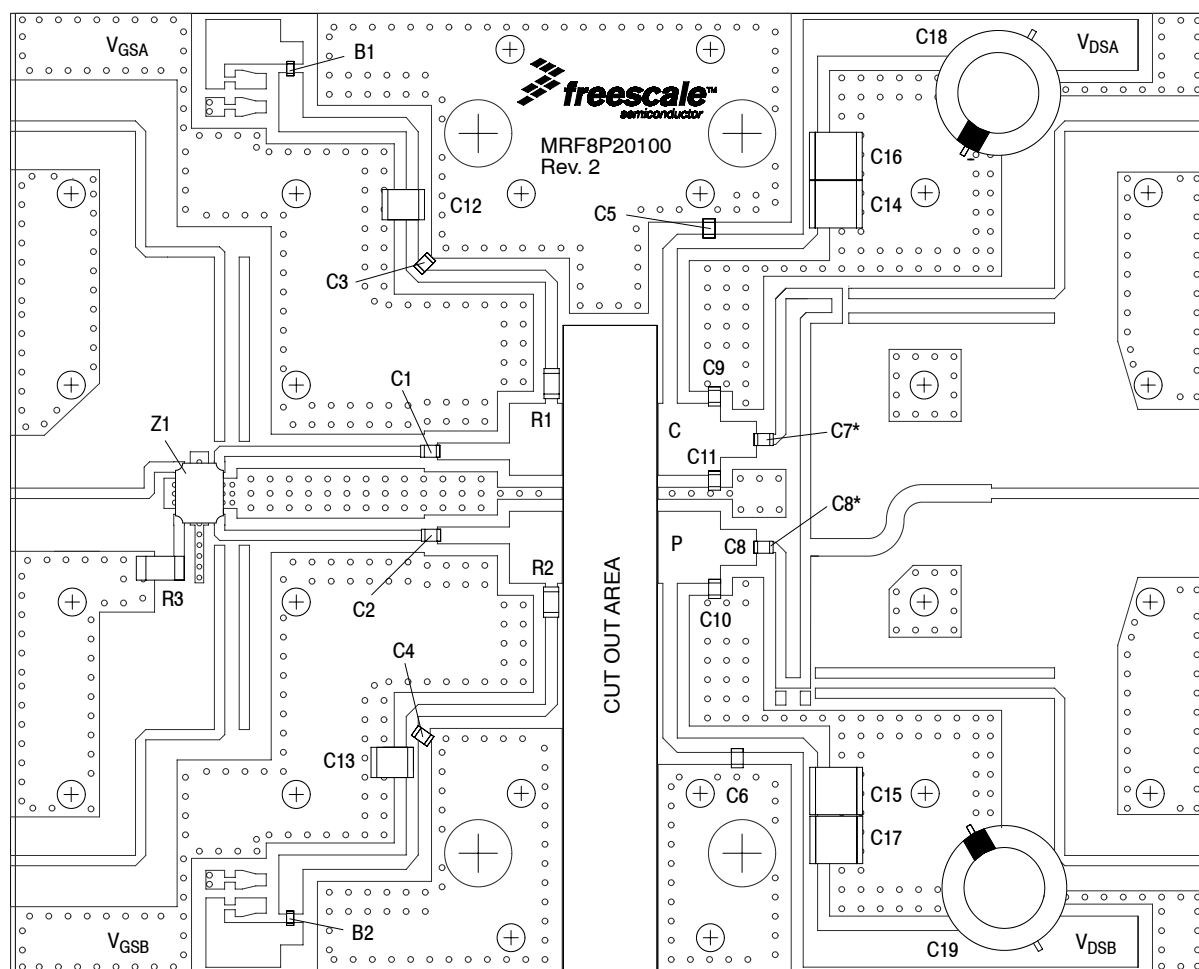
Test Impedances per Compression Level

f (MHz)		Z_{source} Ω	Z_{load} Ω
2010	P1dB	$2.83 - j12.46$	$3.18 - j6.16$
2025	P1dB	$3.43 - j13.20$	$3.16 - j6.14$

Figure 13. Pulsed CW Output Power
versus Input Power @ 28 V

NOTE: Measurement made on the Class AB, carrier side of the device.

ALTERNATE CHARACTERIZATION — 1880 MHz



*C7 and C8 are mounted vertically.

Figure 14. MRF8P20100HR3(HSR3) Test Circuit Component Layout — 1880 MHz

Table 6. MRF8P20100HR3(HSR3) Test Circuit Component Designations and Values — 1880 MHz

Part	Description	Part Number	Manufacturer
B1, B2	RF Ferrite Beads	MPZ2012S300AT000	TDK
C1, C2, C3, C4, C5, C6	12 pF Chip Capacitors	ATC600F120JT250XT	ATC
C7, C8	10 pF Chip Capacitors	ATC600F100JT250XT	ATC
C9, C10, C11	1.5 pF Chip Capacitors	ATC600F1R5BT250XT	ATC
C12, C13	4.7 μ F, 50 V Chip Capacitors	C4532X5R1H475MT	TDK
C14, C15	10 μ F, 50 V Chip Capacitors	C5750X7R1H106KT	TDK
C16, C17	22 μ F, 50 V Chip Capacitors	C5750KF1H226ZT	TDK
C18, C19	220 μ F, 63 V Electrolytic Capacitors	MCGPR63V227M10X21	Multicomp
R1, R2	12 Ω , 1/4 W Chip Resistors	CRCW120612R0FKEA	Vishay
R3	50 Ω , 4 W Chip Resistor	CW12010T0050GBK	ATC
Z1	1900 MHz Band 90°, 3 dB Chip Hybrid Coupler	1P503S	Anaren
PCB	0.020", $\epsilon_r = 3.5$	RO4350B	Rogers

TYPICAL CHARACTERISTICS — 1880 MHz

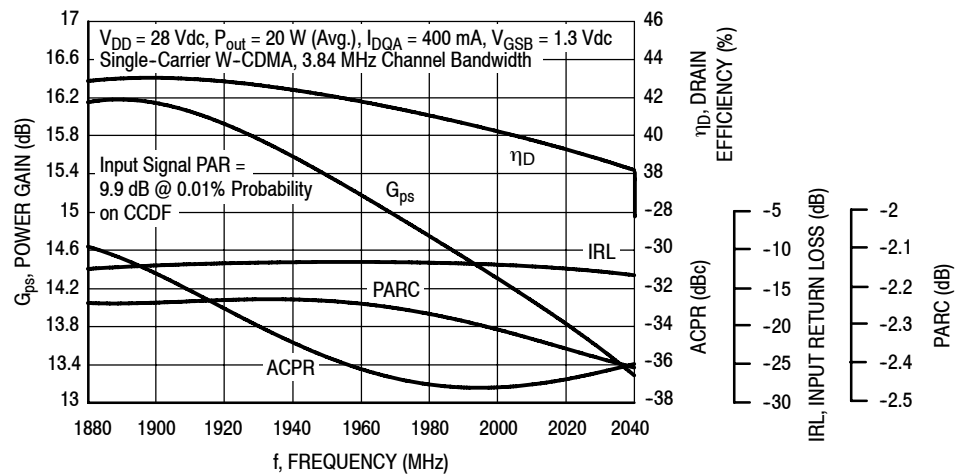


Figure 15. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 20$ Watts Avg.

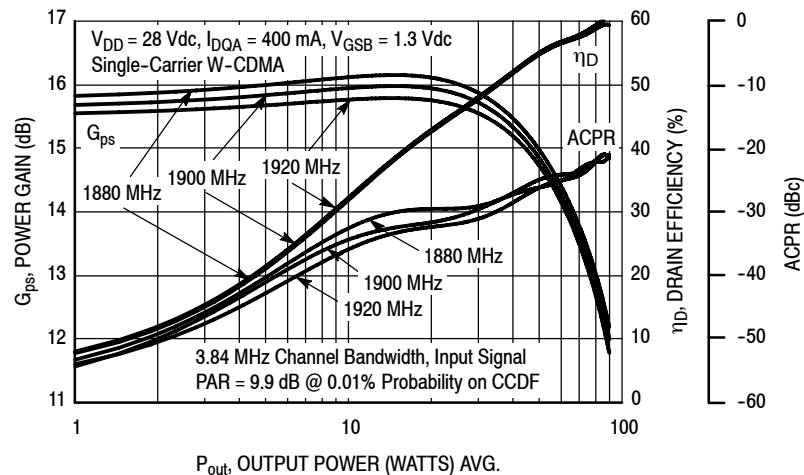


Figure 16. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

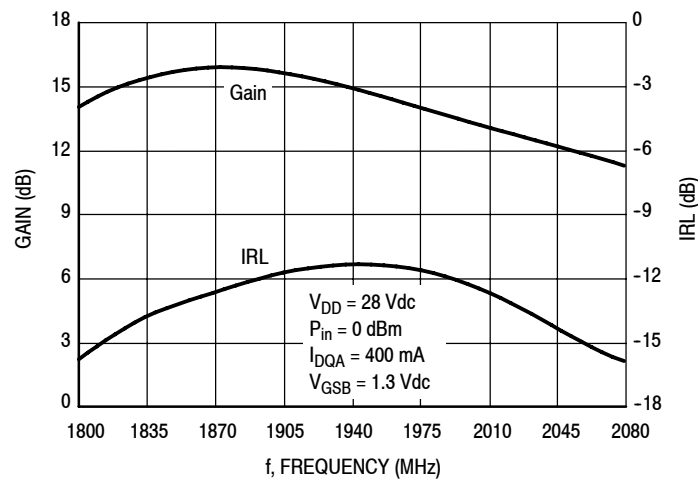


Figure 17. Broadband Frequency Response

$V_{DD} = 28 \text{ Vdc}$, $I_{DQA} = 400 \text{ mA}$, $V_{GSB} = 1.3 \text{ Vdc}$, $P_{out} = 20 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
1880	$2.22 - j7.34$	$6.32 - j6.84$
1900	$2.27 - j7.04$	$6.13 - j6.84$
1920	$2.35 - j6.75$	$5.91 - j6.87$
1940	$2.41 - j6.52$	$5.61 - j6.97$
1960	$2.40 - j6.33$	$5.25 - j7.09$
1980	$2.42 - j6.19$	$4.95 - j7.22$
2000	$2.45 - j6.17$	$4.62 - j7.41$
2020	$2.34 - j6.19$	$4.09 - j7.46$
2040	$2.15 - j5.91$	$3.56 - j7.08$

Note: Measured with Peaking side open.

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

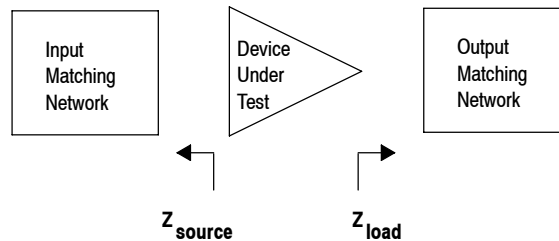


Figure 18. Series Equivalent Source and Load Impedance — Carrier Side — 1880 MHz

$V_{DD} = 28 \text{ Vdc}$, $I_{DQA} = 400 \text{ mA}$, $V_{GSB} = 1.3 \text{ Vdc}$, $P_{out} = 20 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
1880	$2.67 - j6.62$	$0.50 - j3.80$
1900	$2.71 - j6.34$	$0.66 - j3.23$
1920	$2.76 - j6.11$	$0.88 - j2.69$
1940	$2.69 - j5.98$	$1.10 - j2.22$
1960	$2.62 - j5.84$	$1.36 - j1.80$
1980	$2.58 - j5.76$	$1.66 - j1.45$
2000	$2.50 - j5.75$	$2.03 - j1.17$
2020	$2.29 - j5.63$	$2.37 - j0.98$
2040	$2.11 - j5.23$	$2.64 - j0.79$

Note: Measured with Carrier side open.

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

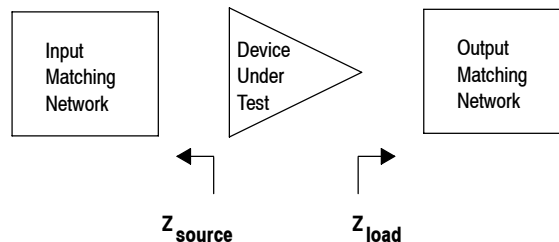


Figure 19. Series Equivalent Source and Load Impedance — Peaking Side — 1880 MHz

ALTERNATE CHARACTERIZATION — GSM EDGE

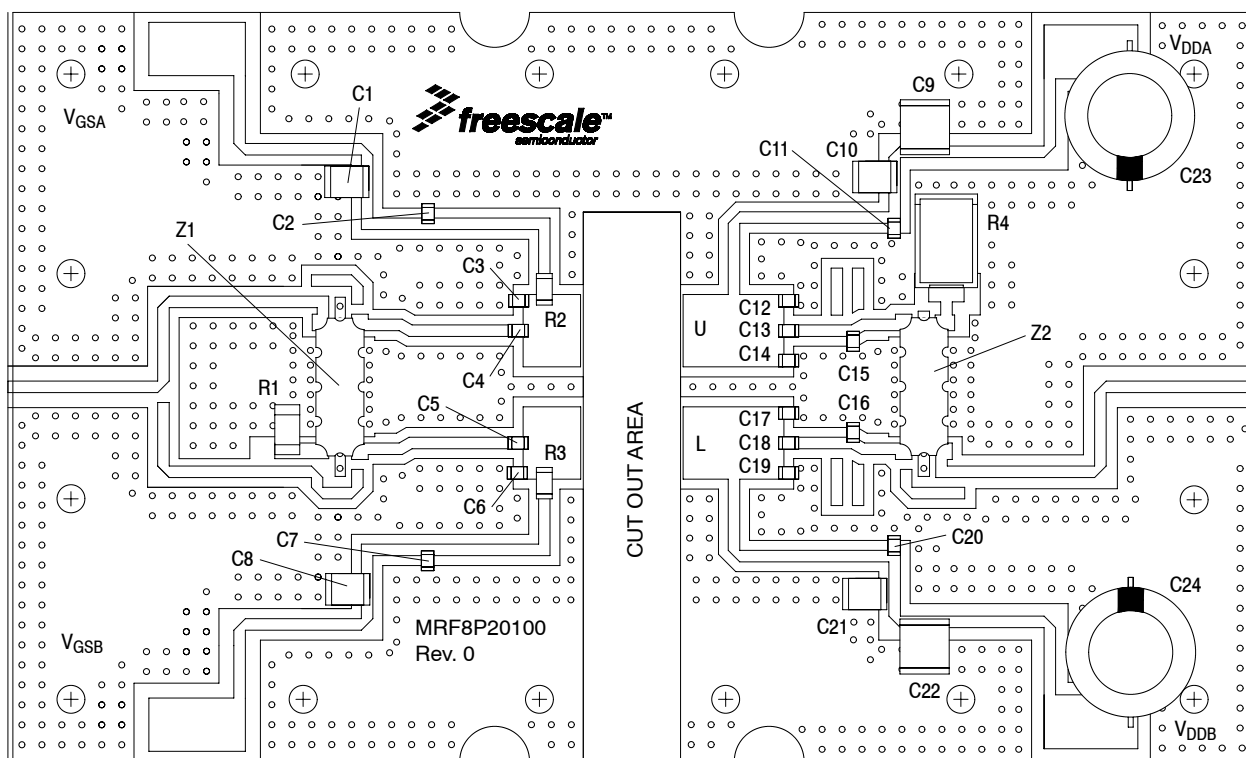


Figure 20. MRF8P20100HR3(HSR3) Test Circuit Component Layout — GSM EDGE

Table 7. MRF8P20100HR3(HSR3) Test Circuit Component Designations and Values — GSM EDGE

Part	Description	Part Number	Manufacturer
C1, C8	2.2 μ F, 50 V Chip Capacitors	C3225X7R2A225KT	TDK
C2, C7	12 pF Chip Capacitors	ATC600F120JT250XT	ATC
C3, C6	2.7 pF Chip Capacitors	ATC600F2R7BT250XT	ATC
C4, C5, C11, C20	15 pF Chip Capacitors	ATC600F150JT250XT	ATC
C9, C22	10 μ F, 50 V Chip Capacitors	C5750X7R1H106K	TDK
C10, C21	4.7 μ F, 50 V Chip Capacitors	C4532X5R1H475M	TDK
C12, C19	0.3 pF Chip Capacitors	ATC600F0R3BT250XT	ATC
C13, C18	22 pF Chip Capacitors	ATC600F220JT250XT	ATC
C14, C17	0.6 pF Chip Capacitors	ATC600F0R6BT250XT	ATC
C15, C16	0.5 pF Chip Capacitors	ATC600F0R5BT250XT	ATC
C23, C24	220 pF, 63 V Electrolytic Capacitors	MCGPR63V227M10X21	Multicomp
R1	50 Ω , 4 W Chip Resistor	CW12010T0050GBK	ATC
R2, R3	12 Ω , 1/4 W Chip Resistors	CRCW120612R0FKEA	Vishay
R4	50 Ω , 80 W, Termination	SMT3725ALNF	EMC
Z1, Z2	1900 MHz Band 90°, 3 dB Chip Hybrid Couplers	XC1900E-03	Anaren
PCB	0.020", $\epsilon_r = 3.5$	RO4350B	Rogers

TYPICAL CHARACTERISTICS — GSM EDGE

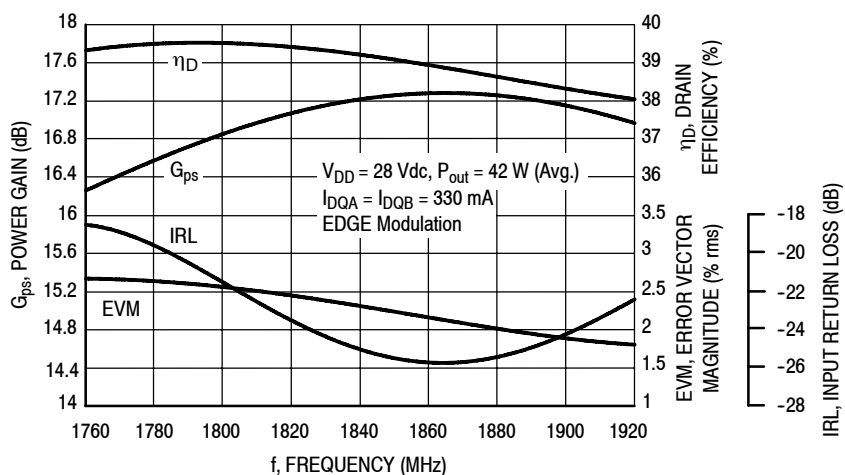


Figure 21. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @ $P_{out} = 42$ Watts Avg.

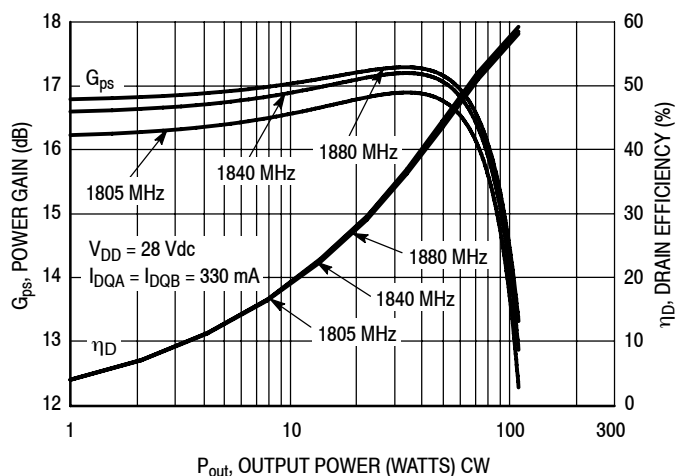


Figure 22. Power Gain and Drain Efficiency versus Output Power

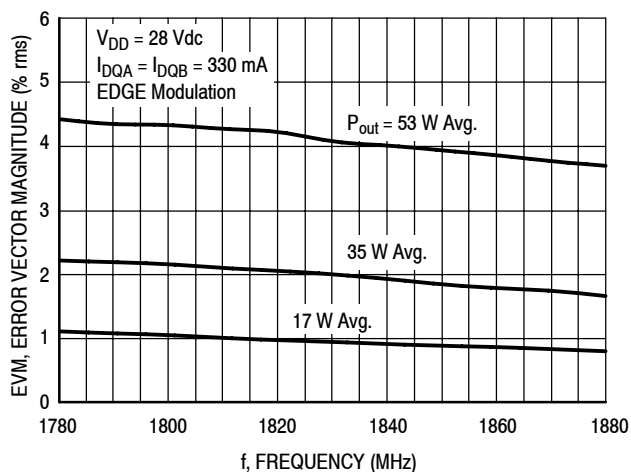


Figure 23. EVM versus Frequency

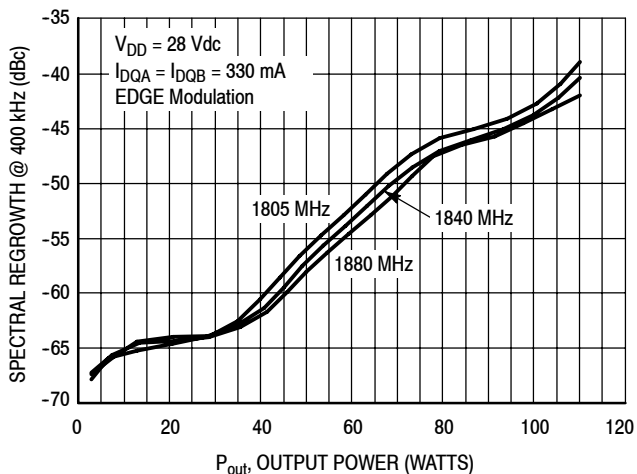


Figure 24. Spectral Regrowth at 400 kHz versus Output Power

TYPICAL CHARACTERISTICS — GSM EDGE

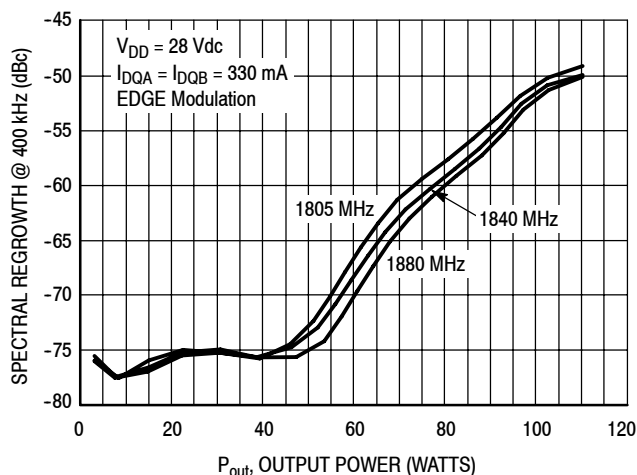


Figure 25. Spectral Regrowth at 600 kHz versus Output Power

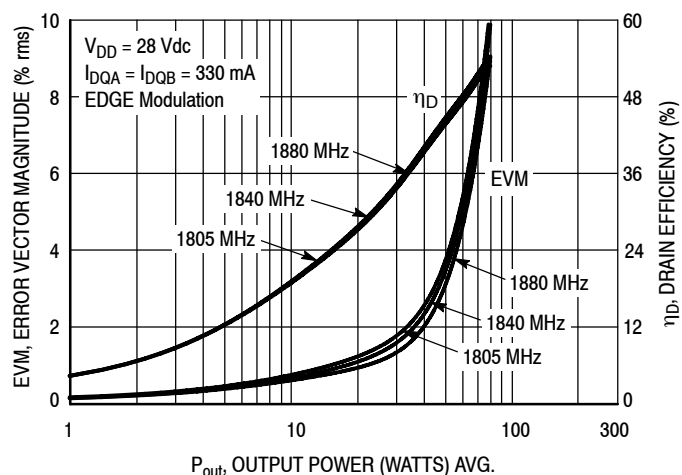


Figure 26. EVM and Drain Efficiency versus Output Power

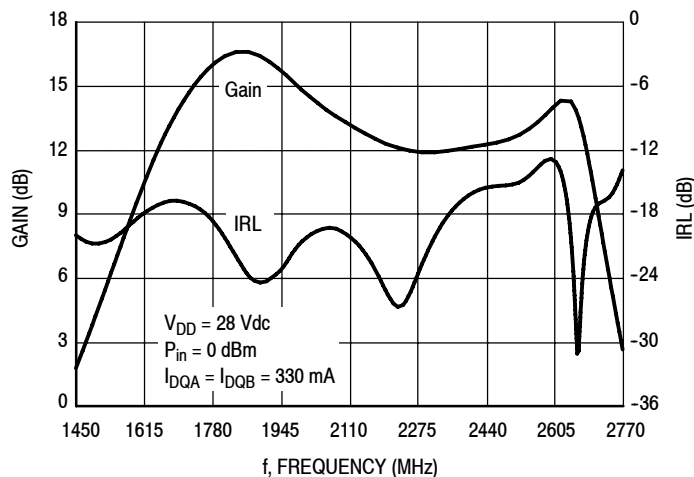


Figure 27. Broadband Frequency Response

$V_{DD} = 28 \text{ Vdc}$, $I_{DQA} = I_{DQB} = 330 \text{ mA}$, $P_{out} = 42 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
1760	$3.12 - j7.74$	$4.39 - j7.66$
1780	$3.13 - j7.35$	$4.44 - j7.38$
1800	$3.21 - j7.12$	$4.50 - j7.30$
1820	$3.20 - j7.05$	$4.42 - j7.31$
1840	$3.08 - j6.98$	$4.26 - j7.28$
1860	$2.95 - j6.82$	$4.10 - j7.15$
1880	$2.88 - j6.57$	$4.00 - j6.92$
1900	$2.87 - j6.21$	$3.95 - j6.62$
1920	$2.89 - j5.85$	$3.94 - j6.36$

Note: Measured with Lower side open.

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

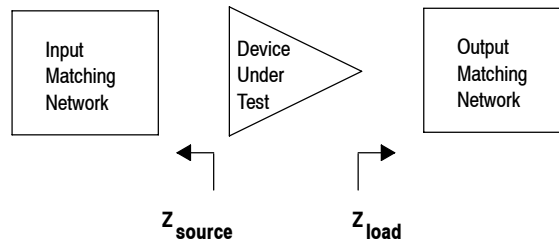


Figure 28. Series Equivalent Source and Load Impedance — Upper Side — GSM EDGE

$V_{DD} = 28 \text{ Vdc}$, $I_{DQA} = I_{DQB} = 330 \text{ Vdc}$, $P_{out} = 42 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
1760	$3.72 - j7.89$	$3.55 - j5.43$
1780	$3.77 - j7.60$	$3.62 - j5.09$
1800	$3.82 - j7.48$	$3.76 - j4.85$
1820	$3.72 - j7.46$	$3.87 - j4.75$
1840	$3.55 - j7.37$	$3.90 - j4.66$
1860	$3.39 - j7.16$	$3.92 - j4.52$
1880	$3.29 - j6.85$	$3.96 - j4.31$
1900	$3.24 - j6.48$	$4.03 - j4.02$
1920	$3.22 - j6.17$	$4.13 - j3.71$

Note: Measured with Upper side open.

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

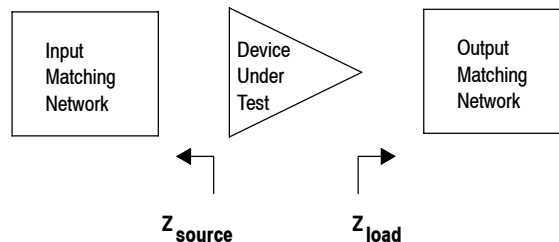
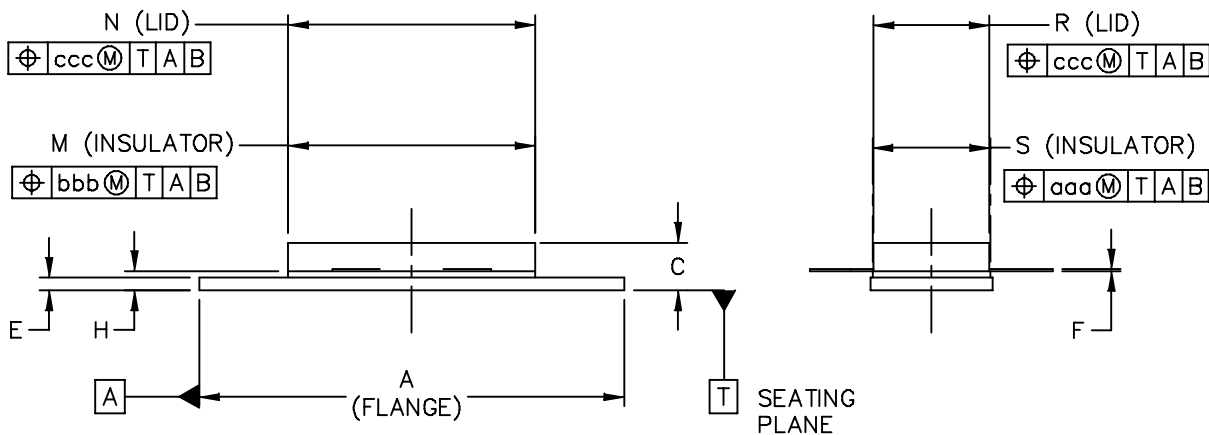
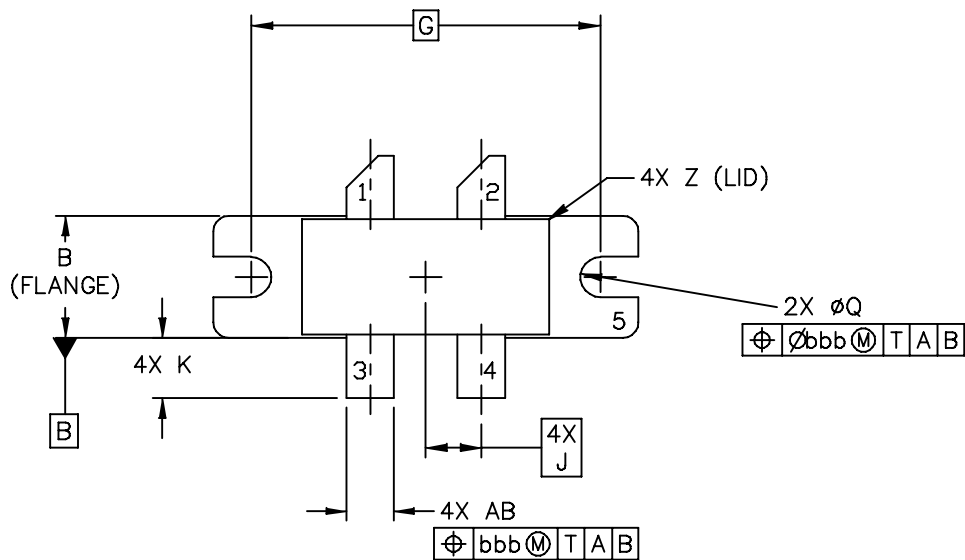


Figure 29. Series Equivalent Source and Load Impedance — Lower Side — GSM EDGE

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE: NI 780-4			DOCUMENT NO: 98ASA10793D		REV: 0
			CASE NUMBER: 465M-01		27 MAR 2007
			STANDARD: NON-JEDEC		

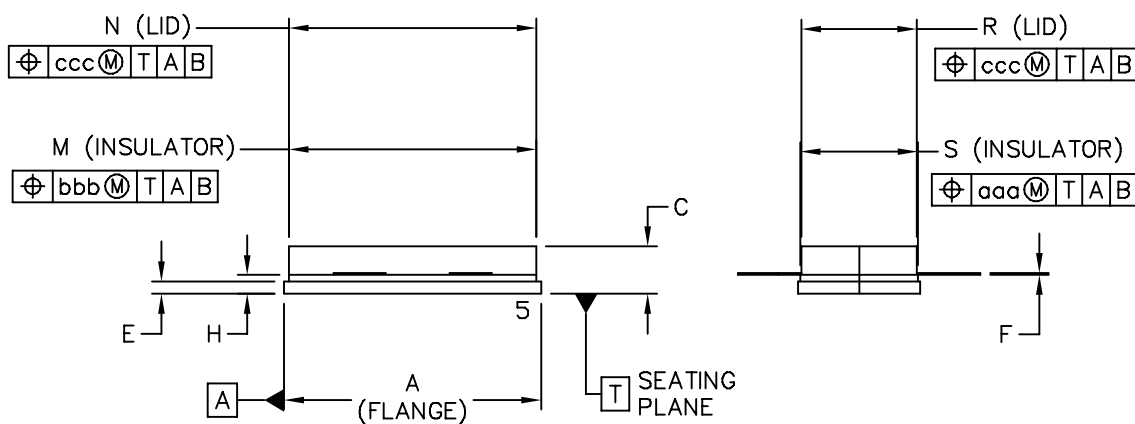
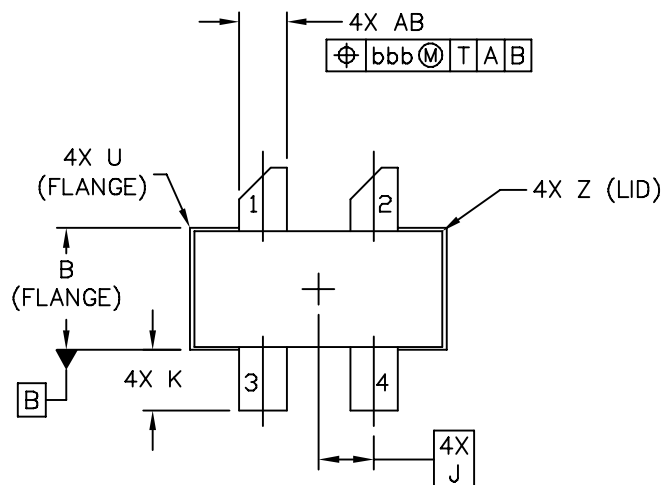
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:

- PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

INCH			MILLIMETER		INCH			MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16	R	.365	.375	9.27	9.53
B	.380	.390	9.65	9.91	S	.365	.375	9.27	9.52
C	.125	.170	3.18	4.32	U		.040		1.02
E	.035	.045	0.89	1.14	Z		.030		0.76
F	.003	.006	0.08	0.15	AB	.145	.155	3.68	3.94
G	1.100 BSC		27.94 BSC						
H	.057	.067	1.45	1.7	aaa	.005		0.127	
J	.175 BSC		4.44 BSC		bbb	.010		0.254	
K	.170	.210	4.32	5.33	ccc	.015		0.381	
M	.774	.786	19.61	20.02					
N	.772	.788	19.61	20.02					
Q	ø.118	ø.138	ø3	ø3.51					
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.				MECHANICAL OUTLINE			PRINT VERSION NOT TO SCALE		
TITLE: NI 780-4					DOCUMENT NO: 98ASA10793D				REV: 0
					CASE NUMBER: 465M-01				27 MAR 2007
					STANDARD: NON-JEDEC				



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE: NI 780S-4		DOCUMENT NO: 98ASA10718D		REV: A	
		CASE NUMBER: 465H-02		27 MAR 2007	
		STANDARD: NON-JEDEC			

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:

- PIN 1. DRAIN
 2. DRAIN
 3. GATE
 4. GATE
 5. SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.805	.815	20.45	20.7	U		.040		1.02
B	.380	.390	9.65	9.91	Z		.030		0.76
C	.125	.170	3.18	4.32	AB	. 145	. 155	3. 68	– 3. 94
E	.035	.045	0.89	1.14					
F	.003	.006	0.08	0.15					
H	.057	.067	1.45	1.7	aaa		.005		0.127
J	. 175 BSC		4. 44 BSC		bbb		.010		0.254
K	.170	.210	4.32	5.33	ccc		.015		0.381
M	.774	.786	19.61	20.02					
N	.772	.788	19.61	20.02					
R	.365	.375	9.27	9.53					
S	.365	.375	9.27	9.52					
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.			MECHANICAL OUTLINE			PRINT VERSION NOT TO SCALE			
TITLE: NI 780S-4					DOCUMENT NO: 98ASA10718D				REV: A
					CASE NUMBER: 465H-02				27 MAR 2007
					STANDARD: NON-JEDEC				

PRODUCT DOCUMENTATION, TOOLS AND SOFTWARE

Refer to the following documents, tools and software to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

For Software and Tools, do a Part Number search at <http://www.freescale.com>, and select the "Part Number" link. Go to the Software & Tools tab on the part's Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Apr. 2010	• Initial Release of Data Sheet

How to Reach Us:

Home Page:

www.freescale.com

Web Support:

<http://www.freescale.com/support>

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2010. All rights reserved.