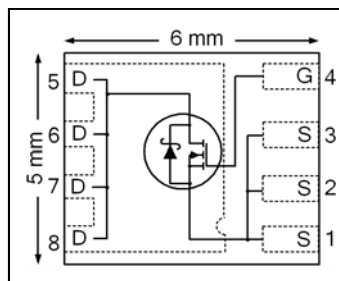


HEXFET® Power MOSFET

V_{DS}	25	V
$R_{DS(on)}$ max (@ $V_{GS} = 10V$)	1.10	mΩ
(@ $V_{GS} = 4.5V$)	1.35	
Q_g (typical)	37.0	nC
I_D (@ T_C (Bottom) = 25°C)	100⑦	A



PQFN 5X6 mm

Applications

- Synchronous Rectifier MOSFET for Synchronous Buck Converters

Features

Low $R_{DS(ON)}$ (<1.10 mΩ)
Schottky Intrinsic Diode with Low Forward Voltage
Low Thermal Resistance to PCB (<1.0°C/W)
Low Profile (<0.9 mm)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant, Halogen-Free
MSL1, Industrial Qualification

results in



Benefits

Lower Conduction Losses
Lower Switching Losses
Enable better thermal dissipation
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFH4210DPbF	PQFN 5mm x 6 mm	Tape and Reel	4000	IRFH4210DTRPbF

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D @ $T_A = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	44	A
I_D @ $T_{C(Bottom)} = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	266⑥⑦	
I_D @ $T_{C(Bottom)} = 100^\circ C$	Continuous Drain Current, V_{GS} @ 10V	168⑥⑦	
I_D @ $T_{C(Bottom)} = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10V (Source Bonding Technology Limited)	100⑦	
I_{DM}	Pulsed Drain Current ①	400	
P_D @ $T_A = 25^\circ C$	Power Dissipation ⑤	3.5	W
P_D @ $T_{C(Bottom)} = 25^\circ C$	Power Dissipation	125	
	Linear Derating Factor	0.028	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ① through ⑦ are on page 8

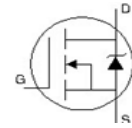
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	25	—	—	V	V _{GS} = 0V, I _D = 1mA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	19	—	mV/°C	Reference to 25°C, I _D = 10mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	0.85	1.10	mΩ	V _{GS} = 10V, I _D = 50A ③
		—	1.10	1.35		V _{GS} = 4.5V, I _D = 50A ③
V _{GS(th)}	Gate Threshold Voltage	1.1	1.6	2.1	V	V _{DS} = V _{GS} , I _D = 100μA
ΔV _{GS(th)}	Gate Threshold Voltage Coefficient	—	-10	—	mV/°C	
I _{DSS}	Drain-to-Source Leakage Current	—	—	250	μA	V _{DS} = 20V, V _{GS} = 0V
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
g _{fs}	Forward Transconductance	392	—	—	S	V _{DS} = 13V, I _D = 50A
Q _g	Total Gate Charge	—	77.0	—	nC	V _{GS} = 10V, V _{DS} = 13V, I _D = 50A
Q _g	Total Gate Charge	—	37.0	55.5	nC	V _{DS} = 13V V _{GS} = 4.5V I _D = 50A
Q _{gs1}	Pre-V _{th} Gate-to-Source Charge	—	7.6	—		
Q _{gs2}	Post-V _{th} Gate-to-Source Charge	—	6.4	—		
Q _{gd}	Gate-to-Drain Charge	—	13.2	—		
Q _{godr}	Gate Charge Overdrive	—	9.8	—		
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	—	19.6	—		
Q _{oss}	Output Charge	—	37	—	nC	V _{DS} = 16V, V _{GS} = 0V
R _G	Gate Resistance	—	1.3	—	Ω	
t _{d(on)}	Turn-On Delay Time	—	19	—	ns	V _{DD} = 13V, V _{GS} = 4.5V I _D = 50A R _G = 1.8Ω
t _r	Rise Time	—	45	—		
t _{d(off)}	Turn-Off Delay Time	—	24	—		
t _f	Fall Time	—	16	—		
C _{iss}	Input Capacitance	—	4812	—	pF	V _{GS} = 0V V _{DS} = 13V f = 1.0MHz
C _{oss}	Output Capacitance	—	1459	—		
C _{rss}	Reverse Transfer Capacitance	—	355	—		

Avalanche Characteristics

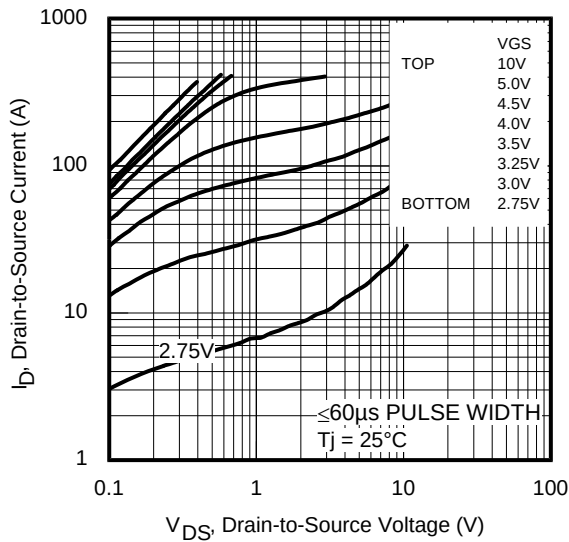
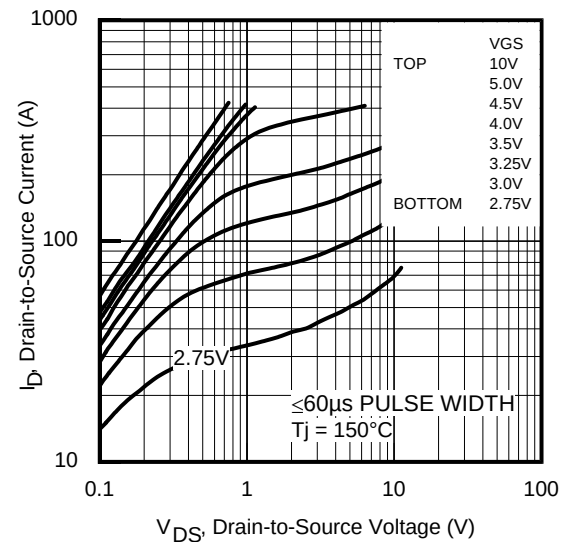
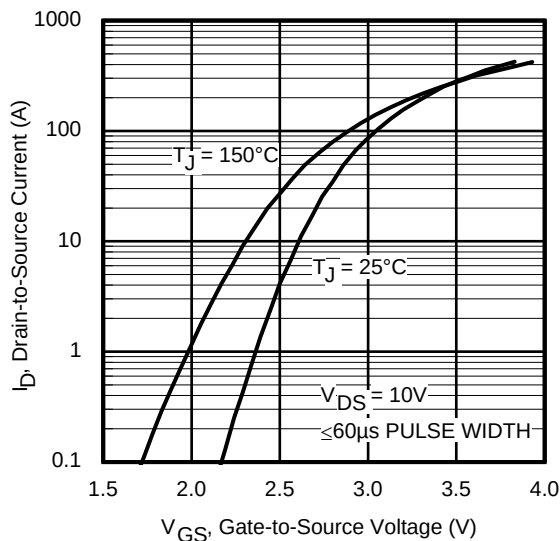
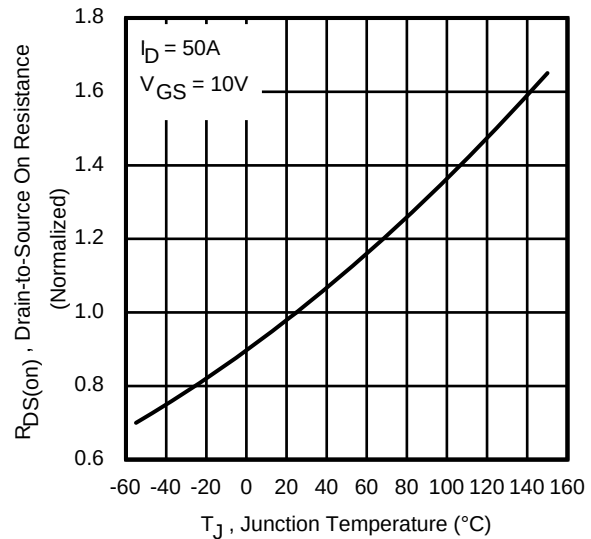
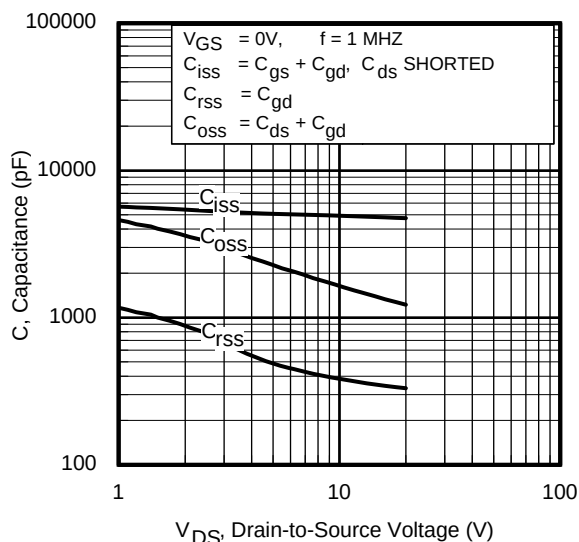
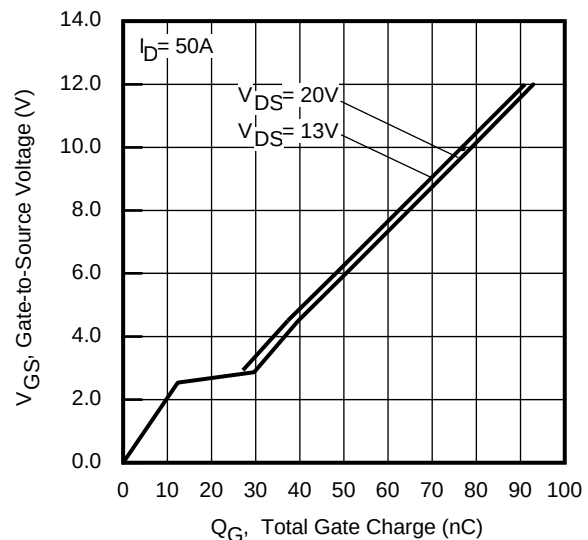
	Parameter	Typ.	Max.
E _{AS}	Single Pulse Avalanche Energy ②	—	247
I _{AR}	Avalanche Current ①	—	50

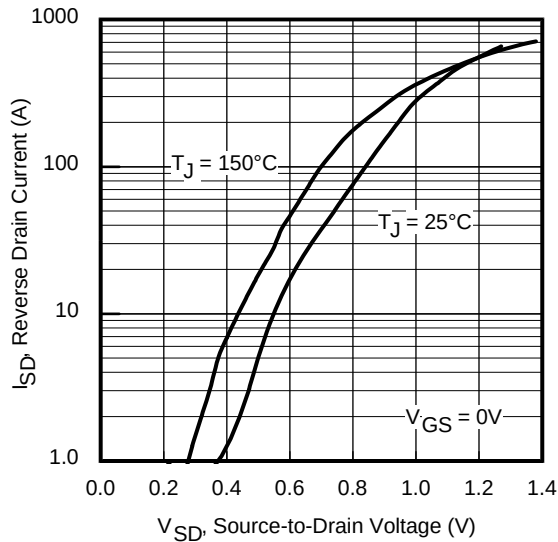
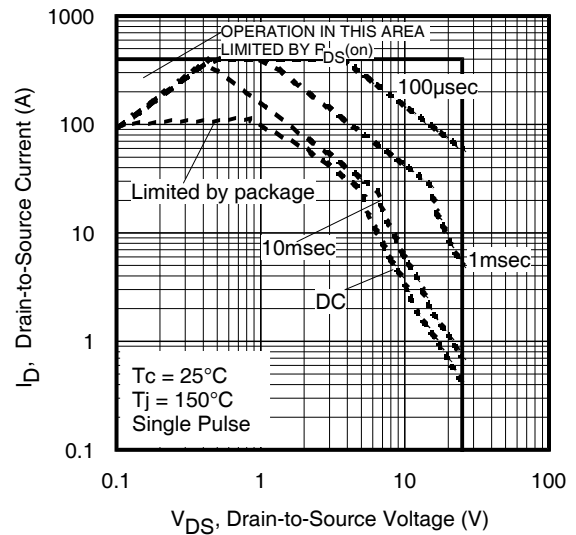
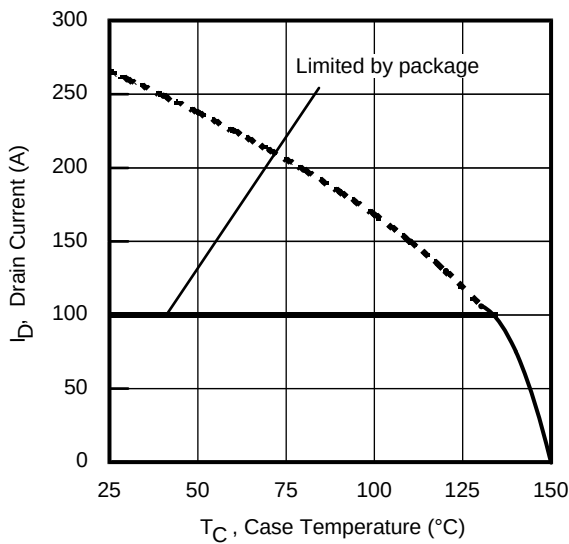
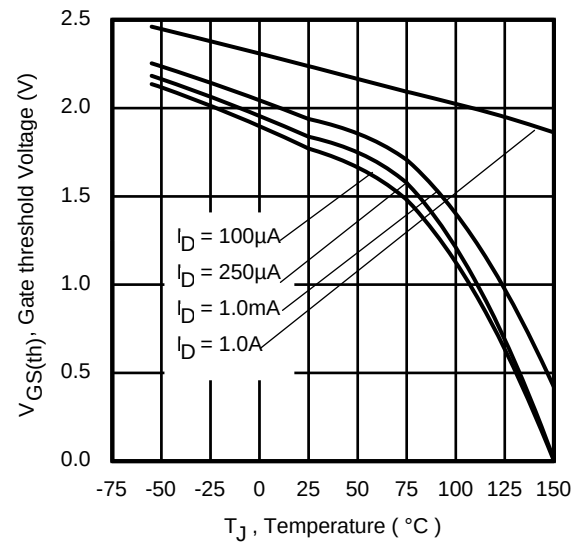
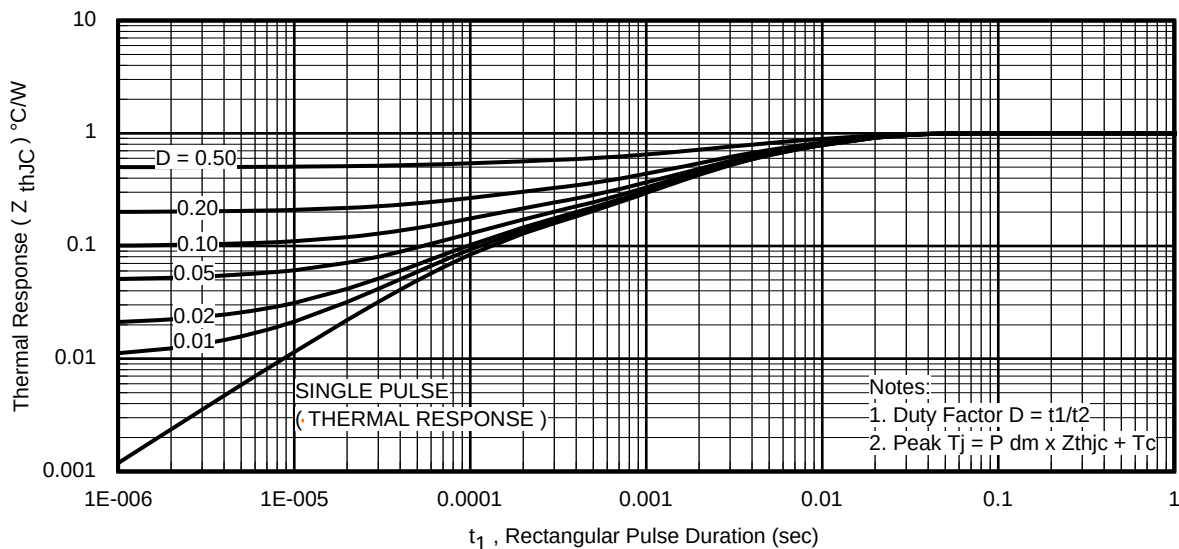
Diode Characteristics

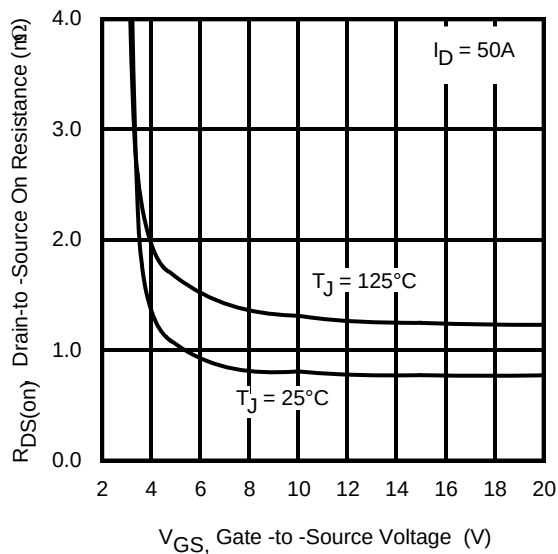
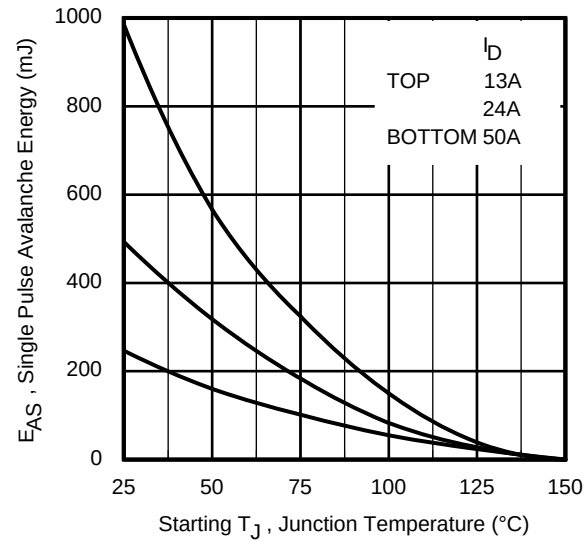
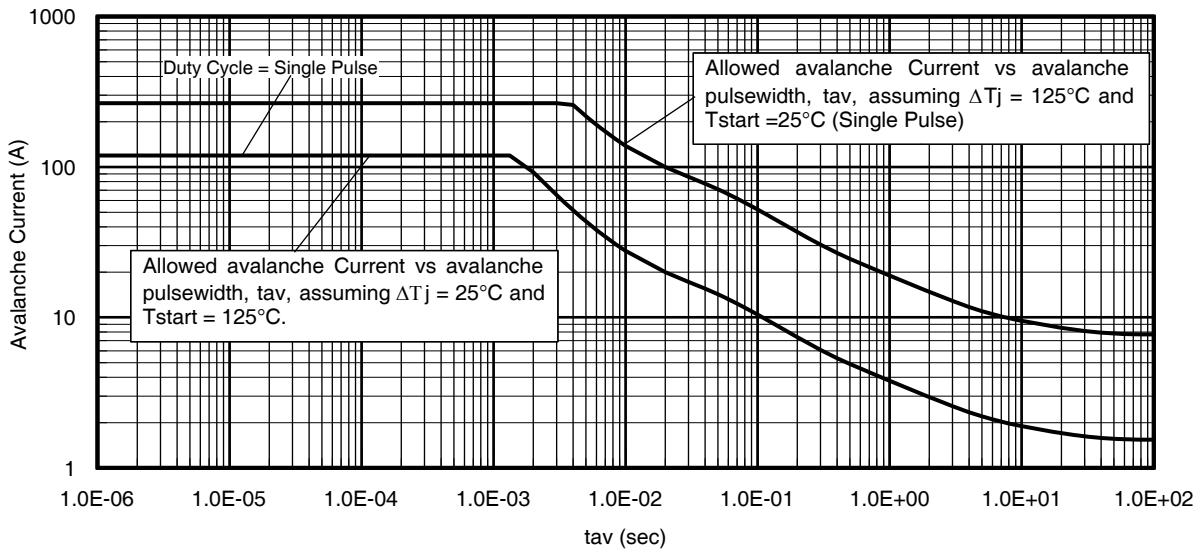
	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	100⑦	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	400		
V _{SD}	Diode Forward Voltage	—	—	0.75	V	T _J = 25°C, I _S = 50A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	—	27	41	ns	T _J = 25°C, I _F = 50A, V _{DD} = 13V di/dt = 300A/μs ③
Q _{rr}	Reverse Recovery Charge	—	59	89	nC	

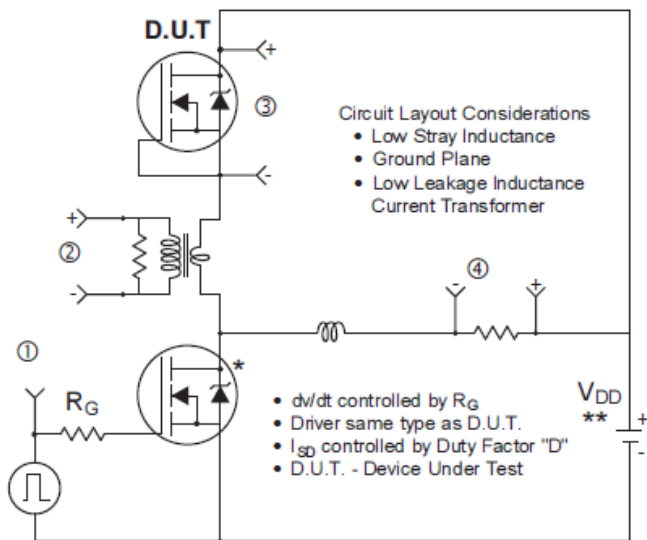
Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC} (Bottom)	Junction-to-Case ④	—	1.0	°C/W
R _{θJC} (Top)	Junction-to-Case ④	—	22	
R _{θJA}	Junction-to-Ambient ⑤	—	36	
R _{θJA} (<10s)	Junction-to-Ambient ⑤	—	21	


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Drain-to-Source Breakdown Voltage

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

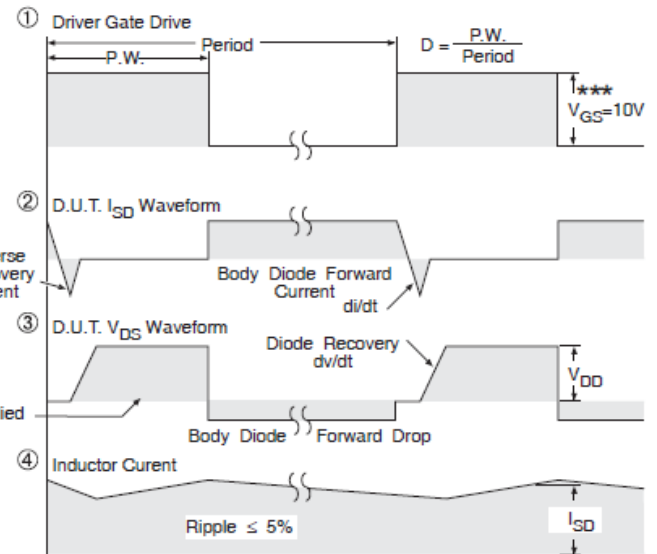

Fig 12. On-Resistance vs. Gate Voltage

Fig 13. Maximum Avalanche Energy vs. Drain Current

Fig 14. Typical Avalanche Current vs. Pulsewidth



* Use P-Channel Driver for P-Channel Measurements

** Reverse Polarity for P-Channel

Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs



*** $V_{GS} = 5V$ for Logic Level Devices

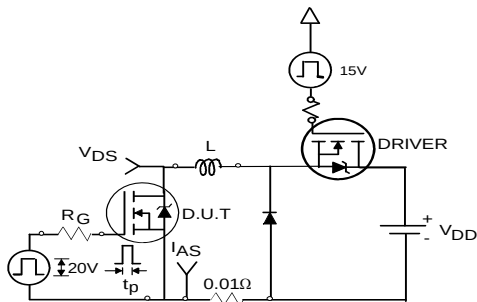


Fig 16a. Unclamped Inductive Test Circuit

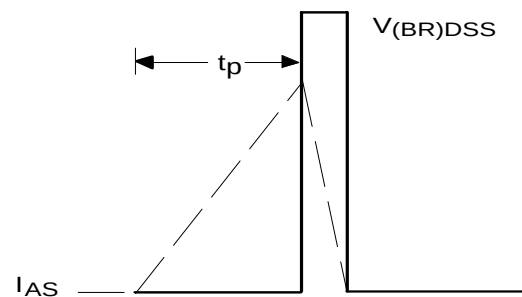


Fig 16b. Unclamped Inductive Waveforms

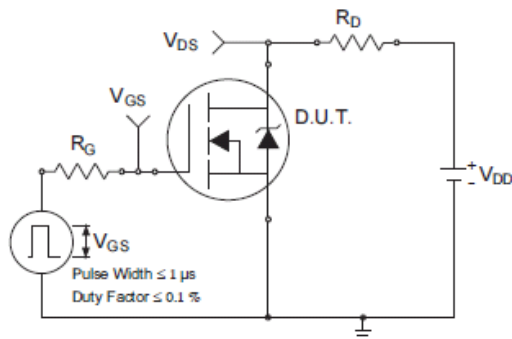


Fig 17a. Switching Time Test Circuit

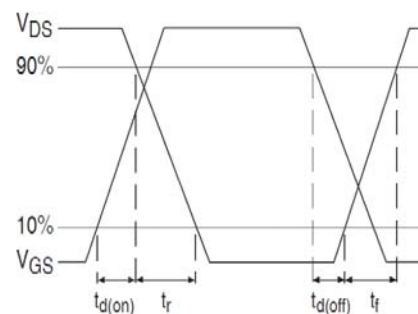


Fig 17b. Switching Time Waveforms

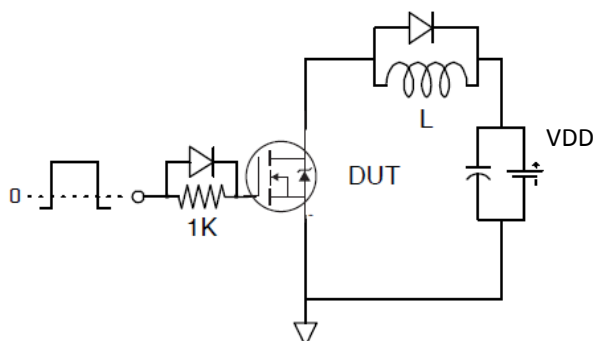


Fig 18. Gate Charge Test Circuit

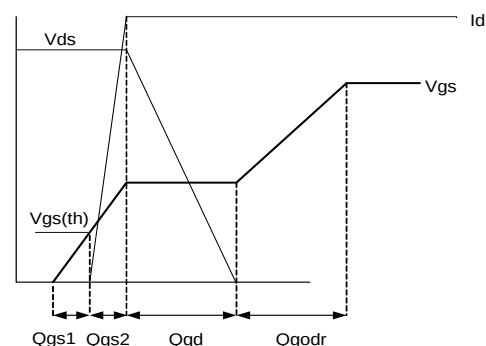
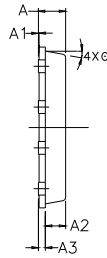
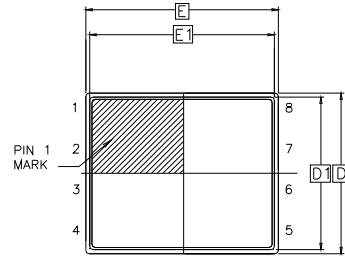


Fig 19. Gate Charge Waveform

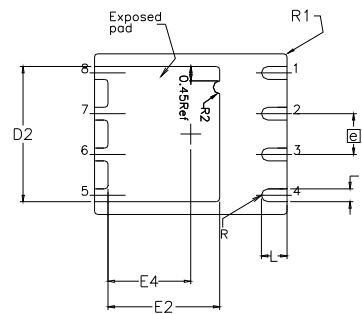
PQFN 5x6 Outline "B" Package Details


SIDE VIEW



TOP VIEW

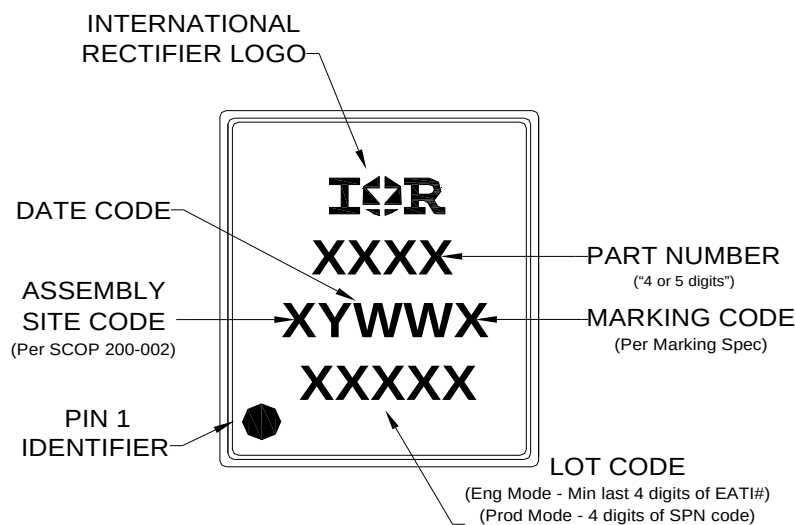
DIM SYMBOL	MIN	NOM	MAX
A	0.800	0.830	1.05
A1	0.000	0.020	0.050
A2	0.580	0.630	0.680
A3		0.254 REF	
Ø	0"	10"	12"
b	0.350	0.400	0.470
D	4.850	5.000	5.150
D1	4.675	4.750	5.000
D2	3.700	4.210	4.300
e		1.270 BSC	
E	5.850	6.000	6.150
E1	5.675	5.750	6.000
E2	3.380	3.480	3.760
E4	2.480	2.580	2.680
L	0.550	0.800	0.900
R		0.200 REF	
R1		0.100 REF	
R2	0.150	0.200	0.250



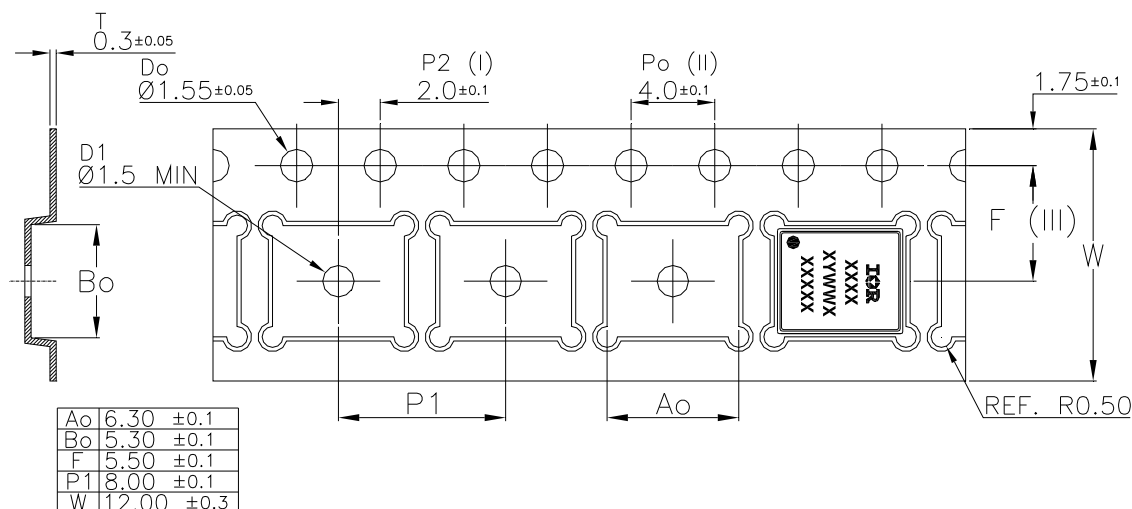
BOTTOM VIEW

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>

For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

PQFN 5x6 Outline "B" Part Marking


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

PQFN 5x6 Outline "B" Tape and Reel


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information[†]

Qualification Level	Industrial (per JEDEC JESD47F ^{††} guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D ^{††})
RoHS Compliant	Yes	

[†] Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability>

^{††} Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.20\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 50\text{A}$.
- ③ Pulse width $\leq 400 \mu\text{s}$; duty cycle $\leq 2\%$.
- ④ R_θ is measured at T_J of approximately 90°C .
- ⑤ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details:
<http://www.irf.com/technical-info/appnotes/an-994.pdf>
- ⑥ Calculated continuous current based on maximum allowable junction temperature.
- ⑦ Current is limited to 100A by source bonding technology.

Revision History

Date	Comments
04/30/2013	Release of final data sheet.
05/17/2013	- Updated package 3D drawing, on page 1. - Added Continuous Drain Current limited by source bonding technology, on page 1. - Divided note 6 into note 6 & 7, on page 8.
08/14/2013	Added "Fast/RFET™" above the part number, on page 1.

International
 Rectifier

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To contact International Rectifier, please visit <http://www.irf.com/whoto-call/>