3.3V Neuron® Chip Network Processor

Features

- 3.3V operation
- **Three 8-bit pipelined processors for concurrent processing of application code and network traffic**
- **Four-pin hardware SCI/SPI interface**
- **Eleven-pin I/O port programmable in 34 modes for fast application program development**
- **Two 16-bit timer/counters for measuring and generating I/O device waveforms**
- **Five-pin communication port that supports direct connect and network transceiver interfaces, and operates at 3.3V or 5V**
- **Programmable pull-ups on IO4–IO7 and 20-mA sink current on IO0–IO3**
- **Unique 48-bit ID number in every device to facilitate network installation and management**
- **0.35-μm Flash process technology**
- **On-chip LVD circuit with programmable trip point**
- **Programmable Pulse Stretching reset**
- **4,096 bytes of SRAM for buffering network data, system, and application data storage**
- **512 bytes (CY7C53150L), 8KB (CY7C53120L8) of Flash memory with on-chip charge pump for flexible storage of configuration data and application code**
- **Addresses up to 58 KB of external memory (CY7C53150L)**
- **12 KB (CY7C53120L8) of ROM containing LonTalk® network protocol firmware**
- **Maximum input clock operation of 20 MHz (CY7C53120L8/3150L) over a –40°C to 85°C[1] temperature range**
- **64-pin and 100-pin TQFP package (CY7C53150L)**
- **32-pin SOIC or 44-pin TQFP package (CY7C53120L8)**

Functional Description

The 3.3V Neuron® chip (CY7C53120L8/3150L) is a low-power version of the 5V Neuron chip with a number of feature enhancements. The CY7C53120L8/3150L Neuron chip implements a node for LonWorks® distributed intelligent control networks. It incorporates, on a single chip, the necessary communication and control functions, both in hardware and firmware, that facilitate the design of a LonWorks node.

The CY7C53120L8/3150L supports all the functionality of the 5V CY7C531x0 Neuron chip. Additionally it features 4 KB of RAM, 8KB of Flash memory (CY7C53120L8), and hardware SCI/SPI. The CY7C53120L8/3150L has an 11-pin configurable I/O block. The I/Os are all 5V-tolerant to allow interfacing to other 5V components and microcontrollers.

The CY7C53120L8/3150L contains a very flexible five-pin communication port that can be configured to interface with a wide variety of media transceivers at a wide range of data rates. The communication port can operate at either 3.3V or 5V. In 5V mode the transceiver is completely backward compatible with existing 5V transceivers. The most common transceiver types are twisted-pair, powerline, RF, IR, fiber-optics, and coaxial.

The CY7C53150L incorporates an external memory interface that can address up to 64 KB with 6 KB of the address space mapped internally. LonWorks nodes that require large application programs can take advantage of this external memory capability.
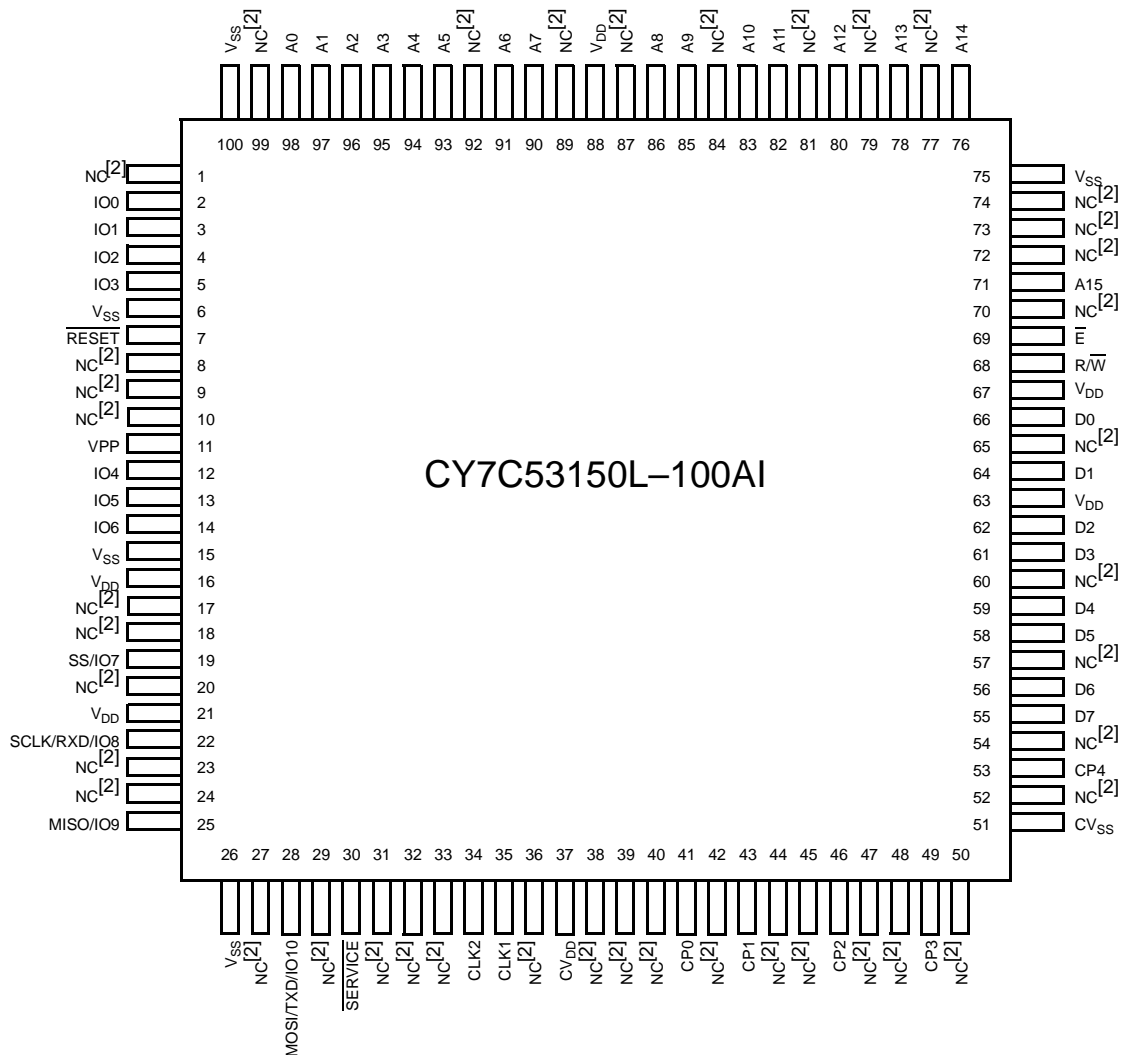
Services at every layer of the OSI networking reference model are implemented in the LonTalk firmware-based protocol stored in 12-KB ROM (CY7C53120L8), or off-chip memory (CY7C53150L). The firmware also contains 34 preprogrammed I/O drivers, simplifying application programming. The application program is stored in the Flash memory (CY7C53120L8) and/or off-chip memory (CY7C53150L), and may be updated by downloading over the network.

Logic Block Diagram
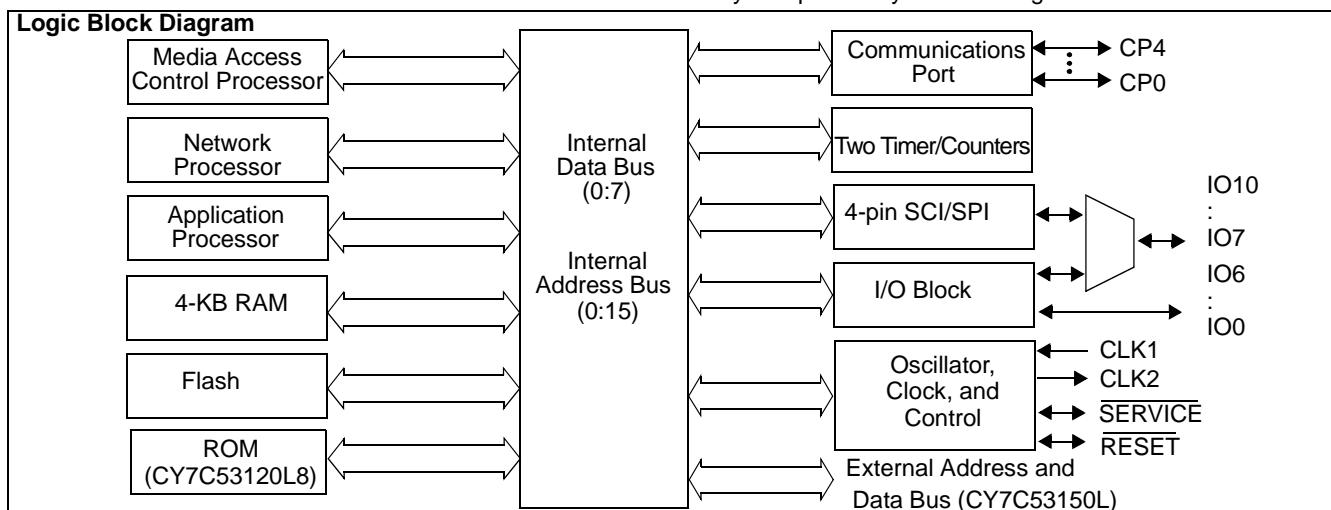
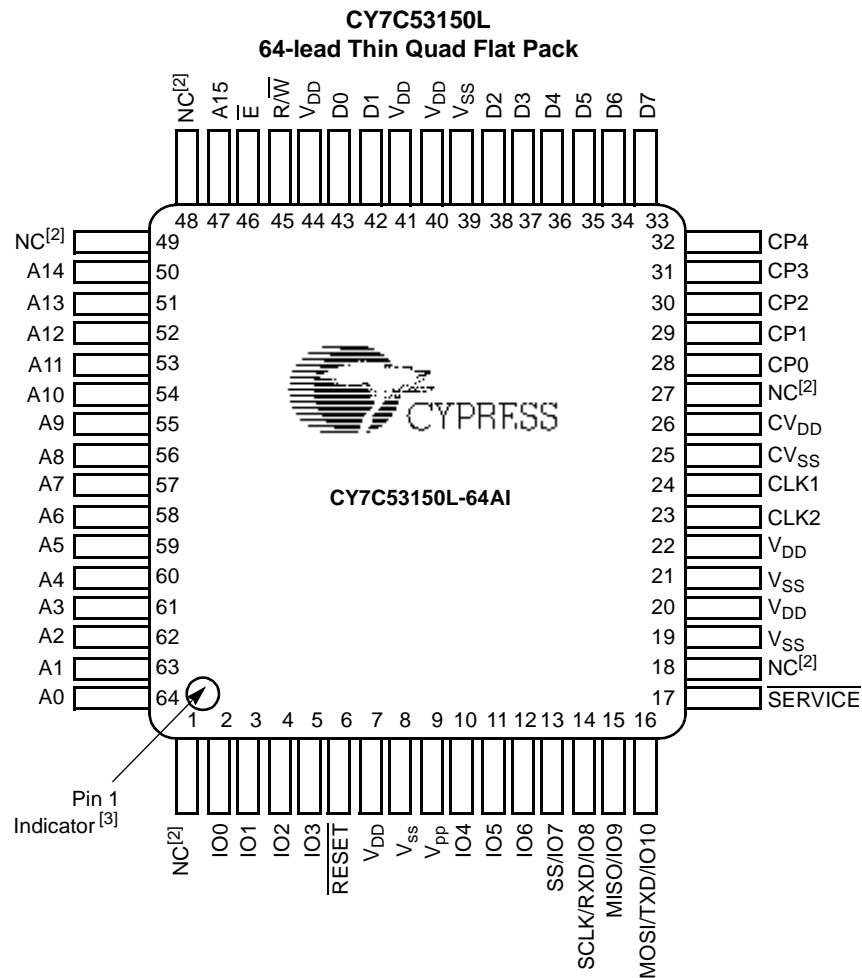
Note:
1. Maximum junction temperature is 105°C. $T_{Junction} = T_{Ambient} + V•I•\theta_{JA}$. 32-pin SOIC θ_{JA} = 51°C/W. 44-pin TQFP θ_{JA} = 43°C/W. 64-pin TQFP θ_{JA} = 44°C/W. 100-pin TQFP θ_{JA} = 49.2°C/W.

CY7C53150L
100-lead Thin Quad Flat Pack

Top-side pins (100–76): V_{SS}, NC[2], A0, A1, A2, A3, A4, A5, NC[2], A6, A7, NC[2], V_{DD}, NC[2], A8, A9, NC[2], A10, A11, NC[2], A12, NC[2], A13, NC[2], A14

Left-side pins (1–25):

Pin	Signal
1	NC[2]
2	IO0
3	IO1
4	IO2
5	IO3
6	V_{SS}
7	$\overline{RESET}$
8	NC[2]
9	NC[2]
10	NC[2]
11	VPP
12	IO4
13	IO5
14	IO6
15	V_{SS}
16	V_{DD}
17	NC[2]
18	NC[2]
19	SS/IO7
20	NC[2]
21	V_{DD}
22	SCLK/RXD/IO8
23	NC[2]
24	NC[2]
25	MISO/IO9

Center label: CY7C53150L–100AI

Right-side pins (75–51):

Pin	Signal
75	V_{SS}
74	NC[2]
73	NC[2]
72	NC[2]
71	A15
70	NC[2]
69	$\overline{E}$
68	R/$\overline{W}$
67	V_{DD}
66	D0
65	NC[2]
64	D1
63	V_{DD}
62	D2
61	D3
60	NC[2]
59	D4
58	D5
57	NC[2]
56	D6
55	D7
54	NC[2]
53	CP4
52	NC[2]
51	CV_{SS}

Bottom-side pins (26–50): V_{SS}, NC[2], MOSI/TXD/IO10, NC[2], $\overline{SERVICE}$, NC[2], NC[2], NC[2], CLK2, CLK1, NC[2], CV_{DD}, NC[2], NC[2], NC[2], CP0, NC[2], CP1, NC[2], NC[2], CP2, NC[2], NC[2], CP3, NC[2]

Note:
2. No Connect (NC) — should not be used. (These pins may be used for internal testing.)

CY7C53150L
64-lead Thin Quad Flat Pack

Pin 1
Indicator [3]

CY7C53150L-64AI

Note:
3. The smaller dimple at the bottom left of the marking indicates pin 1.

44-lead TQFP

32-lead SOIC

PIN 1
INDICATOR
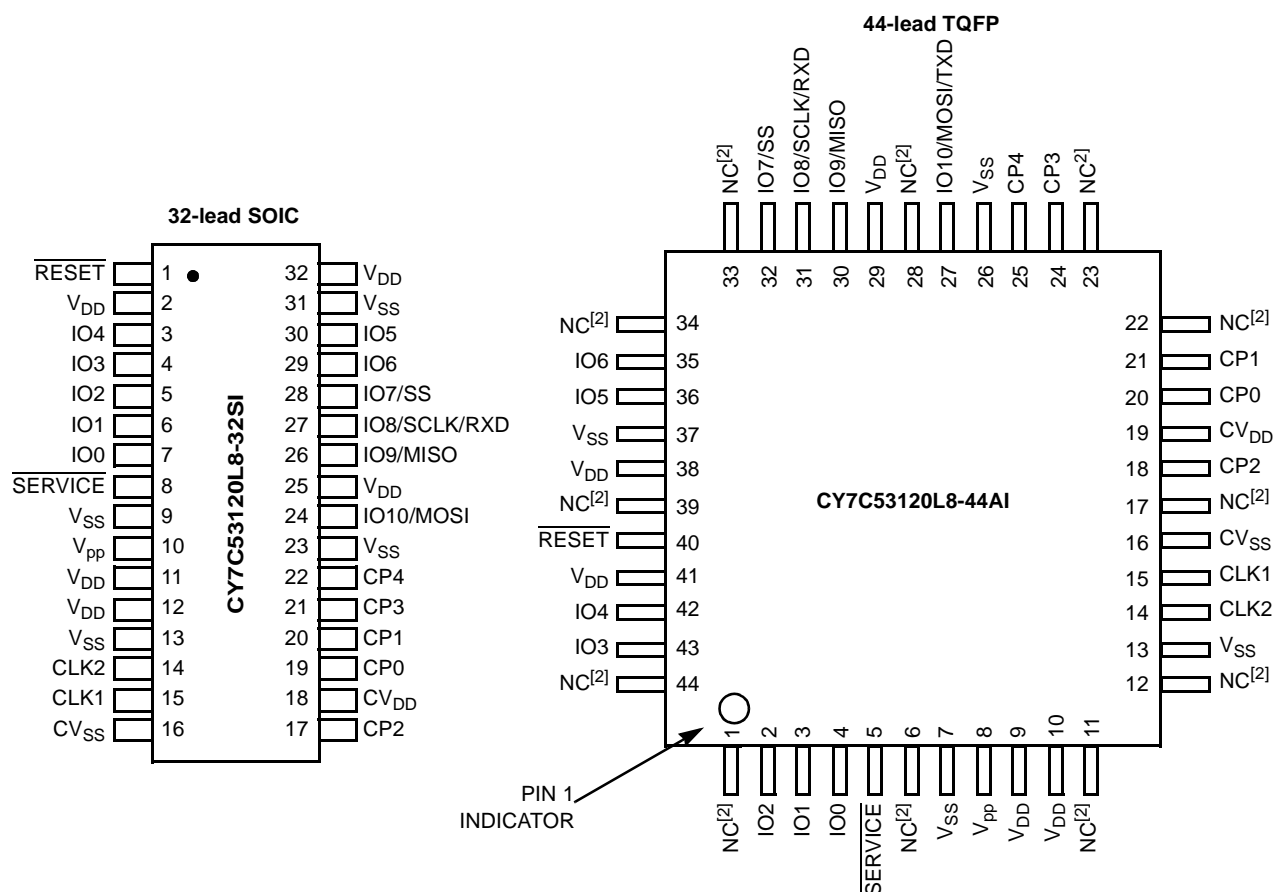
Pin Descriptions

Pin Name	I/O	Pin Function	CY7C53150L TQFP-100 Pin No.	CY7C53150L TQFP-64 Pin No.	CY7C53120L8 SOIC-32 Pin No.	CY7C53120L8 TQFP-44 Pin No.
CLK1	Input	**Oscillator connection or external clock input**.	35	24	15	15
CLK2	Output	**Oscillator connection**. Leave open when external clock is input to CLK1. Maximum of one external load.	34	23	14	14
RESET	I/O (Built-In Pull-up)	**Reset pin (active LOW)**. Note. The allowable external capacitance connected to the RESET pin is 100–1000 pF.	7	6	1	40
SERVICE	I/O (Built-In Configurable Pull-up)	**Service pin (active LOW)**. Alternates between input and output at a 76-Hz rate.	30	17	8	5
IO0–IO3	I/O	**Large current-sink capacity (20 mA)**. General I/O port. The output of timer/ counter 1 may be routed to IO0. The output of timer/counter 2 may be routed to IO1.	2, 3, 4, 5	2, 3, 4, 5	7, 6, 5, 4	4, 3, 2, 43

Pin Descriptions (continued)

Pin Name	I/O	Pin Function	CY7C53150L TQFP-100 Pin No.	CY7C53150L TQFP-64 Pin No.	CY7C53120L8 SOIC-32 Pin No.	CY7C53120L8 TQFP-44 Pin No.
IO4–IO7	I/O (Built-In Configurable Pull-ups)	**General I/O port**. The input to timer/counter 1 may be derived from one of IO4–IO7. The input to timer/counter 2 may be derived from IO4.	12, 13, 14, 19	10, 11, 12, 13	3, 30, 29, 28	42, 36, 35, 32
IO8–IO10	I/O (Program-mable current drive)	**General I/O port**. May be used for serial communication under firmware control.	22, 25, 28	14, 15, 16	27, 26, 24	31, 30, 27
SS	Input	**Slave Select**. Muxed with IO7.	19	13	28	32
SCLK/RXD	I/O	**SPI Clock or SCI RXD**. Muxed with IO8. Can be configured as Open Drain Output.	22	14	27	31
MISO	I/O	**SPI Master In/Slave Out (MISO) Muxed with IO9**. Can be configured as Open Drain Output.	25	15	26	30
MOSI/TXD	I/O	**SPI Master out/Slave In (MOSI) or SCI TXD. Muxed with IO10**. Can be configured as Open Drain Output.	28	16	24	27
D0–D7	I/O	**Bidirectional memory data bus**.	66, 64, 62, 61, 59, 58, 56, 55	43, 42, 38, 37, 36, 35, 34, 33	N/A	N/A
$R/\overline{W}$	Output	**Read/write control output for external memory**.	68	45	N/A	N/A
$\overline{E}$	Output	**Enable clock control output for external memory**.	69	46	N/A	N/A
A0–A15	Output	**Memory address output port**.	98, 97, 96, 95, 94, 93, 91, 90, 86, 85, 83, 82, 80, 78, 76, 71	64, 63, 62, 61, 60, 59, 58, 57, 56, 55, 54, 53, 52, 51, 50, 47	N/A	N/A
V_{DD}	Input	**Power input (3.3V nom.)**. All V_{DD} pins must be connected together externally.	16, 21, 63, 88, 67	7, 20, 22, 40, 41, 44	2, 11, 12, 25, 32	9, 10, 29, 38, 41
V_{SS}	Input	**Power input (0V, GND)**. All V_{SS} pins must be connected together externally.	6, 15, 26, 75, 100	8, 19, 21, 39	9, 13, 23, 31	7, 13, 26, 37
CV_{DD} [4]	Input	**Power input, 5V or 3.3V depending on Communications Port Voltage**.	37	26	18	19
CV_{SS}	Input	**Power input** (0V GND).	51	25	16	16
V_{PP}	Input	**In-circuit test mode control**. If V_{PP} is high when $\overline{RESET}$ is asserted, the I/O, address and data buses become Hi-Z.	11	9	10	8

Note:
4. In case the Comm port is used at 5V, CV_{DD} = 5V can not be applied before V_{DD} has stabilized.

Pin Descriptions (continued)

Pin Name	I/O	Pin Function	CY7C53150L TQFP-100 Pin No.	CY7C53150L TQFP-64 Pin No.	CY7C53120L8 SOIC-32 Pin No.	CY7C53120L8 TQFP-44 Pin No.
CP0–CP4	Communication Network Interface	**Bidirectional port supporting communications in three modes**.	41, 43, 46, 49, 53	28, 29, 30, 31, 32	19, 20, 17, 21, 22	20, 21, 18, 24, 25
NC	–	**No connect**. Must not be connected on the user's PC board, since they may be connected internal to the chip.	1, 8, 9, 10, 17, 18, 20, 23, 24, 27, 29, 31, 32, 33, 36, 38, 39, 40, 42, 44, 45, 47, 48, 50, 52, 54, 57, 60, 65, 70, 72, 73, 74, 77, 79, 81, 84, 87, 89, 92, 99	1, 18, 27, 48, 49	–	1, 6, 11, 12, 17, 22, 23, 28, 33, 34, 39, 44

Memory Usage

All Neuron chips require system firmware to be present when they are powered up. In the case of the CY7C53120L8, this firmware is preprogrammed in the factory in an on-chip ROM. In the case of the CY7C53150L, the system firmware must be present in the first 16 KB of an off-chip nonvolatile memory such as Flash, EPROM, EEPROM, or NVRAM. Because the system firmware implements the network protocol, it cannot itself be downloaded over the network.

For the CY7C53120L8, the user application program is stored in on-chip Flash memory. It may be programmed using a device programmer before board assembly, or may be programmed in-circuit after board assembly through a proprietary 10-pin programming interface or over the LonTalk network from an external network management tool.

For the CY7C53150L, the user application program is stored in on-chip Flash Memory and also in off-chip memory. The user program may initially be programmed into the off-chip memory device using a device programmer.

Flash Memory Retention and Endurance

Data and code stored in Flash Memory is guaranteed to be retained for at least ten years for programming temperature range of –40°C to 85°C.

The Flash memory can typically be written 100,000 times without any data loss[5]. An erase/write cycle takes 20 ms. The system firmware extends the effective endurance of the Flash memory in two ways. If the data being written to a byte of Flash memory is the same as the data already present in that byte, the firmware does not perform the physical write. So for example, an application that sets its own address in Flash memory after every reset will not use up any write cycles if the address has not changed. In addition, system firmware version 13 or higher is able to aggregate writes to eight successive address locations into a single write for CY7C53120L8 devices. For example, if eight KB of code is downloaded over the network, the firmware would execute only 1024 writes rather than 8,192.

Note:
5. For detailed information about data retention after 100K cycles, please see Cypress qualification report.

Ability to switch to fast programming is provided if an LVI trip occurs while programming the flash. This improves the reliability of the chip in case of sudden power failure.

Low-Voltage Inhibit (LVI) Operation

The on-chip Low-voltage Inhibit circuit trips the Neuron chip reset circuit whenever the V_{DD} input drops below a programmable value between 2.7V and 3.05V. The purpose of this feature is to prevent the corruption of nonvolatile memory during voltage drops.

The default value of the LVI trip point is 2.7V. A lower value of trip point voltage decreases the likelihood of the LVI tripping due to noise on V_{DD}. A lower setting is therefore recommended for circuits with a lot of noise on the power supply. In circuits that do not have excessive noise it is recommended that the LVI trip point be increased which results in better flash protection in case of real power loss scenarios.

The LVI also features a programmable digital filter used to filter out V_{DD} noise. This is another method of decreasing the possibility of the LVI being triggered by the noise as opposed to true power loss events. The digital filter is programmed to a value between 16 and 128 clock cycles. The value chosen depends on the frequency of the V_{DD} noise where the digital filter period should slightly exceed the minimum frequency noise seen on V_{DD}. The LVI digital filter defaults to 128 clock cycles.

Reset Stretching

At Power-on, the CY7C53120L8/3150L provides internal Reset Stretching of 50ms minimum at 10MHz clock frequency. Power-on Reset Stretch time scale with frequency. After Power-on, Reset Stretch is 50ms independent of frequency of operation. At Power-on the CY7C53120L8/3150L defaults to Reset Stretch enabled. The Reset Stretch can either be left enabled or disabled through software. Reset Stretching eliminates the need for an external pulse stretching LVI which is required when using the 3150L with an external Flash memory.

Hardware Serial Communication (SPI/SCI) Engine

The CY7C53120L8/3150L features a hardware Serial Communication Engine. The hardware engine is capable of performing high-speed communications in either SPI or SCI more.

Serial Peripheral Interface (SPI) Mode

SPI mode is 4-pin synchronous serial communications interface that can be set as either a Master or a Slave.

SPI Pin Definition

Pin	Function
IO7	Slave Select (SS)
IO8	Hardware SPI Serial Clock (SPSCK)
IO9	Master Input/Slave Output (MISO)
IO10	Master Output/Slave Input (MOSI)

SPI communication is a point-to-point or point-to-multi-point interface that can be configured as master/slave, single-master/multiple-slaves or multiple-masters/single-slave. The master initiates all communication between slave and master. The master drives the SPSCK signal, which is a clock used to synchronize all data communication between master and slave.

Slave Select (SS) is an input to the Neuron chip in both the Master and the Slave modes. In Slave mode, SS is active low with the Slave communicating only when SS is low. In Master mode, the SPI engine functions only when the SS signal is held high. SS can be hard wired high or low or it can be wired to signals being generated from other sources. The Neuron Chip can use IO0 through IO6 for selecting between multiple slaves when acting as a master.

MOSI and MISO are used to send and receive data over SPI. MOSI is a data output in Master mode and is an input in Slave mode. MISO is an input in Master mode and is an output in Slave mode. The phase and polarity of the data relative to the clock signal is programmable and can be configured in four possible modes.

The SPI interface can communicate at a maximum 2.5-Mbps data rate (10-MHz input clock frequency). The data rate is programmable and can be scaled by selecting the desired divisor ranging from 2 to 256 in multiples of 2.

Serial Communication Interface (SCI) Mode

SCI mode provides a full-duplex asynchronous NRZ format serial interface for communicating with other devices with either an SCI or UART interface. The SCI interface is optimized to provide industry standard UART baud rates from the CY7C53120L8/3150L crystal clock rates.

SCI Pin Definitions

Pin	Function
IO8	Receive Data (RXD)
IO10	Transmit Data (TXD)

RXD is used to receive serial data at the specified baud rate. TXD is used to transmit data serially at the specified baud rate. The idle state of the TXD and RXD lines is high. All data bytes begin with a start bit which is a '0'; this is followed by eight or nine bits of data, LSB first, and end with a stop bit which is a return to the idle state of '1.' The number of bits transmitted or received is programmable between eight or nine bits. The ninth bit can be used as a parity bit or as a second stop bit.

The maximum baud rate for the SCI engine is 460.8 Kbaud (10-MHz input clock frequency). The SCI can be programmed to run at most standard UART baud rate values.

Communications Port

The Neuron chip includes a versatile 5-pin communications port that can be configured in three different ways. The Communications port can operate at either 3.3V or 5V. The Communication port can be made backward-compatible with existing 5V transceivers by supplying a 5V supply to the CV_{DD} pin.

In Single-ended Mode, pin CP0 is used for receiving serial data, pin CP1 for transmitting serial data, and pin CP2 enables an external transceiver. Data is communicated using Differential Manchester encoding.

In Special Purpose Mode, pin CP0 is used for receiving serial data, pin CP1 for transmitting serial data, pin CP2 transmits a bit clock, and pin CP4 transmits a frame clock for use by an external intelligent transceiver. In this mode, the external transceiver is responsible for encoding and decoding the data stream.

In Differential Mode, pins CP0 and CP1 form a differential receiver with built-in programmable hysteresis and low-pass filtering. Pins CP2 and CP3 form a differential driver. Serial data is communicated using Differential Manchester encoding.

The following tables describe the communications port when used in Differential Mode.
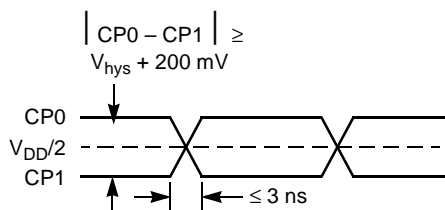
$\left| CP0 - CP1 \right| \geq$
$V_{hys} + 200$ mV

Figure 1. Receiver Input Waveform

Programmable Hysteresis Values (3.3V) (Expressed as differential peak-to-peak voltages in terms of V_{DD})

Hysteresis[6]	V_{hys} Min.	V_{hys} Typ.	V_{hys} Max.
0	0.019 V_{DD}	0.027 V_{DD}	0.035 V_{DD}
1	0.038 V_{DD}	0.054 V_{DD}	0.070 V_{DD}
2	0.057 V_{DD}	0.081 V_{DD}	0.105 V_{DD}
3	0.076 V_{DD}	0.108 V_{DD}	0.140 V_{DD}
4	0.095 V_{DD}	0.135 V_{DD}	0.175 V_{DD}
5	0.114 V_{DD}	0.162 V_{DD}	0.210 V_{DD}
6	0.133 V_{DD}	0.189 V_{DD}	0.245 V_{DD}
7	0.152 V_{DD}	0.216 V_{DD}	0.280 V_{DD}

Programmable Hysteresis Values (5V) (Expressed as differential peak-to-peak voltages in terms of V_{DD})

Hysteresis[6]	V_{hys} Min.	V_{hys} Typ.	V_{hys} Max.
0	0.019 V_{DD}	0.027 V_{DD}	0.035 V_{DD}
1	0.040 V_{DD}	0.054 V_{DD}	0.068 V_{DD}
2	0.061 V_{DD}	0.081 V_{DD}	0.101 V_{DD}
3	0.081 V_{DD}	0.108 V_{DD}	0.135 V_{DD}
4	0.101 V_{DD}	0.135 V_{DD}	0.169 V_{DD}
5	0.121 V_{DD}	0.162 V_{DD}	0.203 V_{DD}
6	0.142 V_{DD}	0.189 V_{DD}	0.236 V_{DD}
7	0.162 V_{DD}	0.216 V_{DD}	0.270 V_{DD}

Programmable Glitch Filter Values[7](Receiver (end-to-end) filter values expressed as transient pulse suppression times)

Filter (F)	Min.	Typ.	Max.	Unit
0	10	75	140	ns
1	120	410	700	ns
2	240	800	1350	ns
3	480	1500	2600	ns

Receiver[8] **(End-to-End) Absolute Asymmetry** (Worst-case across hysteresis)

Filter (F)	Max ($\left| t_{PLH} - t_{PHL} \right|$)	Unit
0	35	ns
1	150	ns
2	250	ns
3	400	ns

Differential Receiver (End-to-End) Absolute Symmetry[9, 10]

Filter (F)	Hysteresis (H)	Max ($\left| t_{PLH} - t_{PHL} \right|$)	Unit
0	0	24	ns

Electrical Characteristics (V_{DD} = 3.0V–3.6V)

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V
V_{IL}	Input Low Voltage IO0–IO10, CP0, CP3, CP4, $\overline{SERVICE}$, D0-D7, $\overline{RESET}$ CP0, CP1 (Differential)	— —	— —	0.8 Programmable	V
V_{IH}	Input High Voltage IO0–IO10, CP0, CP3, CP4, $\overline{SERVICE}$, D0-D7, $\overline{RESET}$ CP0, CP1 (Differential)	2.0 Programmable	— —	— —	V
V_{OL}	Low-Level Output Voltage I_{out} < 20 µA Standard Outputs (I_{OL} = 1.4 mA)[11] High Sink (IO0–IO3), $\overline{SERVICE}$, $\overline{RESET}$ (I_{OL} = 20 mA) High Sink (IO0–IO3), $\overline{SERVICE}$, RESET (I_{OL} = 10 mA) Maximum Sink (CP2, CP3) (I_{OL} = 40 mA) Maximum Sink (CP2, CP3) (I_{OL} = 15 mA)	— — — — — —	— — — — — —	0.1 0.4 0.8 0.4 1.0 0.4	V

Notes:
6. Hysteresis values are on the condition that the input signal swing is 200 mV greater than the programmed value.
7. Must be disabled if data rate is 1.25 Mbps or greater.
8. Receiver input, $V_D = V_{CP0} - V_{CP1}$, at least 200 mV greater than hysteresis levels. See *Figure 1*.
9. CP0 and CP1 inputs each 0.60 Vp – p, 1.25 MHz sine wave 180° out of phase with each other as shown in *Figure 8*. V_{DD} = 5.00 V ± 5% (V_{DD} = 3.30 V ± 5%).
10. t_{PLH}: Time from input switching states from low to high to output switching states. t_{PHL}: Time from input switching states from high to low to output switching states.

PRELIMINARY

Electrical Characteristics $(V_{DD} = 3.0V–3.6V)$ (continued)

V_{OH}	High-Level Output Voltage				V
	$I_{out} < 20$ μA	$V_{DD} - 0.1$	—	—	
	Standard Outputs $(I_{OH} = -1.4$ mA)[11]	$V_{DD} - 0.4$	—	—	
	High Sink (IO0 – IO3), $\overline{SERVICE}$ $(I_{OH} = -1.4$ mA)	$V_{DD} - 0.4$	—	—	
	Maximum Source (CP2, CP3) $(I_{OH} = -40$ mA)	$V_{DD} - 1.0$	—	—	
	Maximum Source (CP2, CP3) $(I_{OH} = -15$ mA)	$V_{DD} - 0.4$	—	—	
V_{hys}	Hysteresis (Excluding CLK1)	175	—	—	mV
I_{in}	Input Current (Excluding Pull-Ups) $(V_{SS}$ to $V_{DD})$[12]	—	—	±10	μA
I_{pu}	Pull-Up Source Current $(V_{out} = 0$ V, Output = High-Z)[12]	60	—	260	μA
I_{DD}	Operating Mode Supply Current[13]				mA
	20-MHz Clock	—	—	21	
	10-MHz Clock	—	—	13	
	5-MHz Clock	—	—	8	
	2.5-MHz Clock	—	—	5	
	1.25-MHz Clock	—	—	3	
	0.625-MHz Clock[14]	—	—	2	
$I_{DDsleep}$	Sleep Mode Supply Current[13]	—	—	10	μA

LVI Trip Point (V_{DD})

Part Number	Min.		Max.	Unit
CY7C53120L8, and CY7C53150L	2.7	Programmable	3.05	V

External Memory Interface Timing — CY7C53150L, $V_{DD} \pm 10\%$ $(V_{DD} = 3.0V$ to 3.6 V, $T_A = -40°C$ to+ 85°C)[1]

Parameter	Description	Min.	Max.	Unit
t_{cyc}	Memory Cycle Time (System Clock Period)[15]	200	3200	ns
PW_{EH}	Pulse Width, $\overline{E}$ High[16]	$t_{cyc}/2 - 5$	$t_{cyc}/2 + 5$	ns
PW_{EL}	Pulse Width, $\overline{E}$ Low[16]	$t_{cyc}/2 - 5$	$t_{cyc}/2 + 5$	ns
t_{AD}	Delay, $\overline{E}$ High to Address Valid	—	35	ns
t_{AH}	Address Hold Time After $\overline{E}$ High	10	—	ns
t_{RD}	Delay, $\overline{E}$ High to R/$\overline{W}$ Valid Read	—	25	ns
t_{RH}	R/$\overline{W}$ Hold Time Read After $\overline{E}$ High	5	—	ns
t_{WR}	Delay, $\overline{E}$ High to R/$\overline{W}$ Valid Write	—	25	ns
t_{WH}	R/$\overline{W}$ Hold Time Write After $\overline{E}$ High	5	—	ns
t_{DSR}	Read Data Setup Time to $\overline{E}$ High	15	—	ns
t_{DHR}	Data Hold Time Read After $\overline{E}$ High	0	—	ns
t_{DHW}	Data Hold Time Write After $\overline{E}$ High[17, 18]	10	—	ns
t_{DDW}	Delay, $\overline{E}$ Low to Data Valid	—	12	ns
t_{DHZ}	Data Three State Hold Time After $\overline{E}$ Low[19]	0	—	ns
t_{DDZ}	Delay, $\overline{E}$ High to Data Three-State[18]	—	42	ns
t_{acc}	External Memory Access Time $(t_{acc} = t_{cyc} - t_{AD} - t_{DSR})$ at 10-MHz input clock	150	—	ns

Notes:
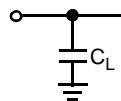11. Standard outputs are IO4–IO10, CP0, CP1, and CP4. ($\overline{RESET}$ is an open drain input/output. CLK2 must have $\leq$ 15 pF load.) For CY7C53150L, standard outputs also include A0–A15, D0–D7, $\overline{E}$, and R/$\overline{W}$.
12. IO4–IO7 and $\overline{SERVICE}$ have configurable pull-ups. $\overline{RESET}$ has a permanent pull-up.
13. Supply current measurement conditions: $V_{DD} = 3.3V$, all outputs under no-load conditions, all inputs $\leq 0.2V$ or $\geq (V_{DD} - 0.2V)$, configurable pull-ups off, crystal oscillator clock input, differential receiver disabled. The differential receiver adds approximately 200 μA typical and 600 μA maximum (at 5V) when enabled. It is enabled on either of the following conditions:
    • Neuron Chip in Operating mode **and** Comm Port in Differential mode.
    • Neuron Chip in Sleep mode **and** Comm Port in Differential mode **and** Comm Port Wake-up not masked.
14. Supported through an external oscillator only.
15. $t_{cyc} = 2(1/f)$, where f is the input clock (CLK1) frequency (10, 5, 2.5, 1.25, or 0.625 MHz).
16. Refer to *Figure 3* for detailed measurement information.
17. The data hold parameter, t_{DHW}, is measured to the disable levels shown in *Figure 4*, rather than to the traditional data invalid levels.
18. Refer to *Figure 5* and *Figure 4* for detailed measurement information.

Differential Transceiver Electrical Characteristics

Characteristic at 3.3V	Min.	Max.	Unit
Receiver Common Mode Voltage Range to maintain hysteresis[20]	0.6	$V_{DD} - 1.5$	V
Receiver Common Mode Range to operate with unspecified hysteresis	0.4	$V_{DD} - 1.3$	V
Input Offset Voltage	$-0.05V_{hys} - 35$	$0.05V_{hys} + 35$	mV
Propagation Delay (F = 0, $V_{ID} = V_{hys}/2 + 200$ mV)	—	230 ns	ns
Input Resistance	5	—	MΩ
Wake-up Time	—	10	μs
Differential Output Impedance for CP2 and CP3[21]		35	Ω

Characteristic at 5V	Min.	Max.	Unit
Receiver Common Mode Voltage Range to maintain hysteresis[20]	1.2	$V_{DD} - 2.2$	V
Receiver Common Mode Range to operate with unspecified hysteresis	0.9	$V_{DD} - 1.75$	V
Input Offset Voltage	$-0.05V_{hys} - 35$	$0.05V_{hys} + 35$	mV
Propagation Delay (F = 0, $V_{ID} = V_{hys}/2 + 200$ mV)	—	230 ns	ns
Input Resistance	5	—	MΩ
Wake-up Time	—	10	μs
Differential Output Impedance for CP2 and CP3[21]		35	Ω

TEST SIGNAL

C_L = 20 pF for $\overline{E}$
C_L = 30 pF for A0–A15, D0–D7, and R/$\overline{W}$
C_L = 50 pF for all other signals

Figure 2. Signal Loading for Timing Specifications Unless Otherwise Specified
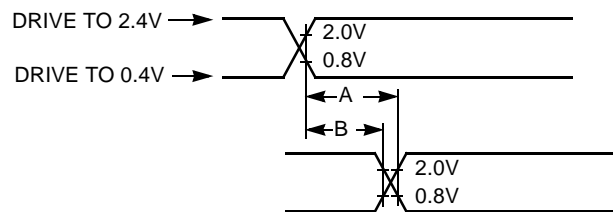
PW_{EH}
2.0V
PW_{EL}
2.0V
0.8V
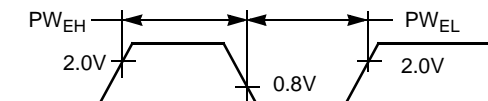
Figure 3. Test Point Levels for $\overline{E}$ Pulse Width Measurements

DRIVE TO 2.4V
DRIVE TO 0.4V
2.0V
0.8V
A
B
2.0V
0.8V

A — Signal valid-to-signal valid specification (maximum or minimum)
B — Signal valid-to-signal invalid specification (maximum or minimum)

Figure 4. Drive Levels and Test Point Levels for Timing Specifications Unless Otherwise Specified

Notes:
19. The three-state condition is when the device is not actively driving data. Refer to *Figure 2* and *Figure 5* for detailed measurement information.
20. Common mode voltage is defined as the average value of the waveform at each input at the time switching occurs.
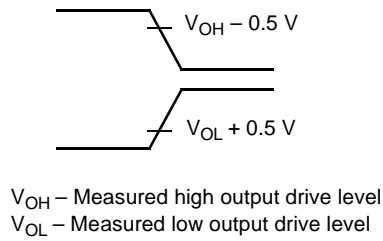21. $Z_0 = |V[CP2]–V[CP3]|/40$ mA for $3.15 \leq V_{DD} \leq 3.45V$.

$V_{OH} - 0.5\ V$

$V_{OL} + 0.5\ V$

V_{OH} – Measured high output drive level
V_{OL} – Measured low output drive level

Figure 5. Test Point Levels for Driven-to-Three-State Time Measurements

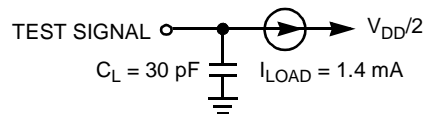TEST SIGNAL $\circ$ $V_{DD}/2$

$C_L = 30\ pF$ $I_{LOAD} = 1.4\ mA$

Figure 6. Signal Loading for Driven-to-Three-State Time Measurements
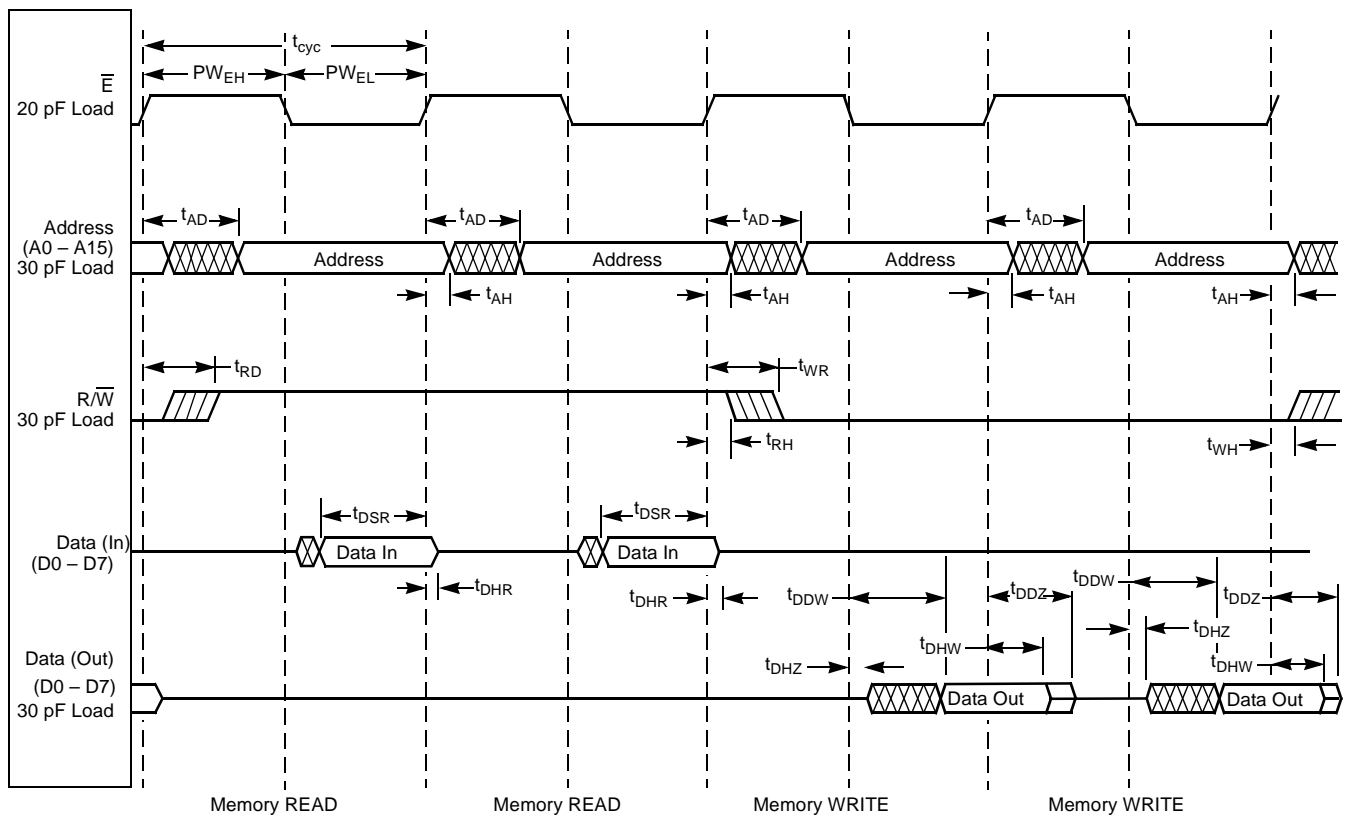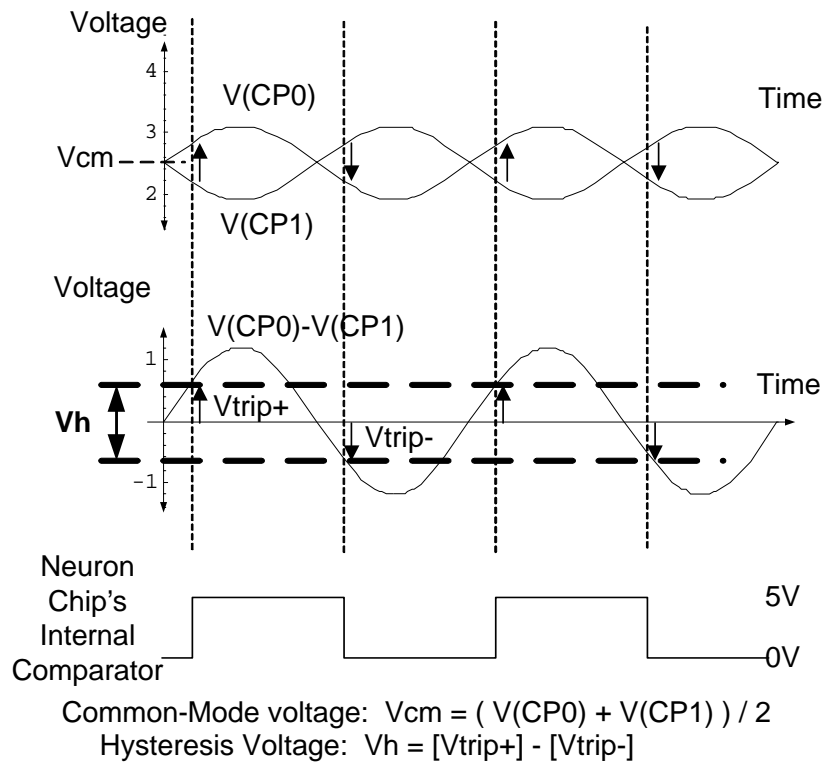

Figure 7. External Memory Interface Timing Diagram

Common-Mode voltage: Vcm = (V(CP0) + V(CP1)) / 2
Hysteresis Voltage: Vh = [Vtrip+] - [Vtrip-]

Figure 8. Differential Receiver Input Hysteresis Voltage Measurement Waveforms for 5V Operation

Common-Mode voltage: Vcm = (V(CP0) + V(CP1)) / 2
Hysteresis Voltage: Vh = [Vtrip+] - [Vtrip-]
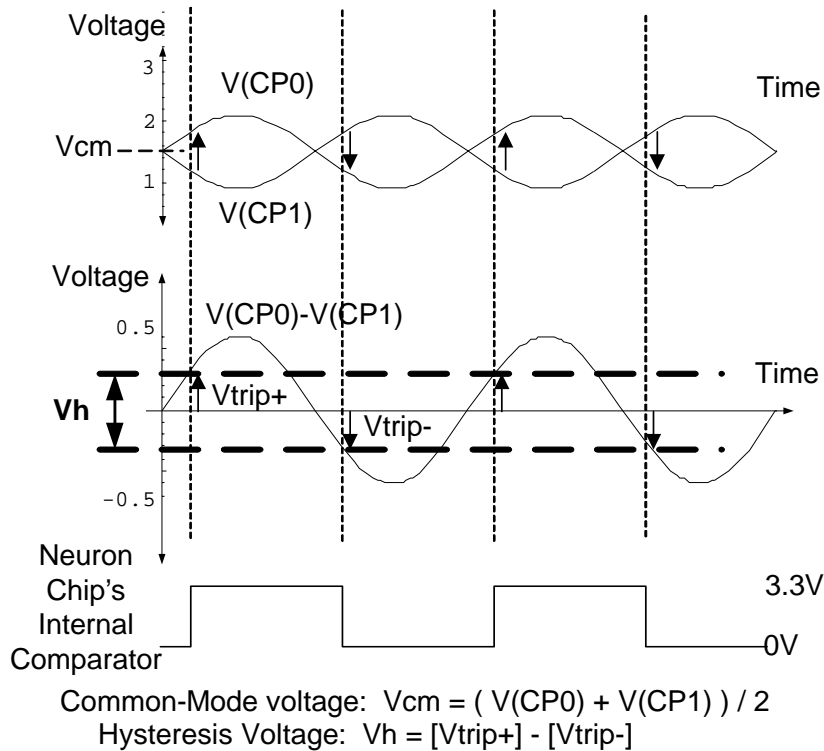
Figure 9. Differential Receiver Input Hysteresis Voltage Measurement Waveforms for 3.3V Operation

Ordering Information

Part Number	Flash (KB)	ROM (KB)	SRAM (KB)	Max. Input Clock (MHz)	Package Name	Package Type
CY7C53150L-64AI	0.5	0	4	20	A65	64-lead Thin Plastic Quad Flat Pack
CY7C53150L-100AI	0.5	0	4	20	A100	100-lead Thin Plastic Quad Flat Pack
CY7C53120L8-32SI	8	12	4	20	S34	32-lead (450 mil) Molded SOIC
CY7C53120L8-44AI	8	12	4	20	A44	44-lead Thin Plastic Quad Flat Pack

Package Diagrams

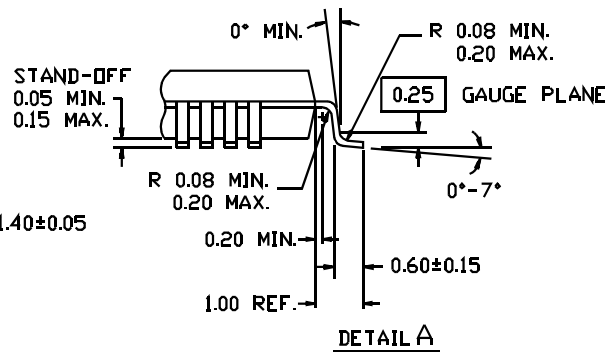**100-pin Thin Plastic Quad Flat Pack (TQFP) A100**
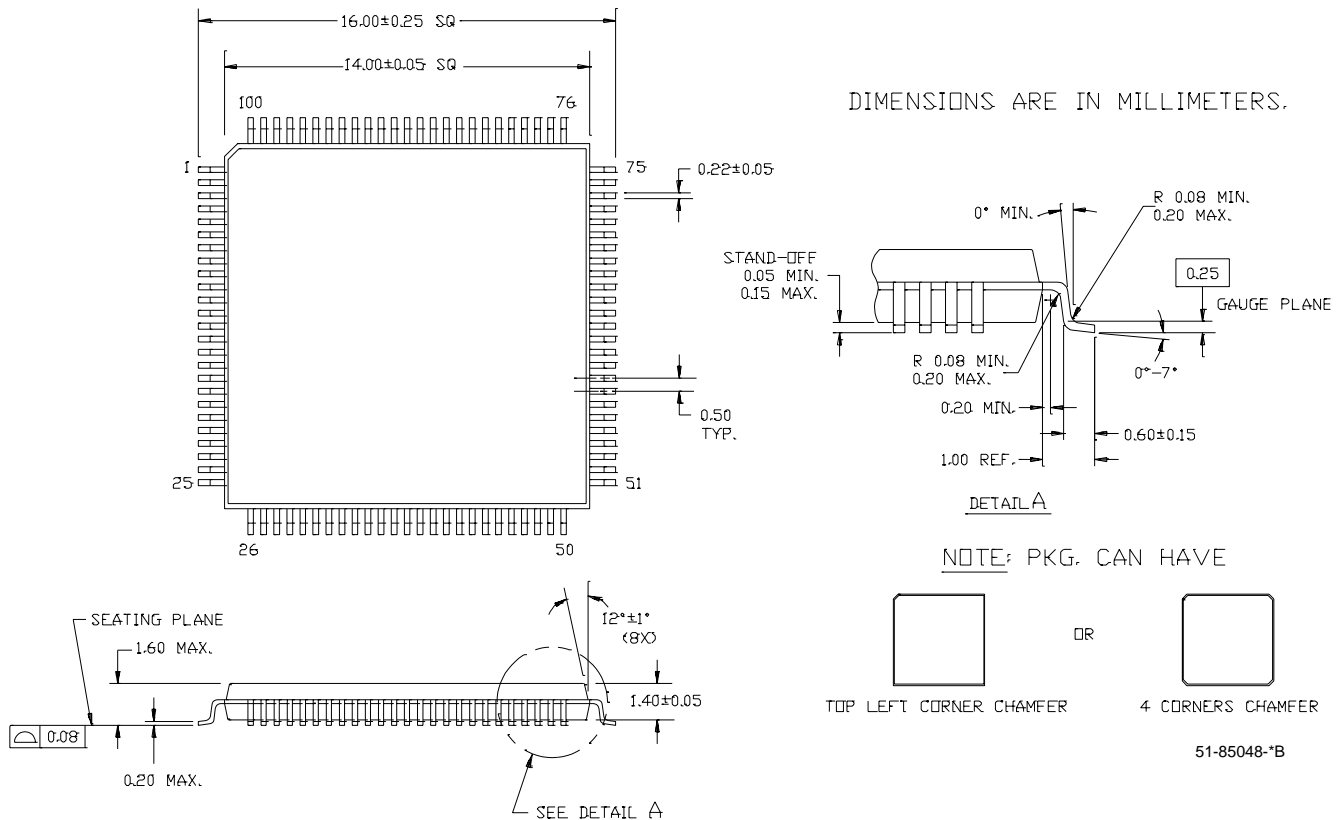
51-85048-*B

Package Diagrams (continued)

64-lead Thin Plastic Quad Flat Pack (14 x 14 x 1.4 mm) A65
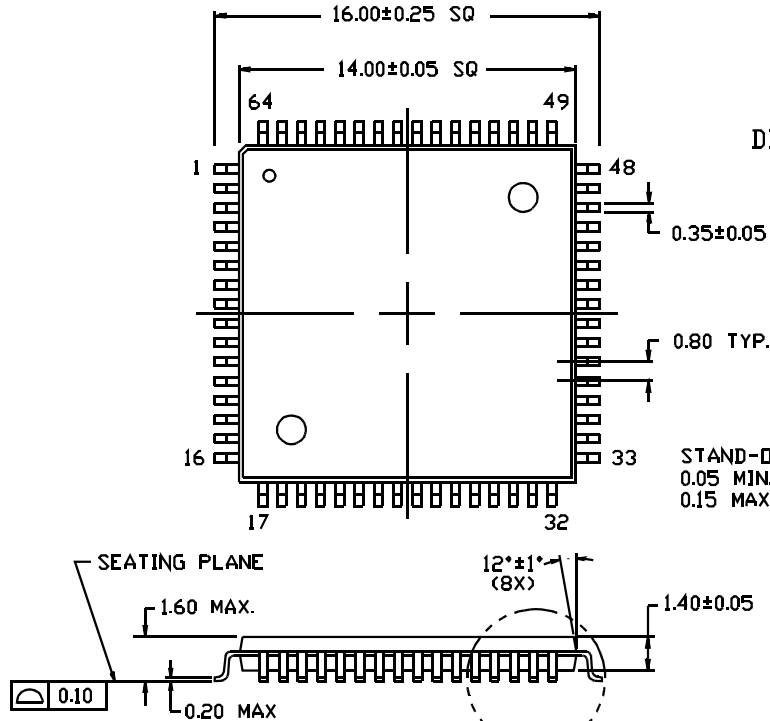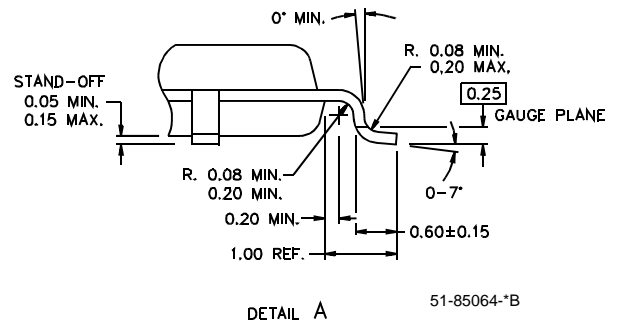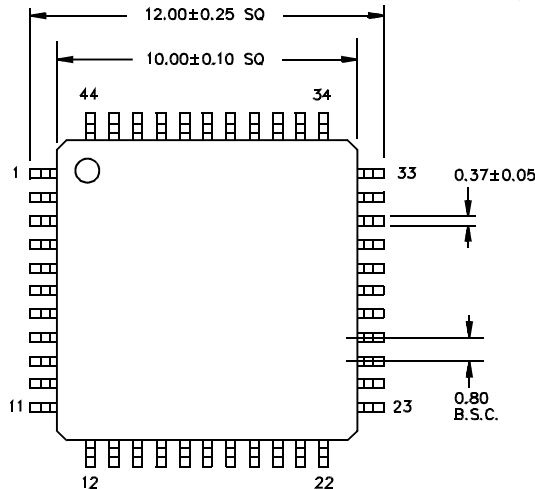
DIMENSIONS ARE IN MILLIMETERS

DETAIL A

51-85046-*B

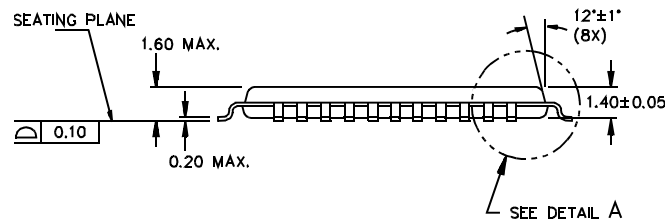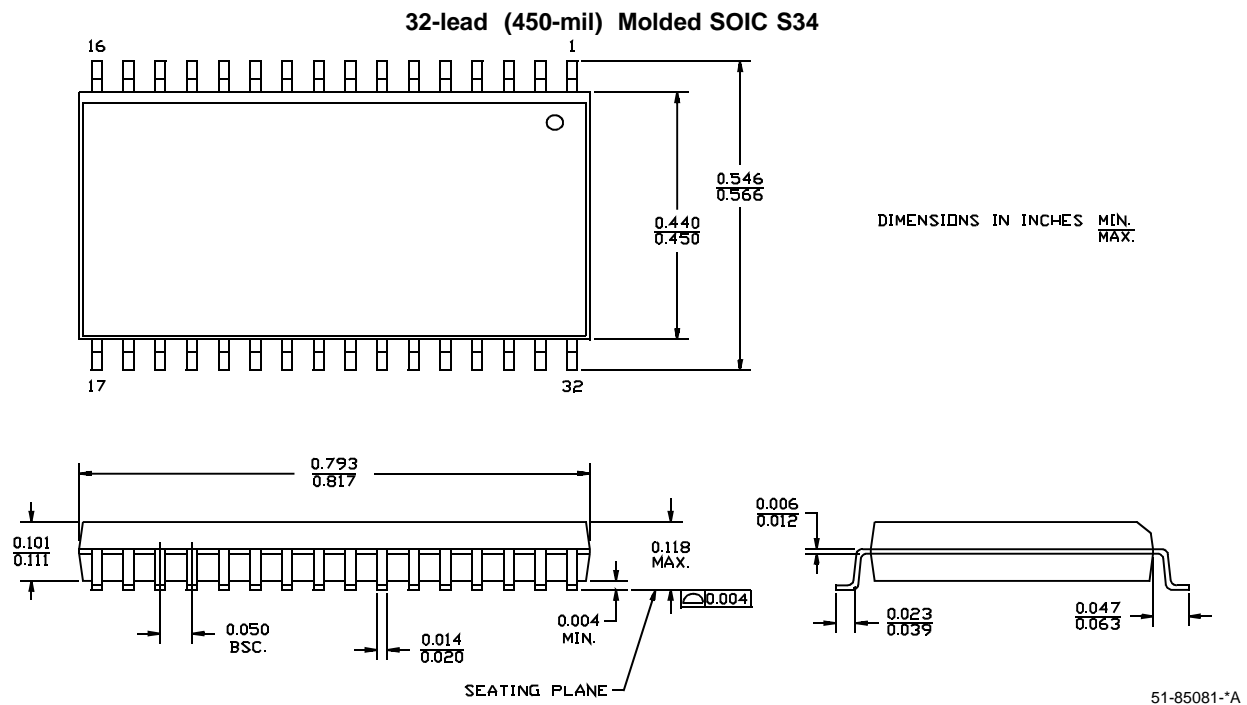### 44-lead Thin Plastic Quad Flat Pack A44

DIMENSIONS ARE IN MILLIMETERS

DETAIL A

51-85064-*B

Package Diagrams (continued)

32-lead (450-mil) Molded SOIC S34

DIMENSIONS IN INCHES MIN.
                      ————
                      MAX.

$\frac{0.546}{0.566}$

$\frac{0.440}{0.450}$

$\frac{0.793}{0.817}$

$\frac{0.101}{0.111}$

0.118 MAX.

0.004 MIN.

0.050 BSC.

$\frac{0.014}{0.020}$

⌒ 0.004

SEATING PLANE

$\frac{0.006}{0.012}$

$\frac{0.023}{0.039}$

$\frac{0.047}{0.063}$

51-85081-*A

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Document History Page

Document Title: CY7C53150L/CY7C53120L8 3.3V Neuron® Chip Network Processor Document Number: 38-10002				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	121963	12/12/02	PVO	New Data Sheet
*A	123762	03/03/03	PVO	Changed Advance Information to Preliminary Added information on LVI, SCI/SPI, Reset Stretching Corrected values of ROM, Hysteresis, and I_{PU} Added 100-pin TQFP pin definitions Made minor corrections to grammar and formatting
*B	125311	03/21/03	KBO	Add information on Power Sequence Corrected values of ROM Added default values of LVI, LVI filter and SPI divisor. Corrected I_{pu} Current limit values Clarified Reset Stretch times Corrected pin definitions (pins 10 to 14) on 100pin TQFP diagram Added Theta-JA value for the 100-pin TQFP package Changed part numbers to CY7C53120L8 / CY7C53150L Added ordering information table