

# MC10EP32, MC100EP32

## 3.3 V / 5 V ECL ÷ 2 Divider

### Description

The MC10/100EP32 is an integrated ÷2 divider with differential CLK inputs.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset allows for the synchronization of multiple EP32's in a system.

The 100 Series contains temperature compensation.

### Features

- 350 ps Typical Propagation Delay
- Maximum Frequency > 4 GHz Typical (Figure 3)
- PECL Mode Operating Range:
  - ♦  $V_{CC} = 3.0$  V to 5.5 V with  $V_{EE} = 0$  V
- NECL Mode Operating Range:
  - ♦  $V_{CC} = 0$  V with  $V_{EE} = -3.0$  V to -5.5 V
- Open Input Default State
- Safety Clamp on Inputs
- Q Output Will Default LOW with Inputs Open or at  $V_{EE}$
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



ON Semiconductor®

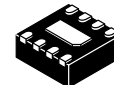
[www.onsemi.com](http://www.onsemi.com)



SOIC-8 NB  
D SUFFIX  
CASE  
751-07

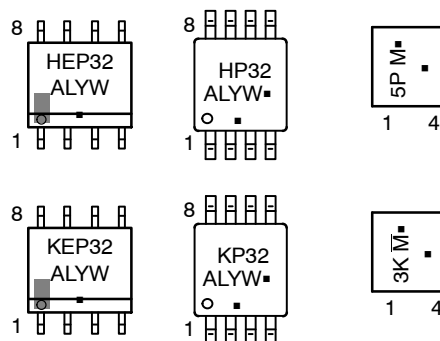


TSSOP-8  
DT SUFFIX  
CASE  
948R-02



DFN-8  
MN SUFFIX  
CASE 506AA

### MARKING DIAGRAMS\*



H = MC10	A = Assembly Location
K = MC100	L = Wafer Lot
5P = MC10	Y = Year
3K = MC100	W = Work Week
M = Date Code	▪ = Pb-Free Package

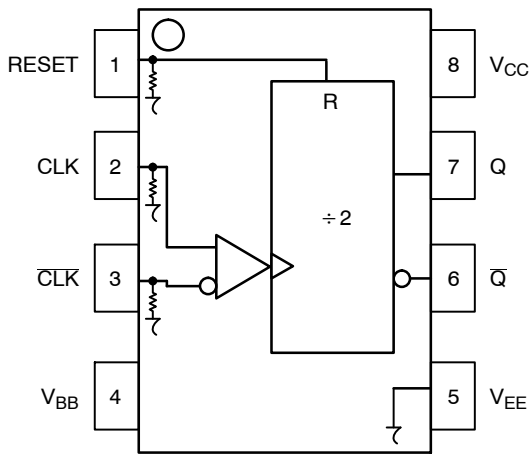
(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

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**Figure 1. 8-Lead Pinout (Top View) and Logic Diagram**

**Table 1. PIN DESCRIPTION**

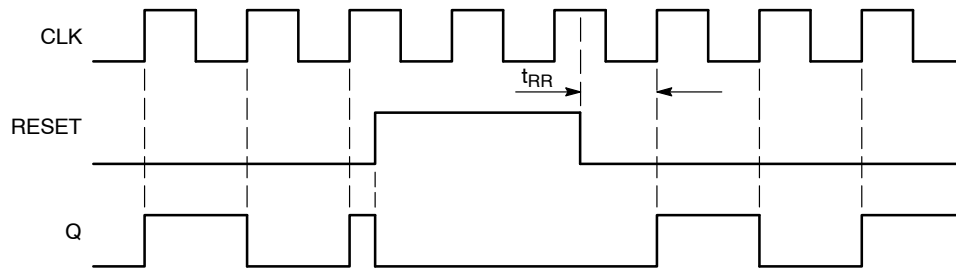
Pin	Function
CLK, $\overline{\text{CLK}}^*$	ECL Clock Inputs
Reset*	ECL Asynchronous Reset
$V_{\text{BB}}$	Reference Voltage Output
Q, $\overline{Q}$	ECL Data Outputs
$V_{\text{CC}}$	Positive Supply
$V_{\text{EE}}$	Negative Supply
EP	(DFN-8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

\*Pins will default LOW when left open.

**Table 2. TRUTH TABLE**

CLK	$\overline{\text{CLK}}$	RESET	Q	$\overline{Q}$
X	X	Z	L	H
Z	Z	L	F	F

Z = LOW to HIGH Transition  
 $\overline{Z}$  = HIGH to LOW Transition  
 F = Divide by 2 Function



**Figure 2. Timing Diagram**

**Table 3. ATTRIBUTES**

Characteristics	Value
Internal Input Pulldown Resistor	75 k $\Omega$
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	> 4 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb-Free Pkg
SOIC-8 NB TSSOP-8 DFN-8	Level 1 Level 3 Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	78 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note [AND8003/D](#).

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**Table 4. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		6	V
V <sub>EE</sub>	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		-6	V
V <sub>I</sub>	PECL Mode Input Voltage NECL Mode Input Voltage	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub> V <sub>I</sub> ≥ V <sub>EE</sub>	6 -6	V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			± 0.5	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-8 NB	190 130	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8 NB	41 to 44	°C/W
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8	185 140	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44	°C/W
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	DFN8	129 84	°C/W
T <sub>sol</sub>	Wave Solder (Pb-Free)	<2 to 3 sec @ 260°C		265	°C
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	(Note 1)	DFN8	35 to 40	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

**Table 5. 10EP DC CHARACTERISTICS, PECL** (V<sub>CC</sub> = 3.3 V, V<sub>EE</sub> = 0 V (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current	23	30	40	23	30	40	23	30	40	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 2)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
V <sub>OL</sub>	Output LOW Voltage (Note 2)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V <sub>IH</sub>	Input HIGH Voltage (Single-Ended)	2090		2415	2155		2480	2215		2540	mV
V <sub>IL</sub>	Input LOW Voltage (Single-Ended)	1365		1690	1430		1755	1490		1815	mV
V <sub>BB</sub>	Output Voltage Reference	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
V <sub>IHCMR</sub>	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	2.0		3.3	2.0		3.3	2.0		3.3	V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.3 V to -2.2 V.
2. All loading with 50 Ω to V<sub>CC</sub> - 2.0 V.
3. V<sub>IHCMR</sub> min varies 1:1 with V<sub>EE</sub>. V<sub>IHCMR</sub> max varies 1:1 with V<sub>CC</sub>. The V<sub>IHCMR</sub> range is referenced to the most positive side of the differential input signal.

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**Table 6. 10EP DC CHARACTERISTICS, PECL** ( $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	23	30	40	23	30	40	23	30	40	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	3865	3990	4115	3930	4055	4180	3990	4115	4240	mV
$V_{OL}$	Output LOW Voltage (Note 2)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	3790		4115	3855		4180	3915		4240	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	3065		3390	3130		3455	3190		3515	mV
$V_{BB}$	Output Voltage Reference	3490	3590	3690	3555	3655	3755	3615	3715	3815	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	2.0		5.0	2.0		5.0	2.0		5.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.
2. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 7. 10EP DC CHARACTERISTICS, NECL** ( $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	23	30	40	23	30	40	23	30	40	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	-1135	-1010	-885	-1070	-945	-820	-1010	-885	-760	mV
$V_{OL}$	Output LOW Voltage (Note 2)	-1935	-1810	-1685	-1870	-1745	-1620	-1810	-1685	-1560	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1210		-885	-1145		-820	-1085		-760	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1935		-1610	-1870		-1545	-1810		-1485	mV
$V_{BB}$	Output Voltage Reference	-1510	-1410	-1310	-1445	-1345	-1245	-1385	-1285	-1185	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .
2. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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**Table 8. 100EP DC CHARACTERISTICS, PECL** ( $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	23	30	37	26	34	40	28	36	42	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
$V_{OL}$	Output LOW Voltage (Note 2)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
$V_{BB}$	Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	2.0		3.3	2.0		3.3	2.0		3.3	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.
2. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 9. 100EP DC CHARACTERISTICS, PECL** ( $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	23	30	37	26	34	40	28	36	42	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
$V_{OL}$	Output LOW Voltage (Note 2)	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	3775		4120	3775		4120	3775		4120	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	3055		3375	3055		3375	3055		3375	mV
$V_{BB}$	Output Voltage Reference	3475	3575	3675	3475	3575	3675	3475	3575	3675	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	2.0		5.0	2.0		5.0	2.0		5.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.
2. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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**Table 10. 100EP DC CHARACTERISTICS, NECL** ( $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	23	30	37	26	34	40	28	36	42	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
$V_{OL}$	Output LOW Voltage (Note 2)	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1225		-880	-1225		-880	-1225		-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
$V_{BB}$	Output Voltage Reference	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .
2. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 11. AC CHARACTERISTICS** ( $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$  or  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OPP}$	Output Voltage Amplitude (See Figure 3) $f_{in} < 3.5\text{ GHz}$ $f_{in} @ 4.0\text{ GHz}$	640	700 740		630	700 710		500	700 600		mV
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Differential CLK to Q, $\bar{Q}$ 10 Series RESET to Q, $\bar{Q}$ 100 Series RESET to Q, $\bar{Q}$	250	330	420	270	350	450	320	400	480	ps
$t_{RR}$	Set/Reset Recovery	200	175		200	175		200	175		ps
$t_{PW}$	Minimum Pulse width RESET	550	475		550	475		550	475		ps
$t_{JITTER}$	CLOCK Random Jitter (RMS) $f_{in} < 3.5\text{ GHz}$ $f_{in} @ \leq 4.0\text{ GHz}$		0.5 0.5	1.5		0.5 0.5	1.5		0.5 0.5	1.5	ps
$V_{PP}$	Input Voltage Swing (Differential Configuration)	150	800	1200	150	800	1200	150	800	1200	mV
$t_r$ $t_f$	Output Rise/Fall Times Q, $\bar{Q}$ (20% – 80%)	50	100	150	70	120	170	70	130	200	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

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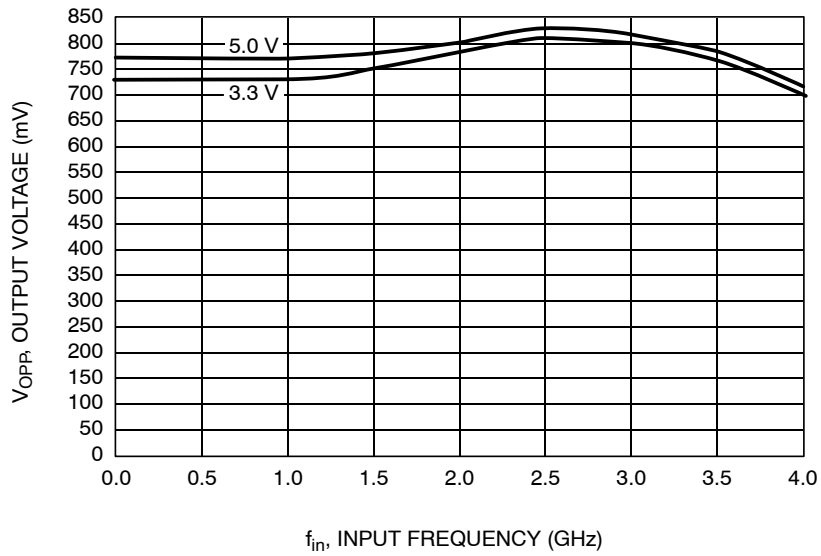


Figure 3. Input Frequency ( $f_{in}$ ) Versus Typical Output Voltage ( $V_{OPP}$ )

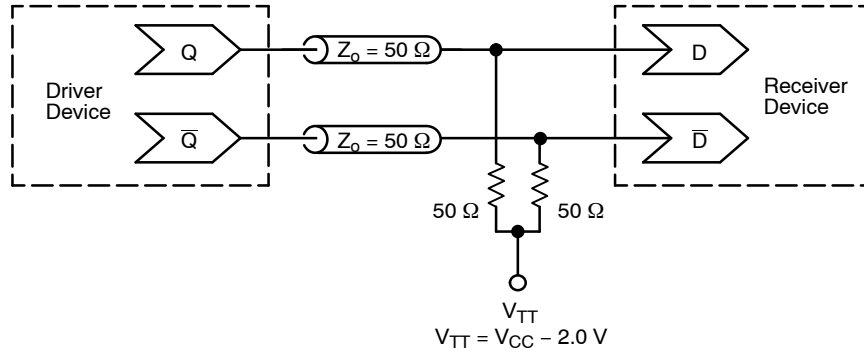


Figure 4. Typical Termination for Output Driver and Device Evaluation  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

# MC10EP32, MC100EP32

## ORDERING INFORMATION

Device	Package	Shipping†
MC10EP32DG	SOIC-8 NB (Pb-Free)	98 Units / Rail
MC10EP32DR2G	SOIC-8 NB (Pb-Free)	2500 / Tape & Reel
MC10EP32DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC10EP32DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC10EP32MNR4G	DFN-8 (Pb-Free)	1000 / Tape & Reel
MC100EP32DG	SOIC-8 NB (Pb-Free)	98 Units / Rail
MC100EP32DR2G	SOIC-8 NB (Pb-Free)	2500 / Tape & Reel
MC100EP32DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC100EP32DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC100EP32MNR4G	DFN-8 (Pb-Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

### Resource Reference of Application Notes

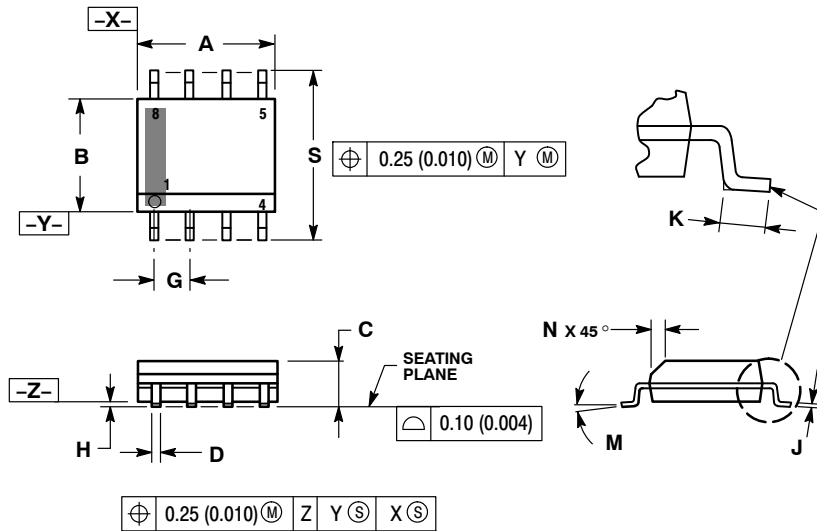
- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices



# MC10EP32, MC100EP32

## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AK

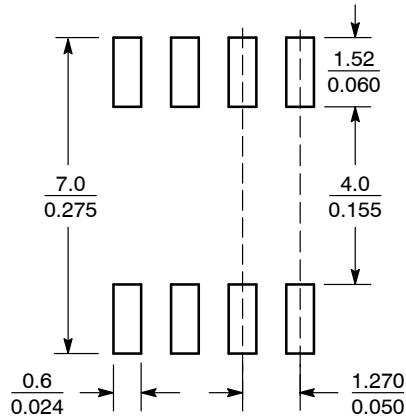


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



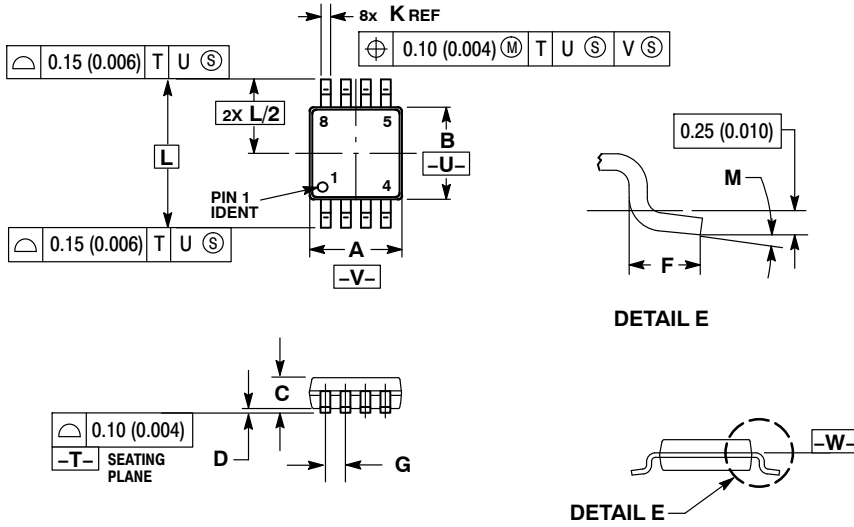
SCALE 6:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, [SOLDERRM/D](#).

# MC10EP32, MC100EP32

## PACKAGE DIMENSIONS

TSSOP-8  
CASE 948R-02  
ISSUE A



### NOTES:

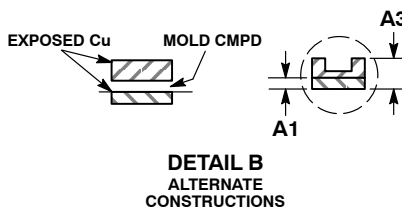
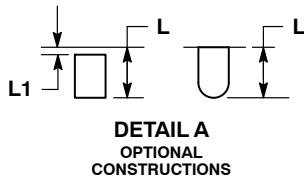
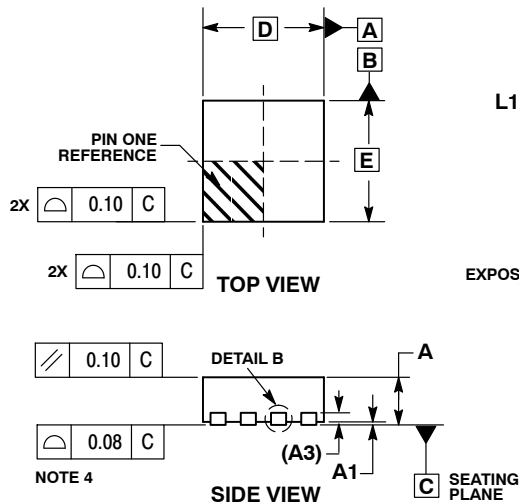
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

# MC10EP32, MC100EP32

## PACKAGE DIMENSIONS

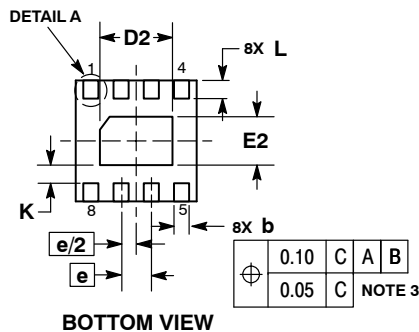
DFN-8 2x2, 0.5P  
CASE 506AA  
ISSUE F



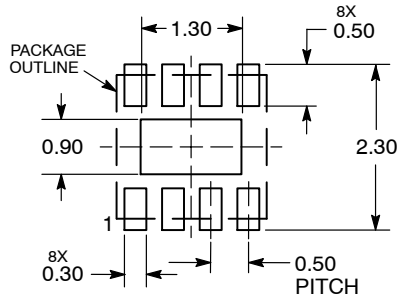
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.20	0.30
D	2.00	BSC
D2	1.10	1.30
E	2.00	BSC
E2	0.70	0.90
e	0.50	BSC
K	0.30	REF
L	0.25	0.35
L1	---	0.10



### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, [SOLDDRRM/D](#).

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