CY62167EV30 MoBL®

16-Mbit (1M × 16/2M × 8) Static RAM

Features

- TSOP I package configurable as 1M × 16 or 2M × 8 SRAM
- Very high speed: 45 ns
- Temperature ranges
  - Industrial: –40 °C to +85 °C
  - Automotive-A: –40 °C to +85 °C
- Wide voltage range: 2.20 V to 3.60 V
- Ultra-low standby power
  - Typical standby current: 1.5 µA
  - Maximum standby current: 12 µA
- Ultra-low active power
  - Typical active current: 2.2 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ Features
- Automatic power-down when deselected
- CMOS for optimum speed and power
- Offered in Pb-free 48-ball VFBGA and 48-pin TSOP I packages

Functional Description

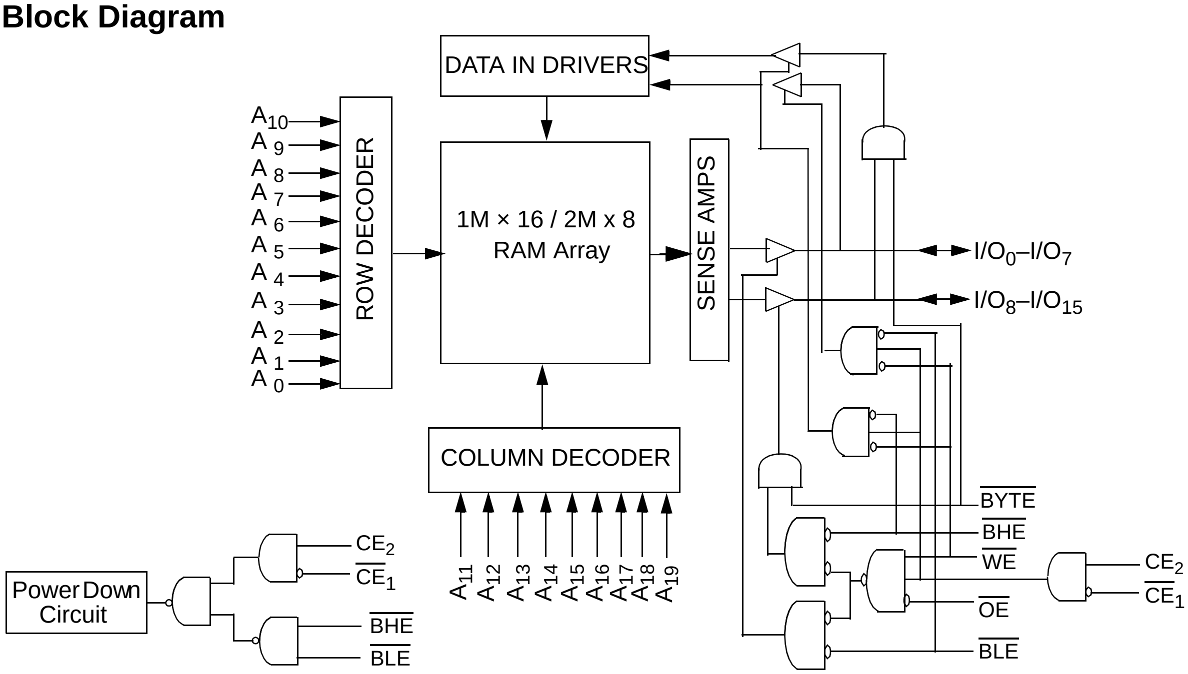
The CY62167EV30 is a high performance CMOS static RAM organized as 1M words by 16 bits or 2M words by 8 bits. This device features an advanced circuit design that provides an ultra low active current. Ultra low active current is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that reduces power consumption by 99 percent when addresses are not toggling. Place the device into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when: the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or a write operation is in progress ($\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW).

To write to the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{19}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from the I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{19}).

To read from the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See Truth Table on page 12 for a complete description of read and write modes.

For a complete list of related documentation, click here.

Logic Block Diagram



Contents

Pin Configuration

Figure 1. 48-ball VFBGA pinout (Top View) [1, 2]

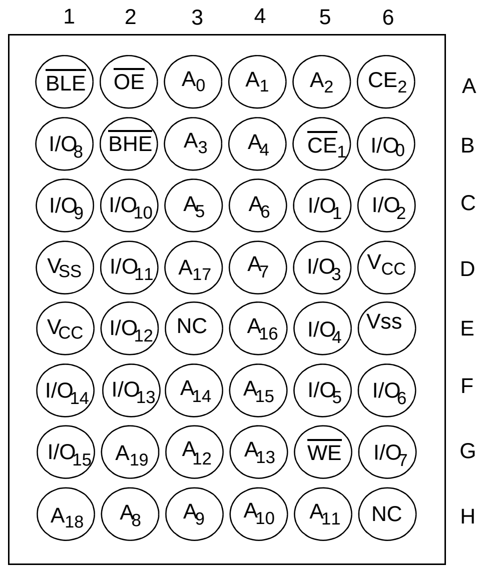
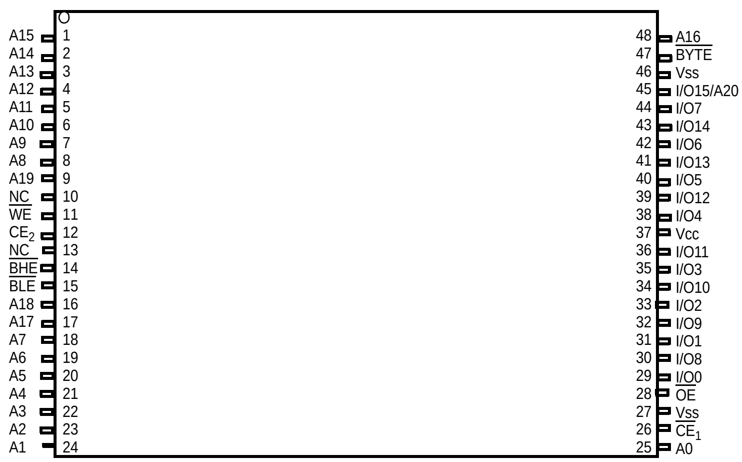


Figure 2. 48-pin TSOP I pinout (Top View) [2, 3]



Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC} (mA)				Standby I_{SB2} (μA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ[4]	Max		Typ[4]	Max	Typ[4]	Max	Typ[4]	Max
CY62167EV30LL	Industrial/Automotive-A	2.2	3.0	3.6	45	2.2	4.0	25	30	1.5	12

Notes
1. Ball H6 for the VFBGA package can be used to upgrade to a 32M density.
2. NC pins are not connected on the die.
3. The BYTE pin in the 48-pin TSOP I package has to be tied to V_{CC} to use the device as a 1 M × 16 SRAM. The 48-pin TSOP I package can also be used as a 2 M × 8 SRAM by tying the BYTE signal to V_{SS}. In the 2 M × 8 configuration, Pin 45 is A20, while BHE, BLE and I/O_8 to I/O_{14} pins are not used.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .... –65 °C to + 150 °C

Ambient temperature
with power applied .... –55 °C to + 125 °C

Supply voltage
to ground potential [5, 6] .... –0.3 V to 3.9 V ($V_{CC(max)}$ + 0.3 V)

DC voltage applied to outputs
in High Z state [5, 6] .... –0.3 V to 3.9 V ($V_{CC(max)}$ + 0.3 V)

DC input voltage [5, 6] .... –0.3 V to 3.9 V ($V_{CC(max)}$ + 0.3 V)

Output current into outputs (LOW) .... 20 mA

Static discharge voltage
(MIL-STD-883, Method 3015) .... >2001 V

Latch-up current .... >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} [7]
CY62167EV30LL	Industrial/ Automotive-A	–40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns (Industrial/ Automotive-A) Min	Typ [8]	Max	Unit
V_{OH}	Output HIGH voltage	$2.2 \le V_{CC} \le 2.7$	I_{OH} = –0.1 mA	2.0	–	–	V
		$2.7 \le V_{CC} \le 3.6$	I_{OH} = –1.0 mA	2.4	–	–	V
V_{OL}	Output LOW voltage	$2.2 \le V_{CC} \le 2.7$	I_{OL} = 0.1 mA	–	–	0.4	V
		$2.7 \le V_{CC} \le 3.6$	I_{OL} = 2.1 mA	–	–	0.4	V
V_{IH}	Input HIGH voltage	$2.2 \le V_{CC} \le 2.7$		1.8	–	V_{CC} + 0.3	V
		$2.7 \le V_{CC} \le 3.6$		2.2	–	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage	$2.2 \le V_{CC} \le 2.7$		–0.3	–	0.6	V
		$2.7 \le V_{CC} \le 3.6$	For VFBGA package	–0.3	–	0.8	V
			For TSOP I package	–0.3	–	0.7[9]	V
I_{IX}	Input leakage current	GND $\le V_I \le V_{CC}$		–1	–	+1	µA
I_{OZ}	Output leakage current	GND $\le V_O \le V_{CC}$, Output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CC(max)}$ I_{OUT} = 0 mA CMOS levels	–	25	30	mA
		f = 1 MHz		–	2.2	4.0	mA
I_{SB1}[10]	Automatic power down current – CMOS inputs	$\overline{CE}_1 \ge V_{CC} - 0.2$ V or $CE_2 \le 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\ge V_{CC} - 0.2$ V, $V_{IN} \ge V_{CC} - 0.2$ V, $V_{IN} \le 0.2$ V, $f = f_{max}$ (address and data only), f = 0 ($\overline{OE}$, and $\overline{WE}$), $V_{CC} = V_{CC(max)}$		–	1.5	12	µA
I_{SB2}[10]	Automatic power down current – CMOS inputs	$\overline{CE}_1 \ge V_{CC} - 0.2$ V or $CE_2 \le 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\ge V_{CC} - 0.2$ V, $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V, f = 0	$V_{CC} = V_{CC(max)}$ Temperature = 25 °C	–	1.5	3.0[11]	µA
			V_{CC} = 3.0 V, Temperature = 40 °C	–	–	3.5[11]	
			$V_{CC} = V_{CC(max)}$ Temperature = 85 °C	–	–	12	

Notes

5. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
6. $V_{IH(max)} = V_{CC}$ + 0.75 V for pulse durations less than 20 ns.
7. Full Device AC operation assumes a 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
9. Under DC conditions the device meets a V_{IL} of 0.8 V. However, in dynamic conditions Input LOW Voltage applied to the device must not be higher than 0.7 V. This is applicable to TSOP I package only.
10. Chip enables ($\overline{CE}_1$ and CE_2), byte enables ($\overline{BHE}$ and $\overline{BLE}$) and $\overline{BYTE}$ must be tied to CMOS levels to meet the I_{SB1}/I_{SB2} / I_{CCDR} spec. Other inputs can be left floating
11. This parameter is guaranteed by design.

Capacitance

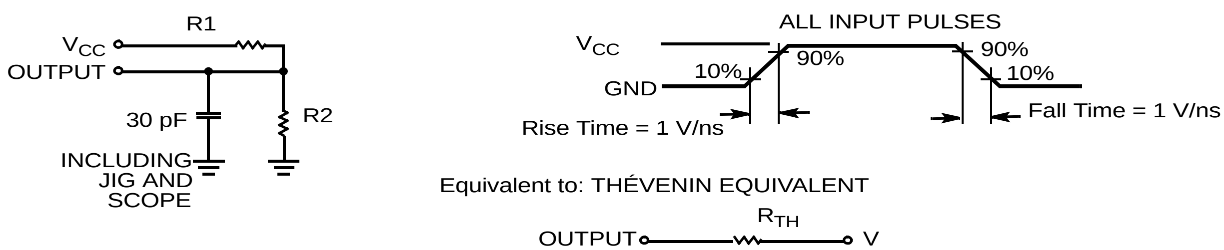
Parameter [12]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [12]	Description	Test Conditions	48-ball VFBGA	48-pin TSOP I	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	55	60	°C/W
Θ_{JC}	Thermal resistance (junction to case)		16	4.3	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Parameters	2.2 V to 2.7 V	2.7 V to 3.6 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note
12. Tested initially and after any design or process changes that may affect these parameters.

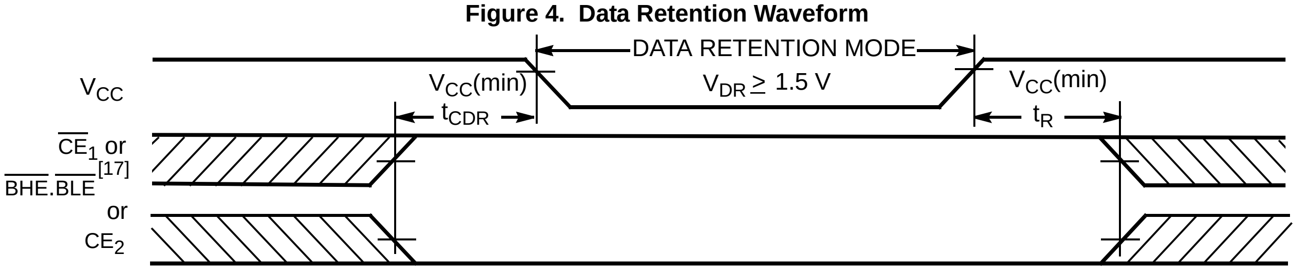
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions			Min	Typ [13]	Max	Unit
V_{DR}	V_{CC} for data retention				1.5	–	–	V
I_{CCDR}[14]	Data retention current	V_{CC} = 1.5 V to 3.0 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Industrial	48-pin TSOP I	–	–	8	µA
		V_{CC} = 1.5 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Industrial	Other packages	–	–	10	µA
			Automotive-A	All packages	–	–	10	µA
t_{CDR}[15]	Chip deselect to data retention time				0	–	–	–
t_R[16]	Operation recovery time				45	–	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes

13. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
14. Chip enables ($\overline{CE}_1$ and CE_2), byte enables ($\overline{BHE}$ and $\overline{BLE}$) and $\overline{BYTE}$ must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
15. Tested initially and after any design or process changes that may affect these parameters.
16. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
17. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Parameter [18, 19]	Description	45 ns (Industrial / Automotive-A)		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [20]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [20, 21]	–	18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z [20]	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z [20, 21]	–	18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power-up	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power-down	–	45	ns
t_{DBE}	BLE / BHE LOW to data valid	–	45	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low Z [20]	10	–	ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to High Z [20, 21]	–	18	ns
Write Cycle [22, 23]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [20, 21]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [20]	10	–	ns

Notes

18. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in Figure 3 on page 5.
19. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
20. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
21. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
22. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
23. The minimum pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 5. Read Cycle No. 1 (Address Transition Controlled) [24, 25]

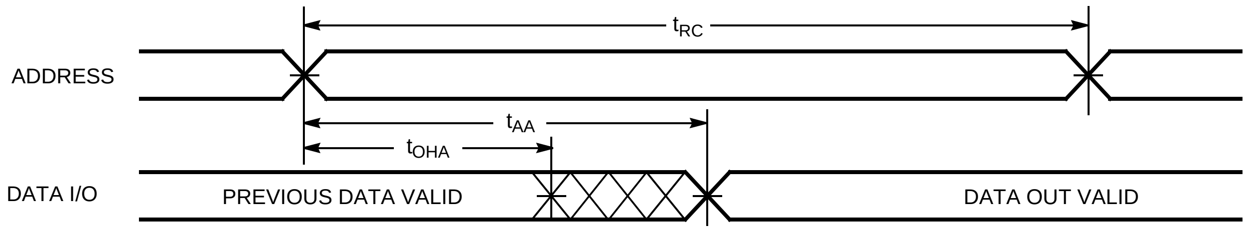
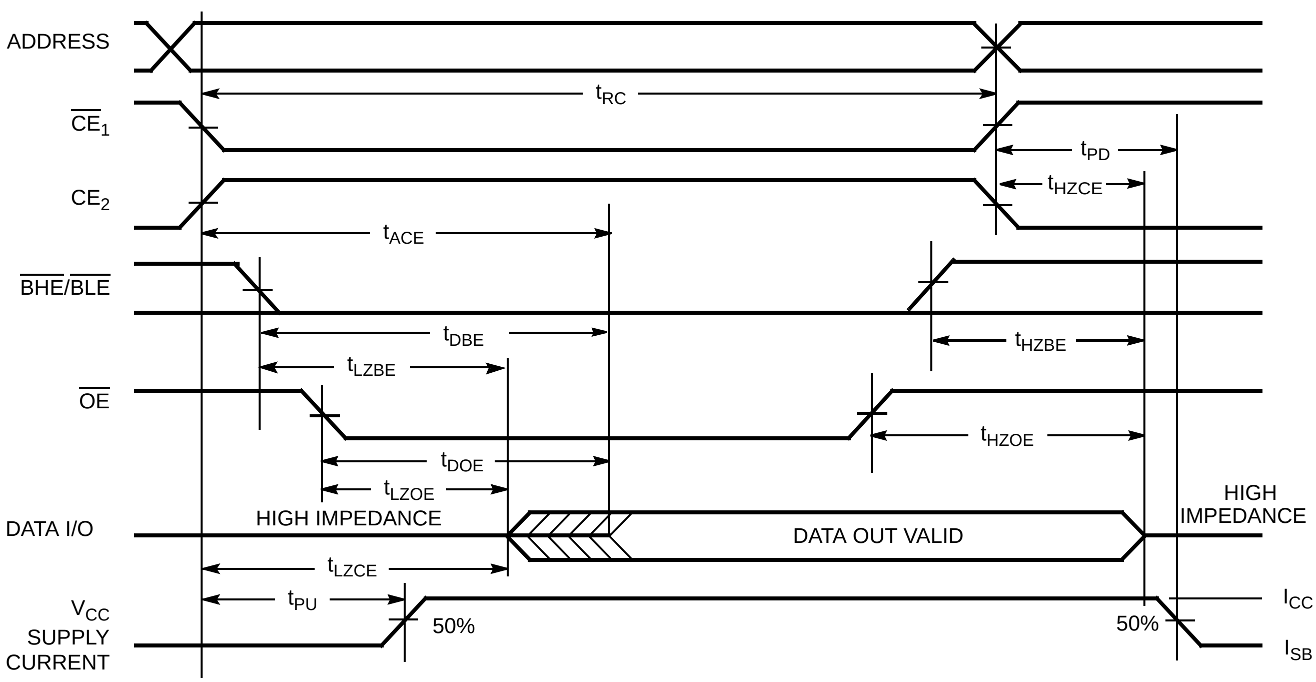


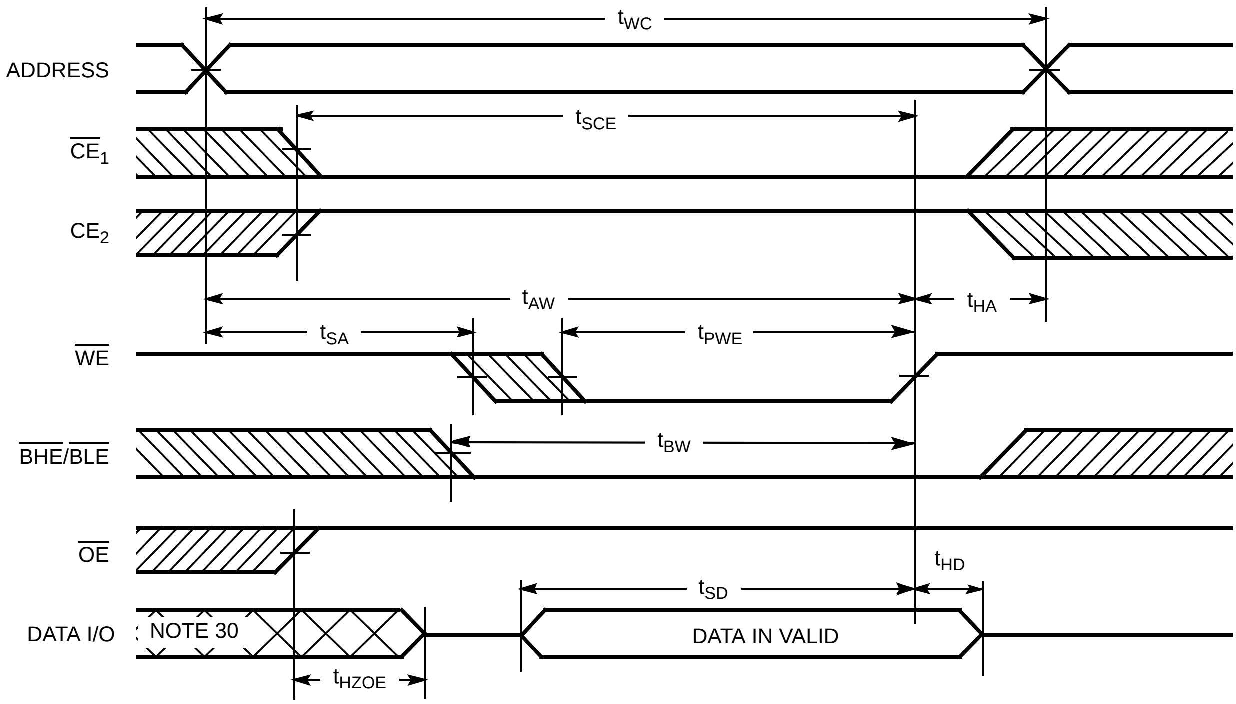
Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled) [25, 26]



Notes
24. The device is continuously selected. $\overline{OE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}, and $CE_2 = V_{IH}$.
25. $\overline{WE}$ is HIGH for read cycle.
26. Address valid before or similar to $\overline{CE}_1$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ($\overline{WE}$ Controlled) [27, 28, 29]

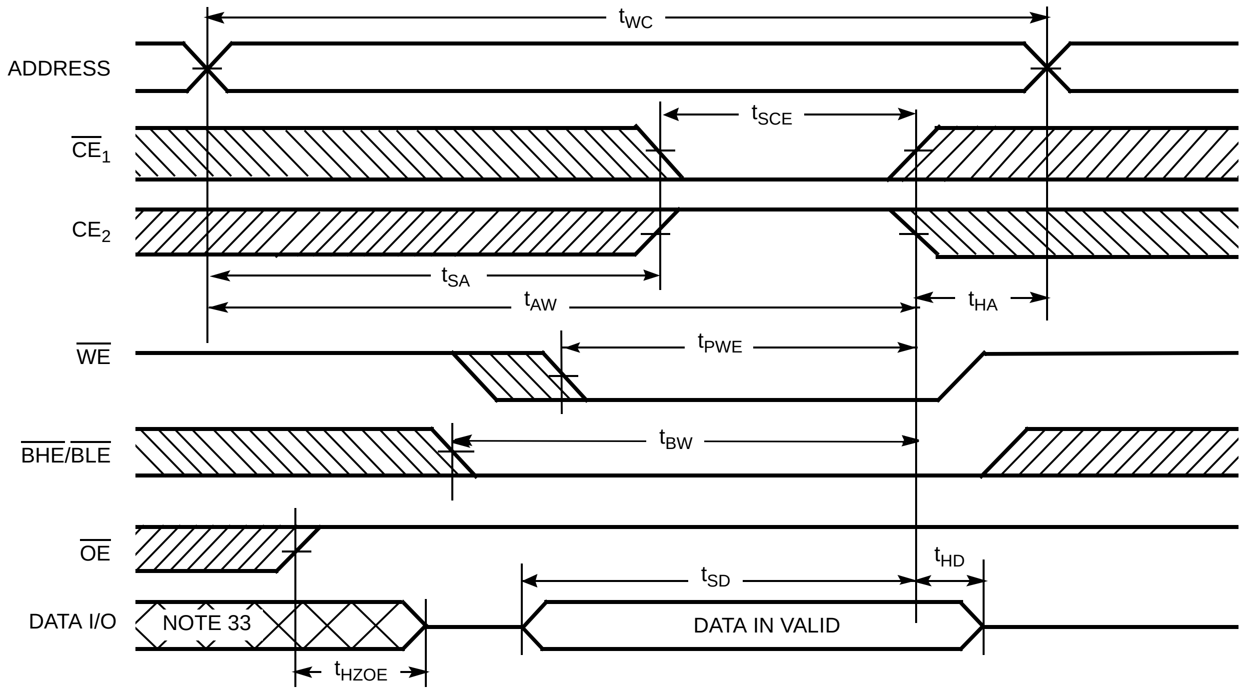


Notes

27. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
28. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
29. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
30. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 2 ($\overline{CE_1}$ or CE_2 Controlled) [31, 32]



Notes

31. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE_1} = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
32. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
33. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) [34]

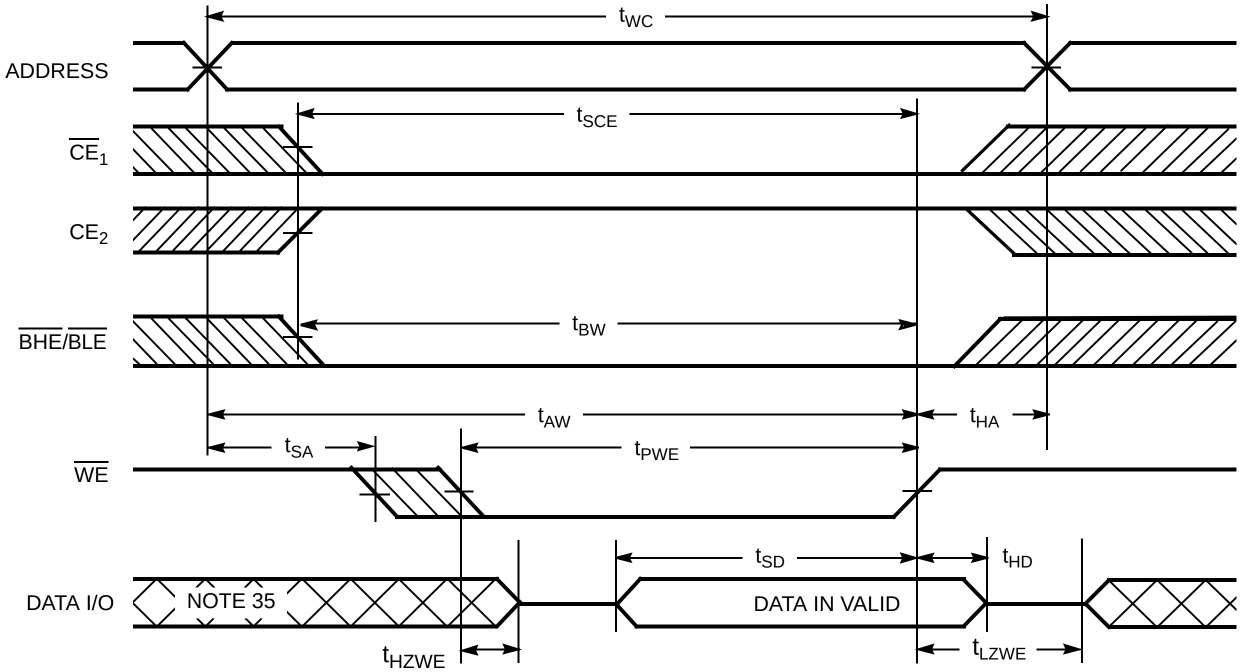
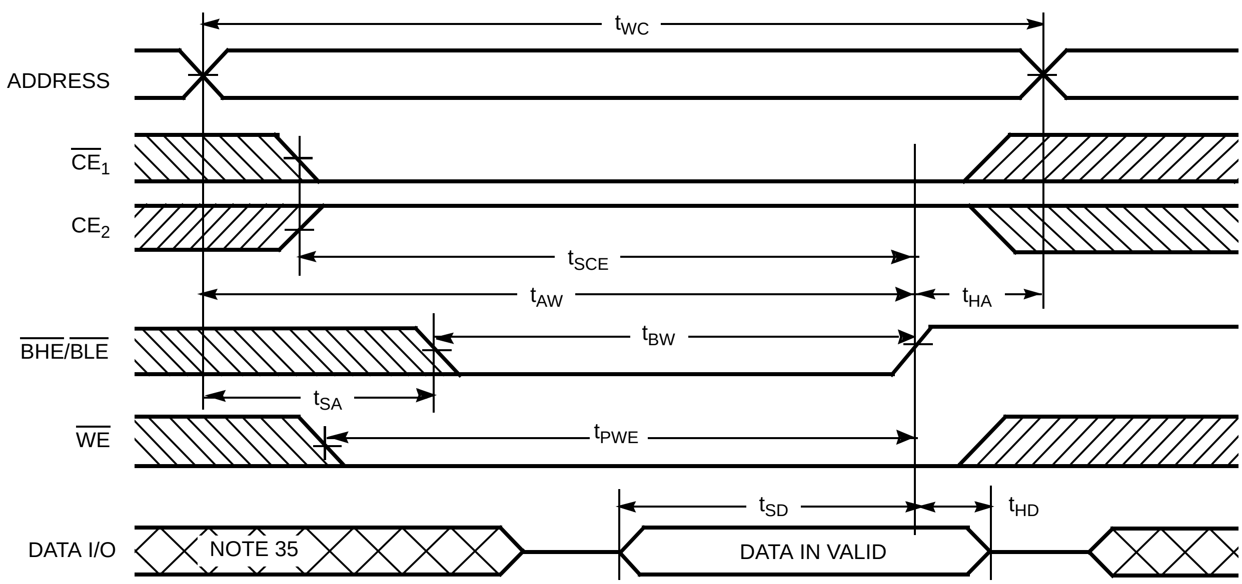


Figure 10. Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ controlled, $\overline{OE}$ LOW) [34]



Notes

34. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
35. During this period the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X[36]	X	X	X[36]	X[36]	High Z	Deselect/Power-down	Standby (I_{SB})
X[36]	L	X	X	X[36]	X[36]	High Z	Deselect/Power-down	Standby (I_{SB})
X[36]	X[36]	X	X	H	H	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	High Z (I/O_0–I/O_7); Data Out (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	High Z (I/O_0–I/O_7); Data In (I/O_8–I/O_{15})	Write	Active (I_{CC})

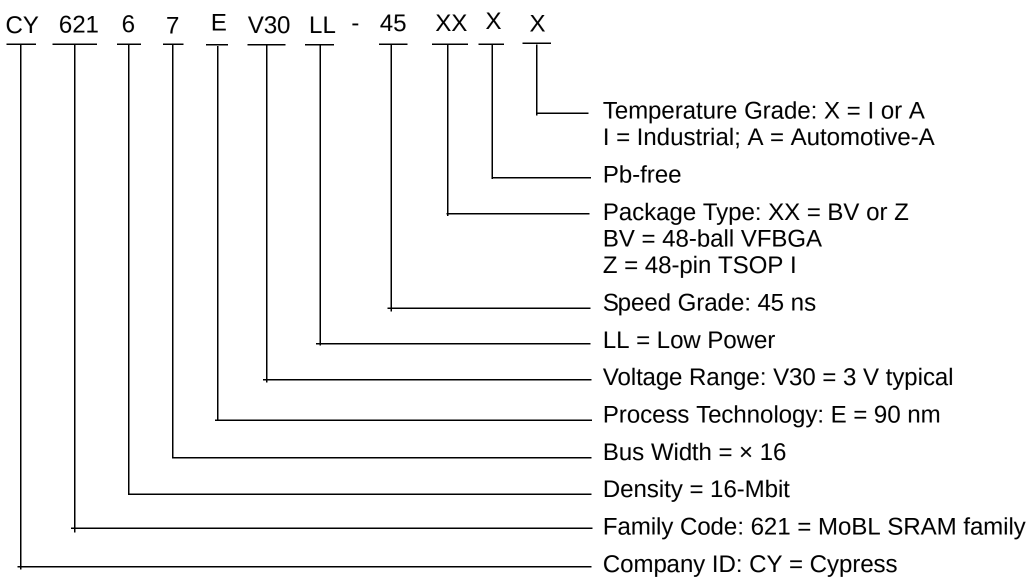
Note

36. The 'X' (Don't care) state for the chip enables and Byte enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

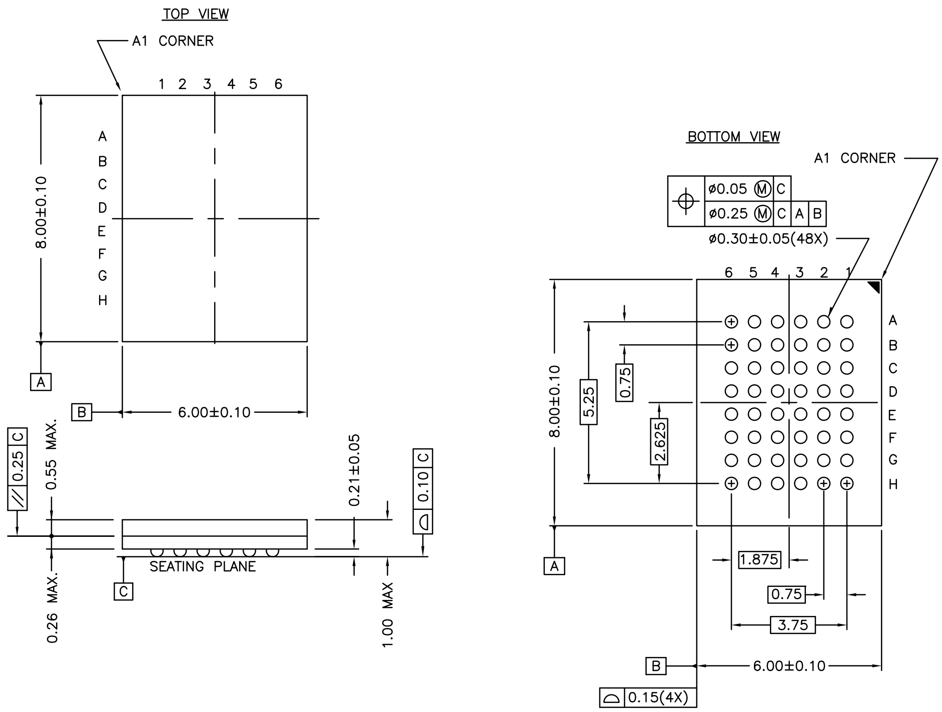
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62167EV30LL-45BVI	51-85150	48-ball VFBGA (6 × 8 × 1 mm), Package Code: BV48	Industrial
	CY62167EV30LL-45BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Package Code: BZ48	
	CY62167EV30LL-45ZXI	51-85183	48-pin TSOP I (Pb-free)	
	CY62167EV30LL-45BVXA	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Package Code: BZ48	Automotive-A
	CY62167EV30LL-45ZXA	51-85183	48-pin TSOP I (Pb-free)	

Ordering Code Definitions



Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150

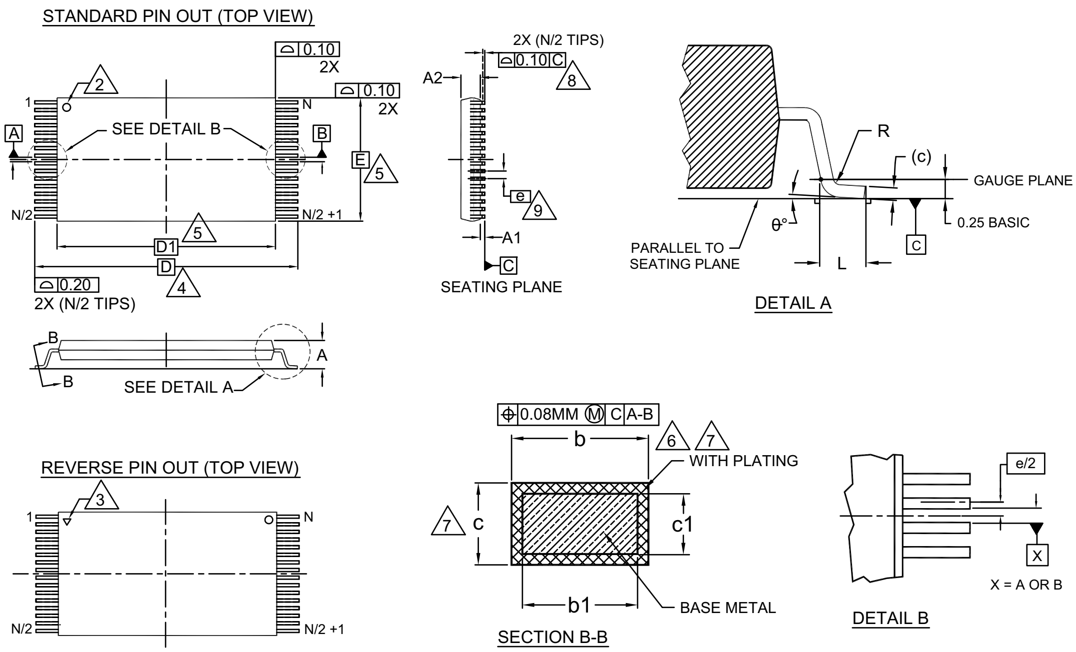


NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Package Diagrams (continued)

Figure 12. 48-pin TSOP I (18.4 × 12 × 1.2 mm) Package Outline, 51-85183



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	20.00 BASIC		
D1	18.40 BASIC		
E	12.00 BASIC		
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8
R	0.08	—	0.20
N	48		

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm .
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 *F

Acronyms

Acronym	Description
$\overline{\text{BHE}}$	byte high enable
$\overline{\text{BLE}}$	byte low enable
$\overline{\text{CE}}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{\text{OE}}$	output enable
SRAM	static random access memory
TSOP	thin small outline package
VFBGA	very fine-pitch ball grid array
$\overline{\text{WE}}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62167EV30 MoBL®, 16-Mbit (1M × 16/2M × 8) Static RAM Document Number: 38-05446				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	202600	AJU	01/23/2004	New data sheet.
*A	463674	NXR	See ECN	Changed status from Advance Information to Preliminary Removed ‘L’ bin and 35 ns speed bin from product offering Modified Data sheet to include x8 configurability. Changed ball E3 in FBGA pinout from DNU to NC Changed the $I_{SB2(Typ)}$ value from 1.3 µA to 1.5 µA Changed the $I_{CC(Max)}$ value from 40 mA to 25 mA Changed Vcc stabilization time in footnote #9 from 100 µs to 200 µs Changed the AC Test Load Capacitance value from 50 pF to 30 pF Corrected typo in Data Retention Characteristics (t_R) from 100 µs to t_{RC} ns Changed t_{OHA}, t_{LZCE}, t_{LZBE}, and t_{LZWE} from 6 ns to 10 ns Changed t_{LZOE} from 3 ns to 5 ns. Changed t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} from 15 ns to 18 ns Changed t_{SCE}, t_{AW}, and t_{BW} from 40 ns to 35 ns Changed t_{PE} from 30 ns to 35 ns Changed t_{SD} from 20 ns to 25 ns Updated 48-ball FBGA Package Information. Updated the Ordering Information table
*B	469169	NSI	See ECN	Minor Change: Moved to external web
*C	1130323	VKN	See ECN	Changed status from Preliminary to Final. Changed I_{CC} max spec from 2.8 mA to 4.0 mA for f = 1MHz Changed I_{CC} typ spec from 22 mA to 25 mA for f = f_{max} Changed I_{CC} max spec from 25 mA to 30 mA for f = f_{max} Added V_{IL} spec for TSOP I package and footnote# 9 Added footnote# 10 related to I_{SB2} and I_{CCDR} Changed I_{SB1} and I_{SB2} spec from 8.5 µA to 12 µA Changed I_{CCDR} spec from 8 µA to 10 µA Added footnote# 15 related to AC timing parameters
*D	1323984	VKN / AESA	See ECN	Modified I_{CCDR} spec for TSOP I package Added 48-ball VFBGA (6 × 7 × 1mm) package Added footnote# 1 related to VFBGA (6 × 7 × 1mm) package Updated Ordering Information table
*E	2678799	VKN / PYRS	03/25/2009	Added Automotive-A information
*F	2720234	VKN / AESA	06/17/2009	Included -45BVXA part in the Ordering information table
*G	2880574	VKN	02/18/2010	Modified I_{CCDR} spec from 8 µA to 10 µA for Auto-A grade. Added Contents. Updated all package diagrams. Updated links in Sales, Solutions, and Legal Information.
*H	2934396	VKN	06/03/10	Added footnote #25 related to chip enable. Updated template.
*I	3006301	RAME	08/12/2010	Included $\overline{BHE}$ and $\overline{BLE}$ in I_{SB1}, I_{SB2}, and I_{CCDR} test conditions to reflect Byte power down feature. Removed 48-ball VFBGA (6 × 7 × 1 mm) package related information. Added Acronyms and Ordering code definition. Format updates to match template.

Document History Page (continued)

Document Title: CY62167EV30 MoBL®, 16-Mbit (1M × 16/2M × 8) Static RAM Document Number: 38-05446				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*J	3295175	RAME	06/29/2011	Updated Package Diagrams. Added Document Conventions. Removed reference to AN1064 SRAM system guidelines. Added I_{SB1} to footnotes 10 and 14. Added byte enables to footnote 36 and referenced to Truth table.
*K	3411301	TAVA	10/17/2011	Updated Switching Waveforms. Updated Package Diagrams. Updated to new template.
*L	3667939	TAVA	07/09/2012	Updated Ordering Information (No change in part numbers, updated details in Package Type column only). Updated Package Diagrams (Spec 51-85150 (Updated figure caption only, no change in revision)).
*M	4102969	VINI	08/23/2013	Updated Switching Characteristics: Updated Note 19. Updated Package Diagrams: spec 51-85150 – Changed revision from *G to *H. Updated to new template. Completing Sunset Review.
*N	4574264	VINI	11/19/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Maximum Ratings: Referred Notes 5 and 6 in “Supply voltage to ground potential”. Updated Switching Characteristics: Added Note 23 and referred the same note in “Write Cycle”.
*O	4715413	VINI	04/07/2015	Updated Electrical Characteristics: Updated details in “Test Conditions” column corresponding to I_{SB2} parameter and added corresponding values. Added Note 11 and referred the same note in maximum values of I_{SB2} parameter corresponding to Test Conditions “V_{CC} = $V_{CC(max)}$, Temperature = 25 °C” and “V_{CC} = 3.0 V, Temperature = 40 °C”.
*P	5734005	VINI	05/11/2017	Updated Package Diagrams: spec 51-85183 – Changed revision from *D to *F. Updated to new template.

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