X9116

Low Noise, Low Power, Low Cost Digitally Controlled Potentiometer (XDCP™)

FN8160
Rev 3.00
February 3, 2011

The Intersil X9116 is a digitally controlled nonvolatile potentiometer designed to be used in trimmer applications. The pot consists of 15 equal resistor segments that connect to the wiper pin through programmable CMOS switches. The tap position is programmed through a 3-wire up/down serial port. The last position of the wiper is stored in a nonvolatile memory location which is recalled at the time of power up of the device.

The wiper moves through sequential tap positions with inputs on the serial port. A falling edge on INC (bar) causes the tap position to increment one position up or down based on whether the U/D (bar) pin is held high or low.

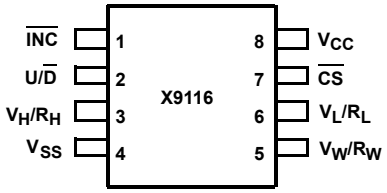
The X9116 can be used in many applications requiring a variable resistance. In many cases it can replace a mechanical trimmer and offers many advantages such as temperature and time stability as well as the reliability of a solid state solution.

Features

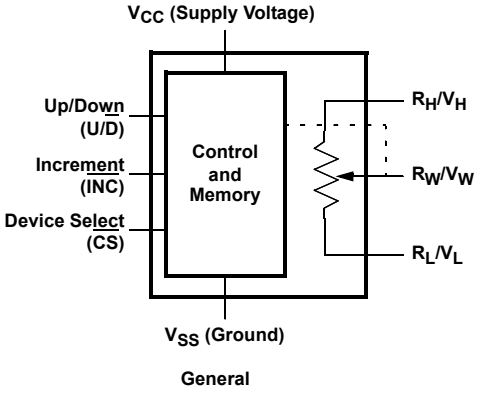
- Solid-state nonvolatile
- 16 wiper taps
- 3-wire up/down serial interface
- V_{CC} = 2.7V and 5V
- Active current < 50µA max.
- Standby current < 5µA max.
- R_{TOTAL} = 10kΩ
- Packages: 8 Ld MSOP, 8 Ld SOIC
- Pb-free plus anneal available (RoHS compliant)

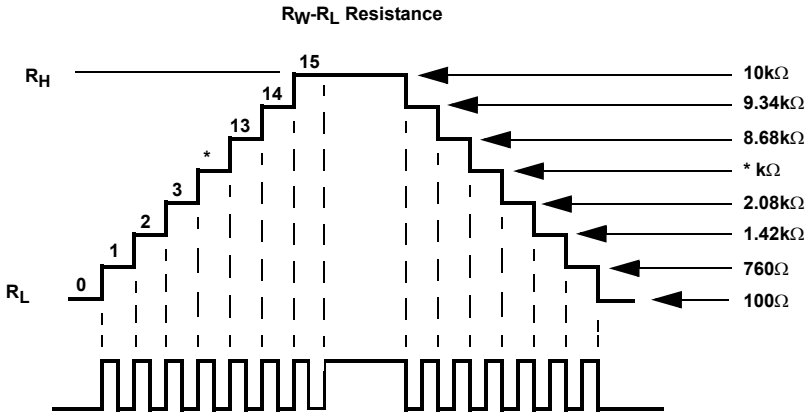
Pinout

SOIC/MSOP



Block Diagram





Ordering Information

PART NUMBER (BRAND) (Notes 1, 2, 3)	PART MARKING	V_{CC} LIMITS (V)	R_{TOTAL} (kΩ)	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
X9116WM8Z	AKY	5V ±10%	10	0 to +70	8 Ld MSOP	M8.118
X9116WM8IZ	DCG			-40 to +85	8 Ld MSOP	M8.118
X9116WS8Z	X9116W Z			0 to +70	8 Ld SOIC	M8.15
X9116WS8IZ	X9116W ZI			-40 to +85	8 Ld SOIC	M8.15
X9116WM8Z-2.7	AOJ	2.7-5.5		0 to +70	8 Ld MSOP	M8.118
X9116WM8IZ-2.7	AKS			-40 to +85	8 Ld MSOP	M8.118
X9116WS8Z-2.7	X9116W ZF			0 to +70	8 Ld SOIC	M8.15
X9116WS8IZ-2.7	X9116W G			-40 to +85	8 Ld SOIC	M8.15

NOTES:

1. Add “T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for X9116. For more information on MSL please see techbrief TB363.

Pin Descriptions

V_H /R_H and V_L /R_L

The high (V_H/R_H) and low (V_L/R_L) terminals of the X9116 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is V_{SS} and the maximum is V_{CC}.

V_W/R_W

R_W/R_W is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 200Ω to 400Ω depending upon V_{CC}.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incremented (up) or decremented (down).

Increment ($\overline{INC}$)

The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)

The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete the X9116 will be placed in the low power standby mode until the device is selected once again.

Pin Descriptions

SYMBOL	DESCRIPTION
V_H/R_H	High Terminal

Pin Descriptions

SYMBOL	DESCRIPTION
V_W/R_W	Wiper Terminal
V_L/R_L	Low Terminal
V_{SS}	Ground
V_{CC}	Supply Voltage
U/$\overline{D}$	Up/Down Control Input
$\overline{INC}$	Increment Control Input
$\overline{CS}$	Chip Select Input

Principles of Operation

There are three sections of the X9116: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 15 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper pin.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for t_{IW} ($\overline{INC}$ to V_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the wiper is set to the value last stored.

Instructions and Programming

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW, the device is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a four bit counter. The output of this counter is decoded to select one of 16 wiper positions along the resistive array.

The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH.

The system may select the X9116, move the wiper, and deselect the device without having to store the latest wiper position in nonvolatile memory. After the wiper movement is performed as described above and once the new position is reached, the system must keep $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position will be maintained until changed by the system or until a power-up/down cycle recalls the previously stored data.

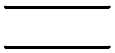
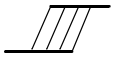
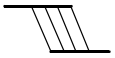
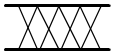
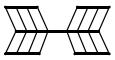
This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation, minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, etc.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained.

Mode Selection

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
L		H	Wiper Up
L		L	Wiper Down
	H	X	Store Wiper Position
H	X	X	Standby Current
	L	X	No Store, Return to Standby

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don’t Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Absolute Maximum Ratings

Temperature Under Bias . . . . . -65°C to +135°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$, V_H/R_H, V_L/R_L
and V_{CC} with Respect to V_{SS} . . . . . -1V to +7V
$\Delta V = |V_H/R_H - V_L/R_L|$ 5.5V
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp
I_W (10 seconds) . . . . . ±10.0mA

Recommended Operating Conditions

Temperature Range
Commercial . . . . . 0°C to +70°C
Industrial . . . . . -40°C to +85°C
Supply Voltage (V_{CC}) Limits
X9116 . . . . . 5V ± 10%
X9116-2.7 . . . . . 2.7V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Potentiometer Specifications Over recommended operating conditions unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +85°C or 0°C to +70°C.**

SYMBOL	PARAMETER	TEST CONDITIONS/NOTES	MIN (Note 10)	TYP	MAX (Note 10)	UNIT
R_{TOTAL}	End to end resistance variation		**-20**		**+20**	%
V_{VH}	V_H/R_H terminal voltage	V_{SS} = 0V	**V_{SS}**		**V_{CC}**	V
V_{VL}	V_L/R_L terminal voltage	V_{SS} = 0V	**V_{SS}**		**V_{CC}**	V
	Power rating	R_{TOTAL} = 10kΩ			**10**	mW
R_W	Wiper resistance	I_W = 1mA, V_{CC} = 5V		200	**400**	Ω
R_W	Wiper resistance	I_W = 1mA, V_{CC} = 2.7V		400	**1000**	Ω
I_W	Wiper current		**-5.0**		**+5.0**	mA
	Noise	Ref: 1kHz		-120		dBV
	Resolution			6		%
	Absolute linearity (Note 4)	$V_{w(n)(actual)} - V_{w(n)(expected)}$	**-1**		**+1**	MI (Note 6)
	Relative linearity (Note 5)	$V_{w(n+1)} - [V_{w(n)} + MI]$	**-0.2**		**+0.2**	MI (Note 6)
	R_{TOTAL} temperature coefficient			±300		ppm/°C
	Ratiometric temperature coefficient			±20		ppm/°C
$C_H/C_L/C_W$	Potentiometer capacitances	See “Circuit #3 SPICE Macro Model” on page 5		10/10/25		pF

NOTES:

4. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage = ($V_{w(n)}$(actual) - $V_{w(n)}$(expected)) = ±1 MI Maximum.
5. Relative linearity is a measure of the error in step size between taps = $V_{W(n+1)}$ -[$V_{w(n)}$ + MI] = ±0.2 MI.
6. 1 MI = Minimum Increment = R_{TOT}/15.

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DC Electrical Specifications Over recommended operating conditions unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C or 0°C to +70°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 10)	TYP (Note 7)	MAX (Note 10)	UNIT
I_{CC1}	V_{CC} active current (Increment)	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = 0.4V/2.4V @ max t_{CYC}			**150**	µA
I_{CC2}	V_{CC} active current (Store) (EEPROM Store)	$\overline{CS}$ = V_{IH}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = V_{IH} @ max t_{WR}			**400**	µA
I_{SB}	Standby supply current	$\overline{CS}$ = V_{CC} – 0.3V, U/$\overline{D}$ and $\overline{INC}$ = V_{SS} or V_{CC} – 0.3V			**5**	µA
I_{LI}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input leakage current	V_{IN} = V_{SS} to V_{CC}			**±10**	µA
V_{IH}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input HIGH voltage		**2V**		**V_{CC} + 0.5**	V
V_{IL}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input LOW voltage		**-0.5**		**0.8**	V
C_{IN}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input capacitance	V_{CC} = 5V, V_{IN} = V_{SS}, T_A = +25°C, f = 1MHz		10		pF

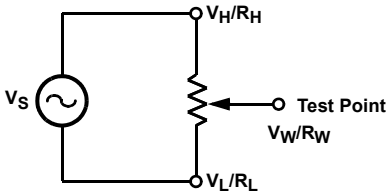
NOTES:

7. Typical values are for T_A = +25°C and nominal supply voltage.

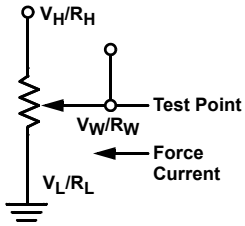
Endurance and Data Retention

PARAMETER	MIN	UNIT
Minimum endurance	100,000	Data changes per bit
Data retention	100	Years

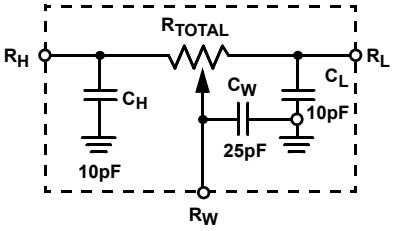
Test Circuit #1



Test Circuit #2



Circuit #3 SPICE Macro Model



A.C. Conditions of Test

Input pulse levels	0V to 3V
Input rise and fall times	10ns
Input reference levels	1.5V

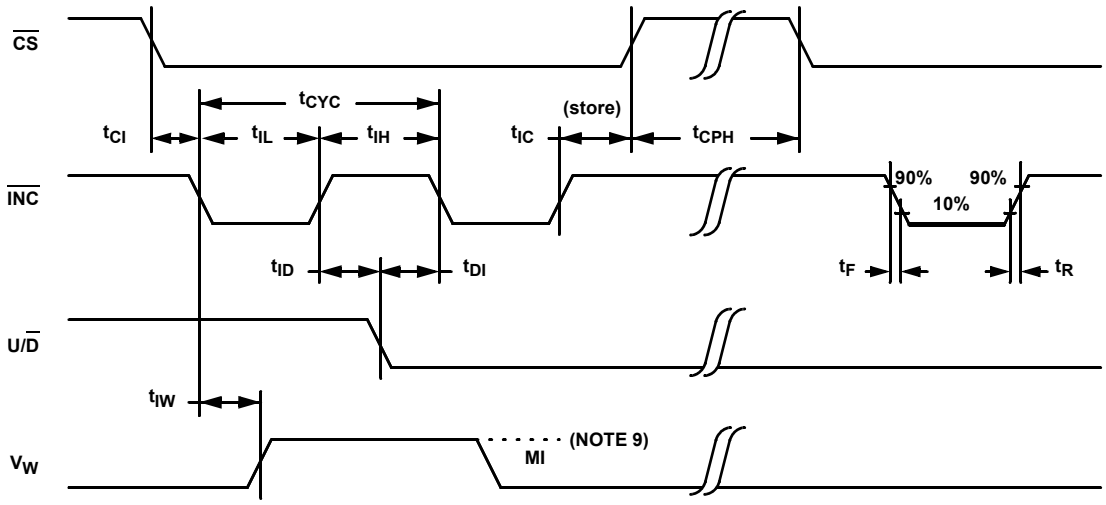
DC Electrical Specifications Over recommended operating conditions unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C or 0°C to +70°C.**

SYMBOL	PARAMETER	MIN (Note 10)	TYP (NOTE 8)	MAX (Note 10)	UNIT
t_{CI}	$\overline{CS}$ to $\overline{INC}$ setup	**100**			ns
t_{ID}	$\overline{INC}$ HIGH to U/$\overline{D}$ change	**100**			ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ setup	**2.9**			µs
t_{IL}	$\overline{INC}$ LOW period	**1**			µs
t_{IH}	$\overline{INC}$ HIGH period	**1**			µs
t_{IC}	$\overline{INC}$ inactive to $\overline{CS}$ inactive	**1**			µs
t_{CPH}	$\overline{CS}$ deselect time (STORE)	**10**			ms
t_{IW}	$\overline{INC}$ to Vw change		1	**5**	µs
t_{CYC}	$\overline{INC}$ cycle time	**4**			µs
t_R, t_F	$\overline{INC}$ input rise and fall time			**500**	µs
t_{PU}	Power up to wiper stable			**5**	µs
t_R V_{CC}	V_{CC} Power-up rate	**15**		**50**	mV/µs
t_{WR}	Store cycle		5	**10**	ms

Power Up and Down Requirements

There are no restrictions on the power-up or power-down conditions of V_{CC} and the voltages applied to the potentiometer pins provided that V_{CC} is always more positive than or equal to V_H, V_L, and V_W, i.e., $V_{CC} \geq V_H, V_L, V_W$. The V_{CC} ramp rate spec is always in effect.

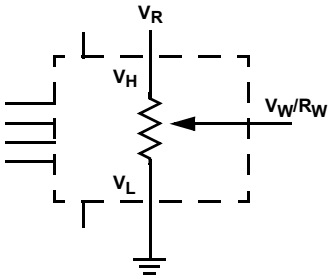
A.C. Timing



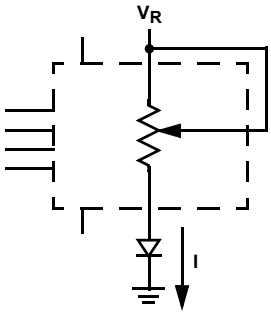
NOTES:

8. Typical values are for T_A = +25°C and nominal supply voltage.
9. MI in the A.C. timing diagram refers to the minimum incremental change in the V_W output due to a change in the wiper position.
10. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Basic Configurations of Electronic Potentiometers



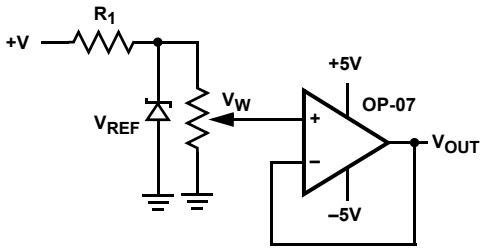
THREE-TERMINAL POTENTIOMETER;
VARIABLE VOLTAGE DIVIDER



TWO-TERMINAL VARIABLE RESISTOR;
VARIABLE CURRENT

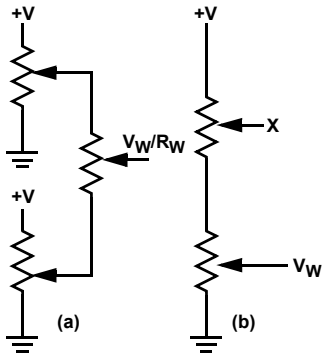
Basic Circuits

BUFFERED REFERENCE VOLTAGE

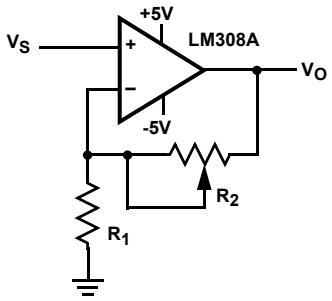


$V_{OUT} = V_W/R_W$

CASCADING TECHNIQUES

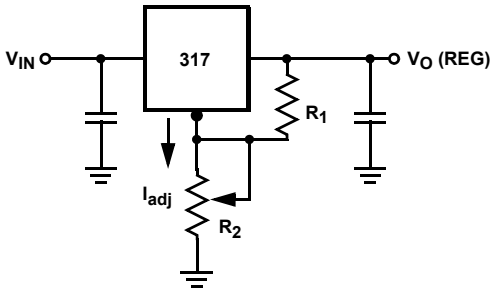


NONINVERTING AMPLIFIER



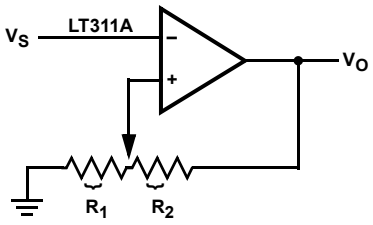
$V_O = (1+R_2/R_1)V_S$

VOLTAGE REGULATOR



V_O (REG) = 1.25V (1+R_2/R_1)+Iadj R_2

COMPARATOR WITH HYSTERESIS



$V_{UL} = \{R_1/(R_1+R_2)\}\ V_O(max)$
$V_{LL} = \{R_1/(R_1+R_2)\}\ V_O(min)$

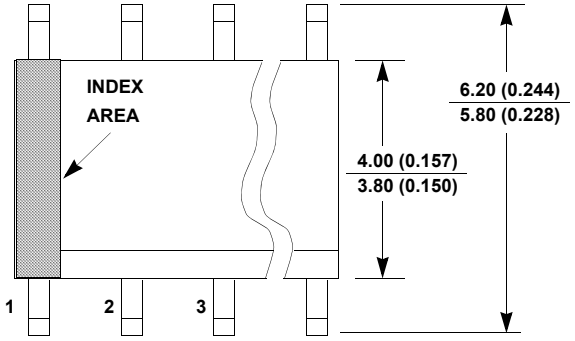
(FOR ADDITIONAL CIRCUITS, SEE AN115)

Package Outline Drawing

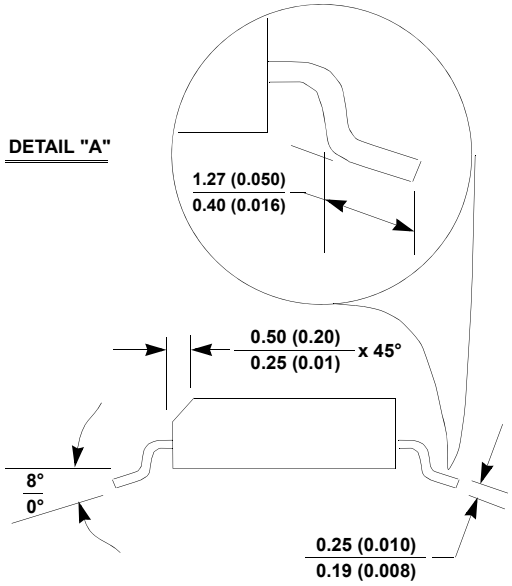
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

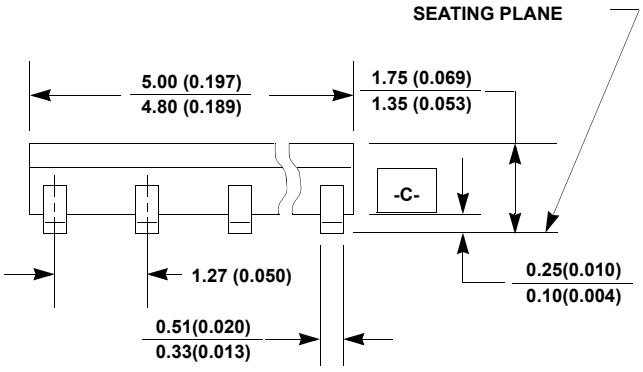
Rev 2, 11/10



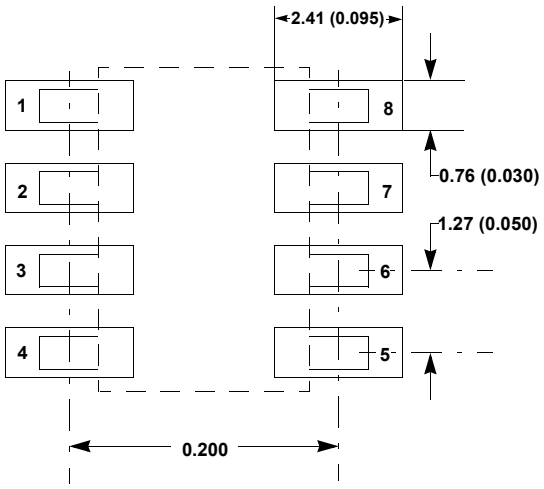
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

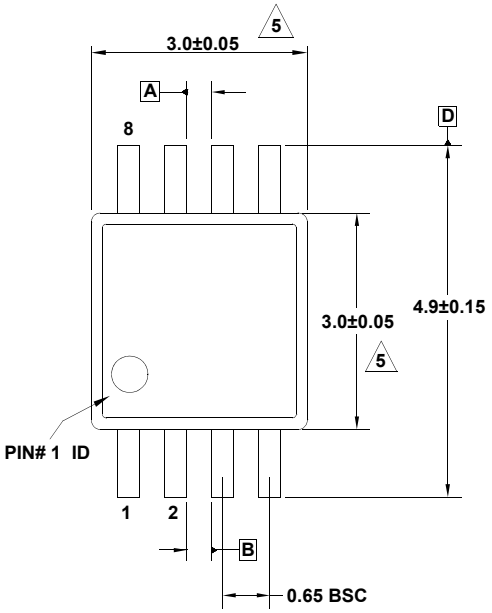
NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

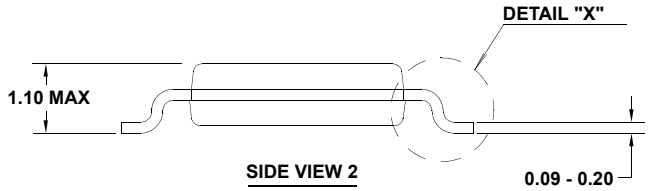
Package Outline Drawing

M8.118

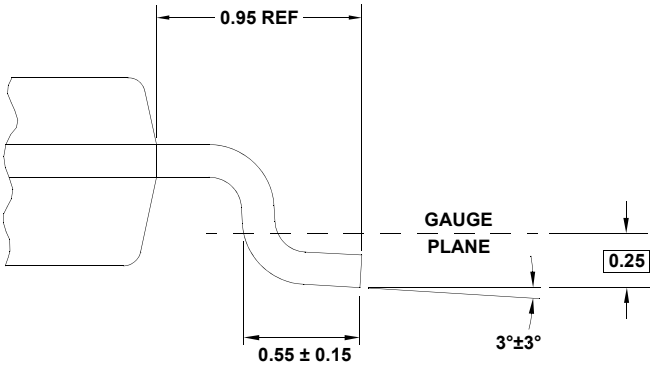
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE
Rev 3, 3/10



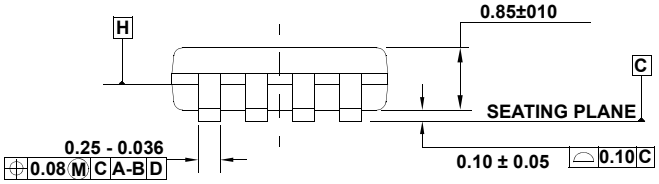
TOP VIEW



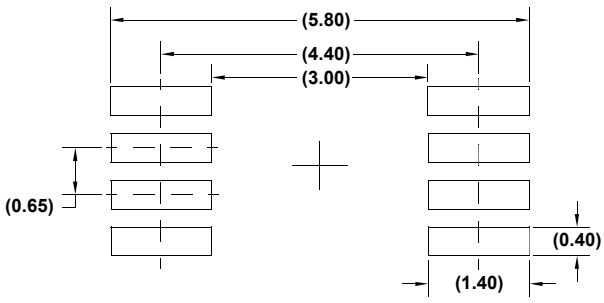
SIDE VIEW 2



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.