

SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688, SN74LS682, SN74LS684 THRU SN74LS688 8-BIT MAGNITUDE/IDENTITY COMPARATORS

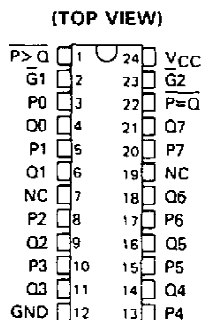
D2617, JANUARY 1981—REVISED MARCH 1988

SDLS008

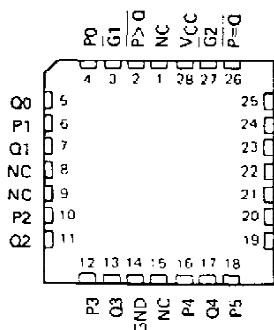
- Compares Two-8-Bit Words
- Choice of Totem-Pole or Open-Collector Outputs
- Hysteresis at P and Q Inputs
- 'LS682 has 20-k Ω Pullup Resistors on the Q Inputs
- SN74LS686 and 'LS687 . . . JT and NT 24-Pin, 300-Mil Packages

TYPE	P = Q	P > Q	OUTPUT ENABLE	OUTPUT CONFIGURATION	20-k Ω PULLUP
'LS682	yes	yes	no	totem-pole	yes
'LS684	yes	yes	no	totem-pole	no
'LS685	yes	yes	no	open-collector	no
SN74LS686	yes	yes	yes	totem-pole	no
'LS687	yes	yes	yes	open-collector	no
'LS688	yes	no	yes	totem-pole	no

SN54LS687 . . . JT PACKAGE
SN74LS686, SN74LS687 . . . DW OR NT PACKAGE



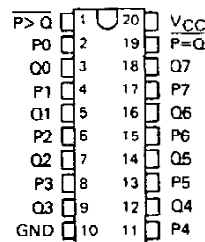
SN54LS687 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

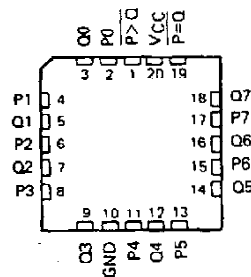
SN54LS682, SN54LS684, SN54LS685 . . . J PACKAGE
SN74LS682, SN74LS684, SN74LS685 . . . DW OR N PACKAGE

(TOP VIEW)



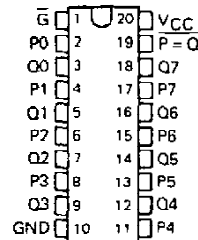
SN54LS682, SN54LS684, SN54LS685 . . . FK PACKAGE

(TOP VIEW)



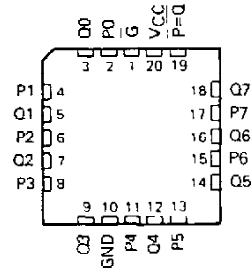
SN54LS688 . . . J PACKAGE
SN74LS688 . . . DW OR N PACKAGE

(TOP VIEW)



SN54LS688 . . . FK PACKAGE

(TOP VIEW)



PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688 **SN74LS682, SN74LS684 THRU SN74LS688** **8-BIT MAGNITUDE/IDENTITY COMPARATORS**

description

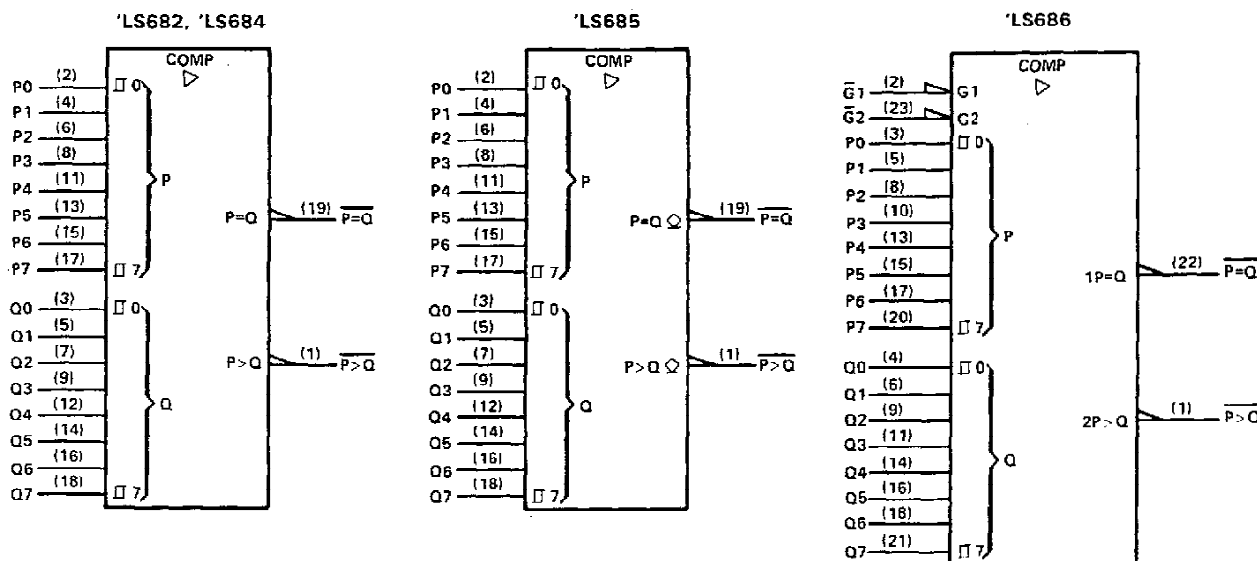
These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide $\overline{P=Q}$ outputs and all except 'LS688 provide $\overline{P>Q}$ outputs as well. The 'LS682, 'LS684, 'LS686, and 'LS688 have totem-pole outputs, while the 'LS685 and 'LS687 have open-collector outputs. The 'LS682 features 20-k Ω pullup termination resistors on the Q inputs for analog or switch data.

FUNCTION TABLE

INPUTS			OUTPUTS	
DATA	ENABLES		$\overline{P=Q}$	$\overline{P>Q}$
P, Q	$\overline{G}, \overline{G1}$	$\overline{G2}$		
P=Q	L	X	L	H
P>Q	X	L	H	L
P<Q	X	X	H	H
P=Q	H	X	H	H
P>Q	X	H	H	H
X	H	H	H	H

- NOTES: 1. The last three lines of the function table applies only to the devices having enable inputs, i.e., 'LS686 thru 'LS688.
2. The $\overline{P<Q}$ function can be generated by applying the $\overline{P=Q}$ and $\overline{P>Q}$ outputs to a 2-input NAND gate.
3. For 'LS686 and 'LS687, $\overline{G1}$ enables $\overline{P=Q}$ and $\overline{G2}$ enables $\overline{P>Q}$.

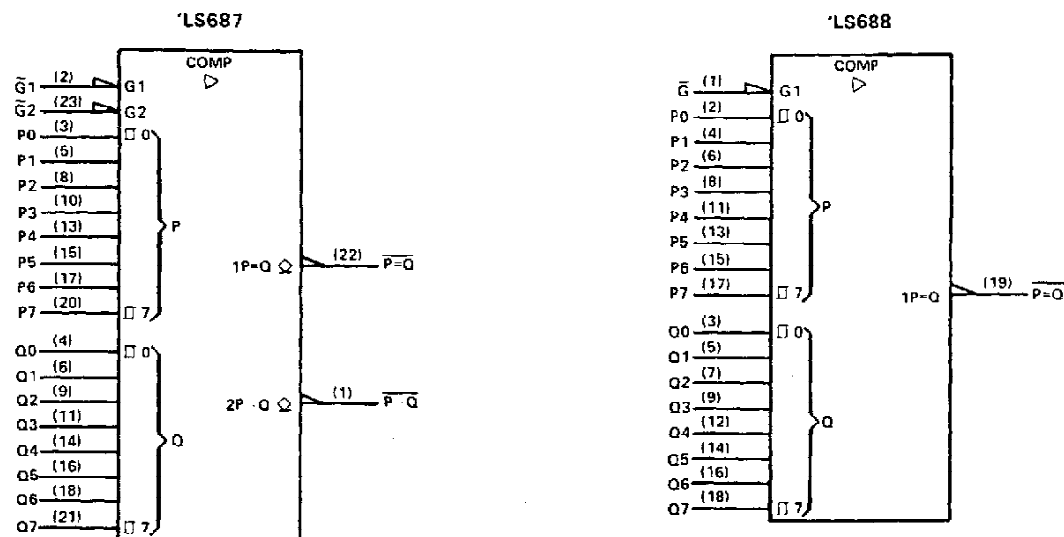
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, JT, N, and NT packages.

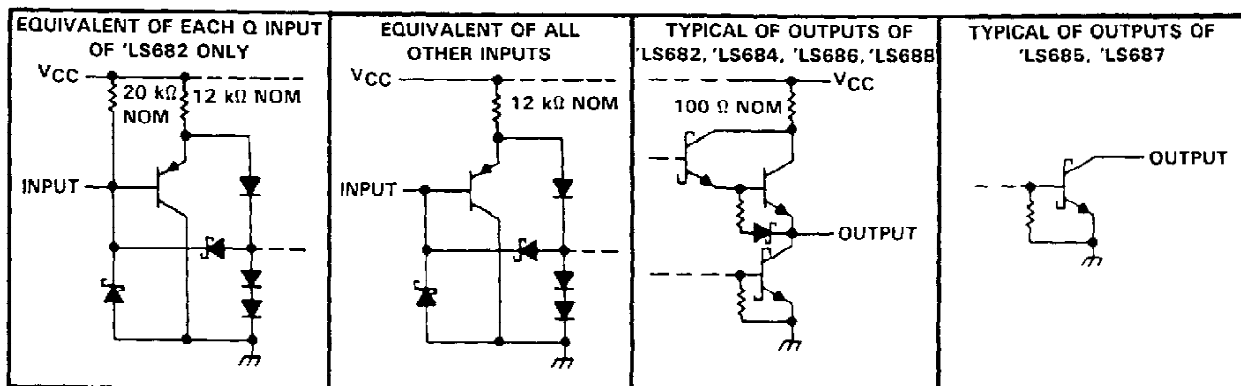
**SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688,
SN74LS682, SN74LS684 THRU SN74LS688
8-BIT MAGNITUDE/IDENTITY COMPARATORS**

logic symbols† (continued)



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, JT, N, and NT packages.

schematics of inputs and outputs

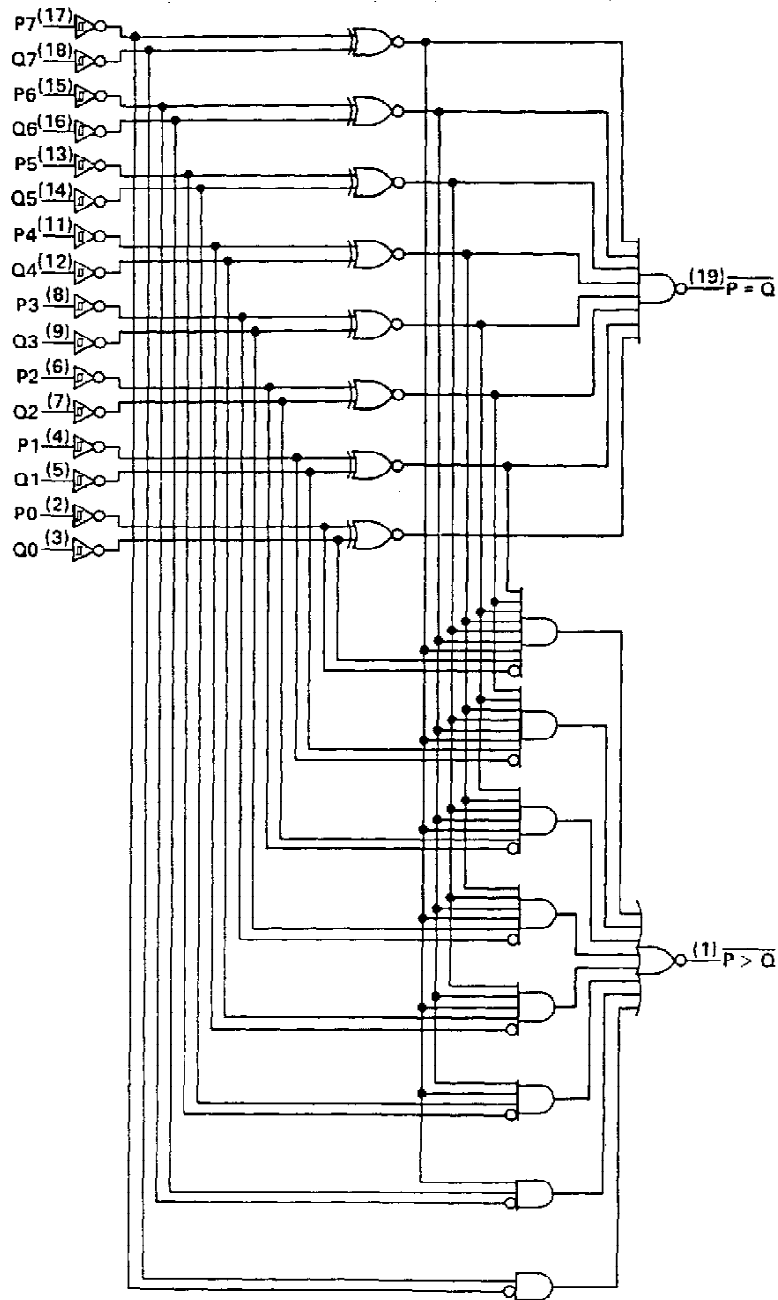


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**SN54LS682, SN54LS684, SN54LS685
SN74LS682, SN74LS684, SN74LS685
8-BIT MAGNITUDE/IDENTITY COMPARATORS**

'LS682, 'LS684, 'LS685 logic diagram (positive logic)



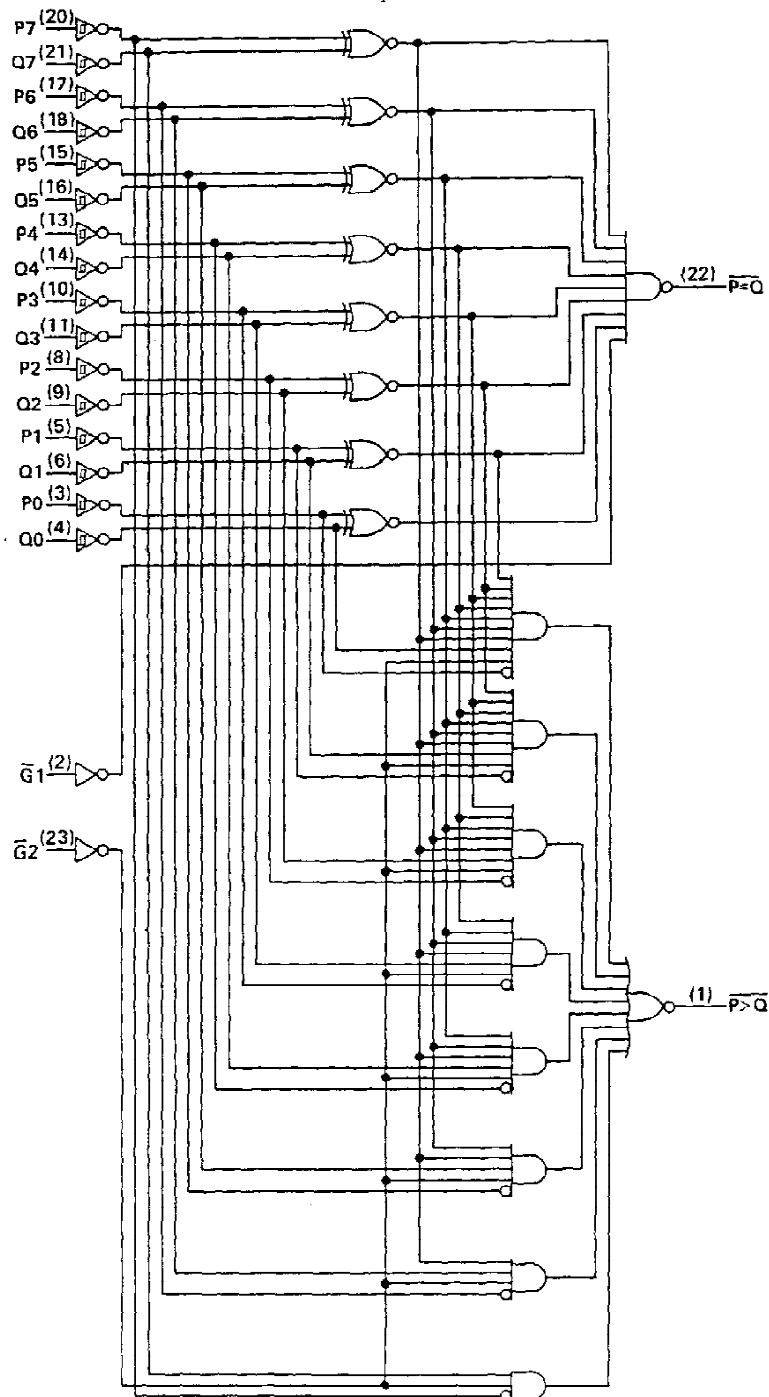
Pin numbers shown are for DW, J, and N packages.

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SN54LS687
SN74LS686, SN74LS687
8-BIT MAGNITUDE/IDENTITY COMPARATORS

'LS686, 'LS687 logic diagram (positive logic)



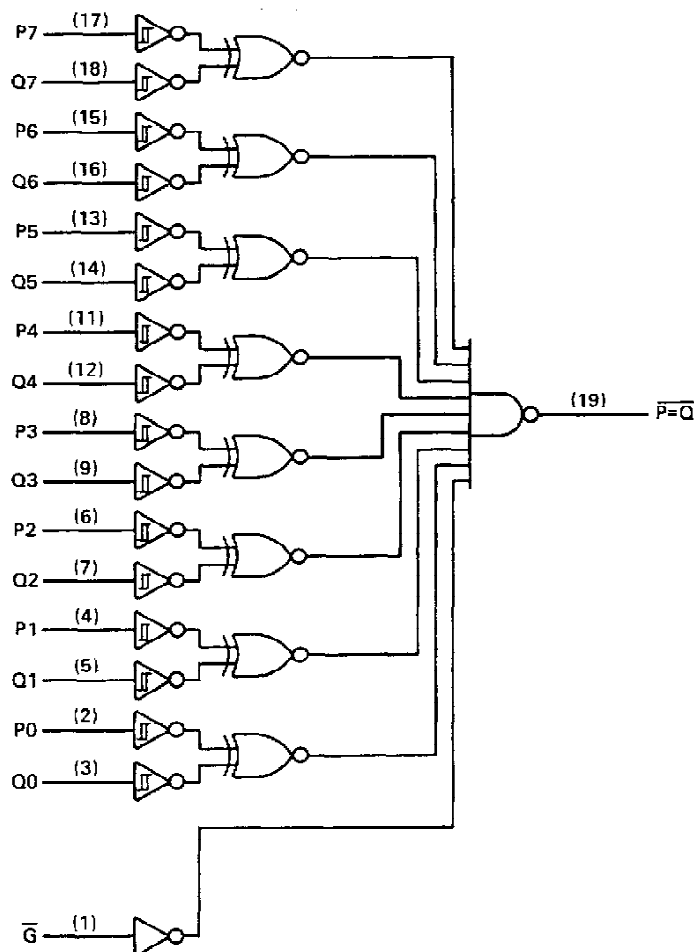
Pin numbers shown are for DW, JT, and NT packages.

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**SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688
SN74LS682, SN74LS684 THRU SN74LS688
8-BIT IDENTITY COMPARATORS**

'LS688 logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: Q inputs of 'LS682	5.5 V
All other inputs	7 V
Off-state output voltage: 'LS685, 'LS687	7 V
Operating free-air temperature range:	
SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688	-55°C to 125°C
SN74LS682, SN74LS684 thru SN74LS688	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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SN54LS682, SN54LS684, SN54LS688
SN74LS682, SN74LS684, SN74LS686, SN74LS688
8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH TOTEM-POLE OUTPUTS

recommended operating conditions

	SN54LS [†]			SN74LS [†]			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.85	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54LS'		SN74LS'		UNIT	
				MIN	TYP‡	MAX	MIN		TYP‡
V _{IH}	High-level input voltage			2		2		V	
V _{IL}	Low-level input voltage			0.7		0.8		V	
V _{T+} - V _{T-}	Hysteresis	P or Q inputs	V _{CC} = MIN	0.4		0.4		V	
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = -18 mA	-1.5		-1.5		V	
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{ILmax} , I _{OH} = -400 μA	2.5		2.7		V	
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{ILmax} , I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V	
			I _{OL} = 24 mA			0.35	0.5		
I _I	Input current at maximum input voltage	Q inputs, 'LS682	V _{CC} = MAX, V _I = 5.5 V		0.1		0.1	mA	
		All other inputs	V _{CC} = MAX, V _I = 7 V						
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7 V		20		20	μA	
I _{IL}	Low-level input current	Q inputs, 'LS682	V _{CC} = MAX, V _I = 0.4 V		-0.4		-0.4	mA	
		All other inputs			-0.2		-0.2		
I _{OS} §	Short-circuit output current		V _{CC} = MAX, V _O = 0		-20	-100	-20	-100	mA
I _{CC}	Supply current	'LS682	V _{CC} = MAX, See Note 1		42	70	42	70	mA
		'LS684			40	65	40	65	
		'LS686			44	75	44	75	
		'LS688			40	65	40	65	

[†] For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

^{\S} Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 1: I_{CC} is measured with any $\bar{Q}$ inputs grounded, all other inputs at 4.5 V, and all outputs open.

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SN54LS682, SN54LS684, SN54LS688
SN74LS682, SN74LS684, SN74LS686, SN74LS688
8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH TOTEM-POLE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER†	FROM (INPUTS)	TO (OUTPUT)	TEST CONDITIONS	'LS682		'LS684		'LS686		'LS688		UNIT
				MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	
tPLH	P	$\overline{P} = \overline{Q}$	RL = 667 Ω, CL = 45 pF, All other inputs low, See Note 2	13	25	15	25	13	25	12	18	ns
tPHL				15	25	17	25	20	30	17	23	
tPLH	Q	$\overline{P} = \overline{Q}$		14	26	16	25	13	25	12	18	ns
tPHL				15	25	15	25	21	30	17	23	
tPLH	$\overline{Q}, \overline{Q}1$	$\overline{P} = \overline{Q}$						11	20	12	18	ns
tPHL								19	30	13	20	
tPLH	P	$\overline{P} > \overline{Q}$		20	30	22	30	19	30			ns
tPHL				15	30	17	30	15	30			
tPLH	Q	$\overline{P} > \overline{Q}$		21	30	24	30	18	30			ns
tPHL				19	30	20	30	19	30			
tPLH	$\overline{Q}2$	$\overline{P} > \overline{Q}$						21	30			ns
tPHL								16	25			

† t_{PLH} = propagation delay time, low-to-high-level outputs; t_{PHL} = propagation delay time, high-to-low-level output.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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SN54LS685, SN54LS687
SN74LS685, SN74LS687, SN74LS688
8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH TOTEM-POLE OUTPUTS

recommended operating conditions

	SN54LS [*]			SN74LS [*]			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.85	5	5.25	V
High-level output current, I_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	SN54LS [*]			SN74LS [*]			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
$V_{T+} - V_{T-}$	Hysteresis	P or Q inputs		0.4			0.4		V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
I_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}, V_{OH} = 5.5 \text{ V}$			250			100	μA
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}, I_{OL} = 12 \text{ mA}$	0.25	0.4		0.25	0.4		V
		$I_{OL} = 24 \text{ mA}$				0.35	0.5		
I_I		$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1			0.1		mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20			20		μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.2			-0.2		mA
I_{CC}	Supply current	'LS685		40	65		40	65	mA
		'LS687		44	75		44	75	

[†]For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

^{*}All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 1: I_{CC} is measure with any $\bar{Q}$ inputs grounded, all other inputs at 4.5 V, and all outputs open.

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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54LS685, SN54LS687

SN74LS685, SN74LS687

8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH OPEN-COLLECTOR OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS685			'LS687			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	P	$\overline{P=Q}$	R _L = 667 Ω, C _L = 45 pF, All other inputs low, See Note 2		30	45		24	35	ns
t _{PHL}					19	35		20	30	
t _{PLH}	Q	$\overline{P=Q}$			24	45		24	35	ns
t _{PHL}					23	35		20	30	
t _{PLH}	$\overline{Q}, \overline{Q1}$	$\overline{P=Q}$						21	35	ns
t _{PHL}								18	30	
t _{PLH}	P	$\overline{P>Q}$			32	45		24	35	ns
t _{PHL}					16	35		16	30	
t _{PLH}	Q	$\overline{P>Q}$			30	45		24	35	ns
t _{PHL}					20	35		16	30	
t _{PLH}	$\overline{Q2}$	$\overline{P>Q}$						24	35	ns
t _{PHL}								15	30	

[†] t_{PLH} = propagation delay time, low-to-high-level outputs; t_{PHL} = propagation delay time, high-to-low-level output.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

TEXAS
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POST OFFICE BOX 655012 • DALLAS, TEXAS 75286

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
8415101RA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8415101RA SNJ54LS682J
8415101SA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8415101SA SNJ54LS682W
84152012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84152012A SNJ54LS 684FK
8415201RA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8415201RA SNJ54LS684J
84153012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84153012A SNJ54LS 688FK
8415301RA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8415301RA SNJ54LS688J
8415301SA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8415301SA SNJ54LS688W
SN54LS682J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS682J
SN54LS682J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS682J
SN54LS684J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS684J
SN54LS684J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS684J
SN54LS688J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS688J
SN54LS688J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS688J
SN74LS682DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	0 to 70	LS682
SN74LS682DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS682
SN74LS682DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS682
SN74LS682N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS682N
SN74LS682N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS682N
SN74LS682NSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS682
SN74LS682NSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS682
SN74LS684DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS684
SN74LS684DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS684

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LS684N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS684N
SN74LS684N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS684N
SN74LS684NSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS684
SN74LS684NSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS684
SN74LS688DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	0 to 70	LS688
SN74LS688DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS688
SN74LS688DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS688
SN74LS688N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS688N
SN74LS688N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS688N
SN74LS688NE4	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS688N
SN74LS688NSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS688
SN74LS688NSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS688
SNJ54LS682J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8415101RA SNJ54LS682J
SNJ54LS682J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8415101RA SNJ54LS682J
SNJ54LS682W	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8415101SA SNJ54LS682W
SNJ54LS682W.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8415101SA SNJ54LS682W
SNJ54LS684FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84152012A SNJ54LS 684FK
SNJ54LS684FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84152012A SNJ54LS 684FK
SNJ54LS684J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8415201RA SNJ54LS684J
SNJ54LS684J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8415201RA SNJ54LS684J
SNJ54LS688FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84153012A SNJ54LS 688FK

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54LS688FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84153012A SNJ54LS 688FK
SNJ54LS688J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8415301RA SNJ54LS688J
SNJ54LS688J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8415301RA SNJ54LS688J
SNJ54LS688W	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8415301SA SNJ54LS688W
SNJ54LS688W.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8415301SA SNJ54LS688W

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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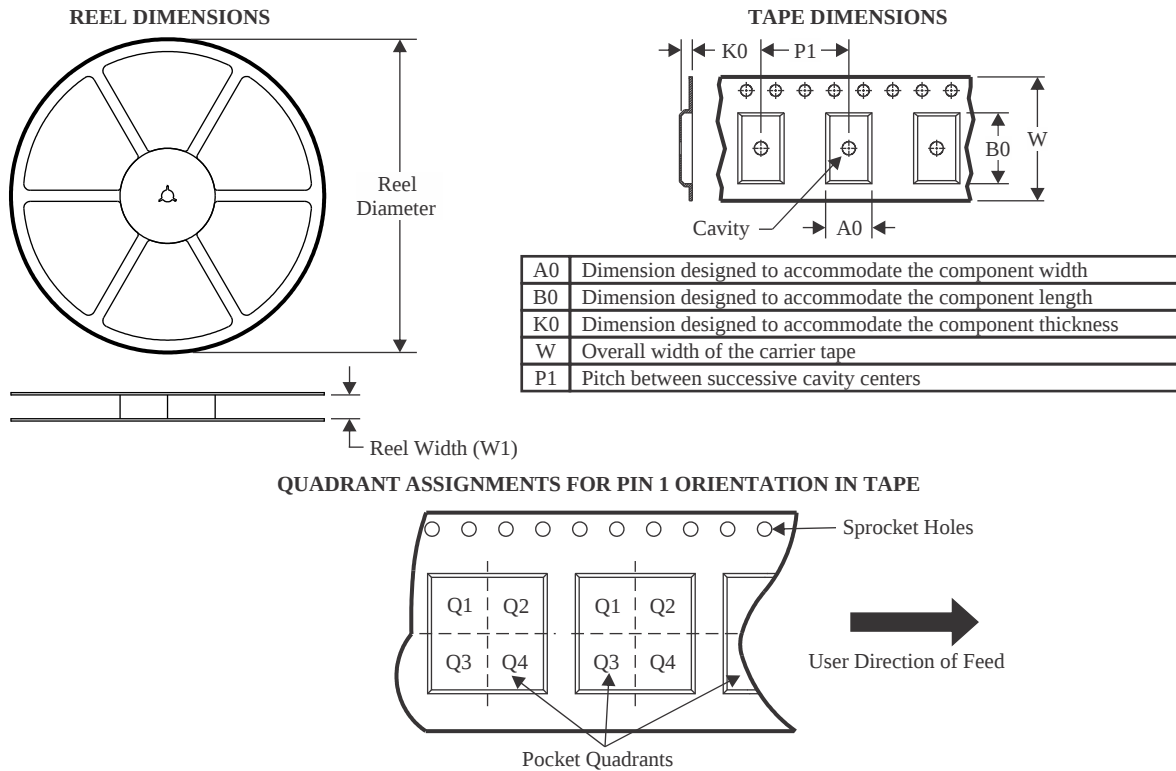
OTHER QUALIFIED VERSIONS OF SN54LS682, SN54LS684, SN54LS688, SN74LS682, SN74LS684, SN74LS688 :

- Catalog : [SN74LS682](#), [SN74LS684](#), [SN74LS688](#)
- Military : [SN54LS682](#), [SN54LS684](#), [SN54LS688](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS682DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS682NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LS684DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS684NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LS688DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LS688NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

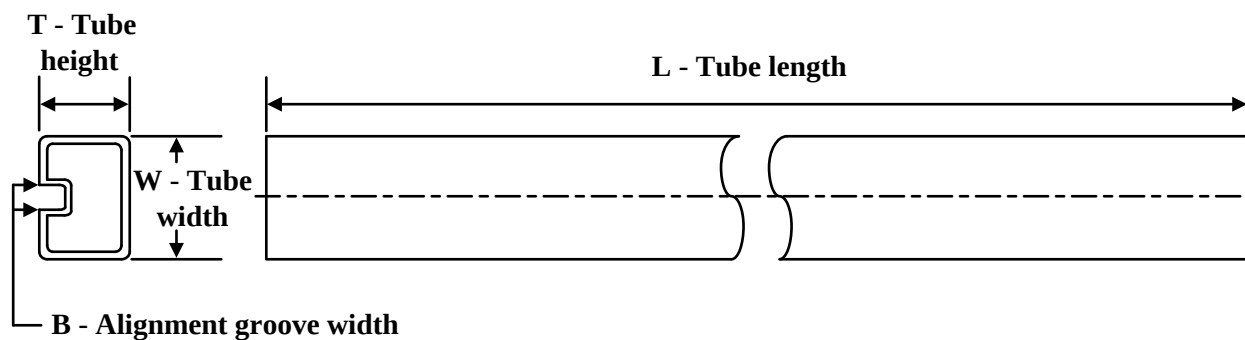
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS682DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LS682NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LS684DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LS684NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LS688DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LS688NSR	SOP	NS	20	2000	356.0	356.0	45.0

TUBE

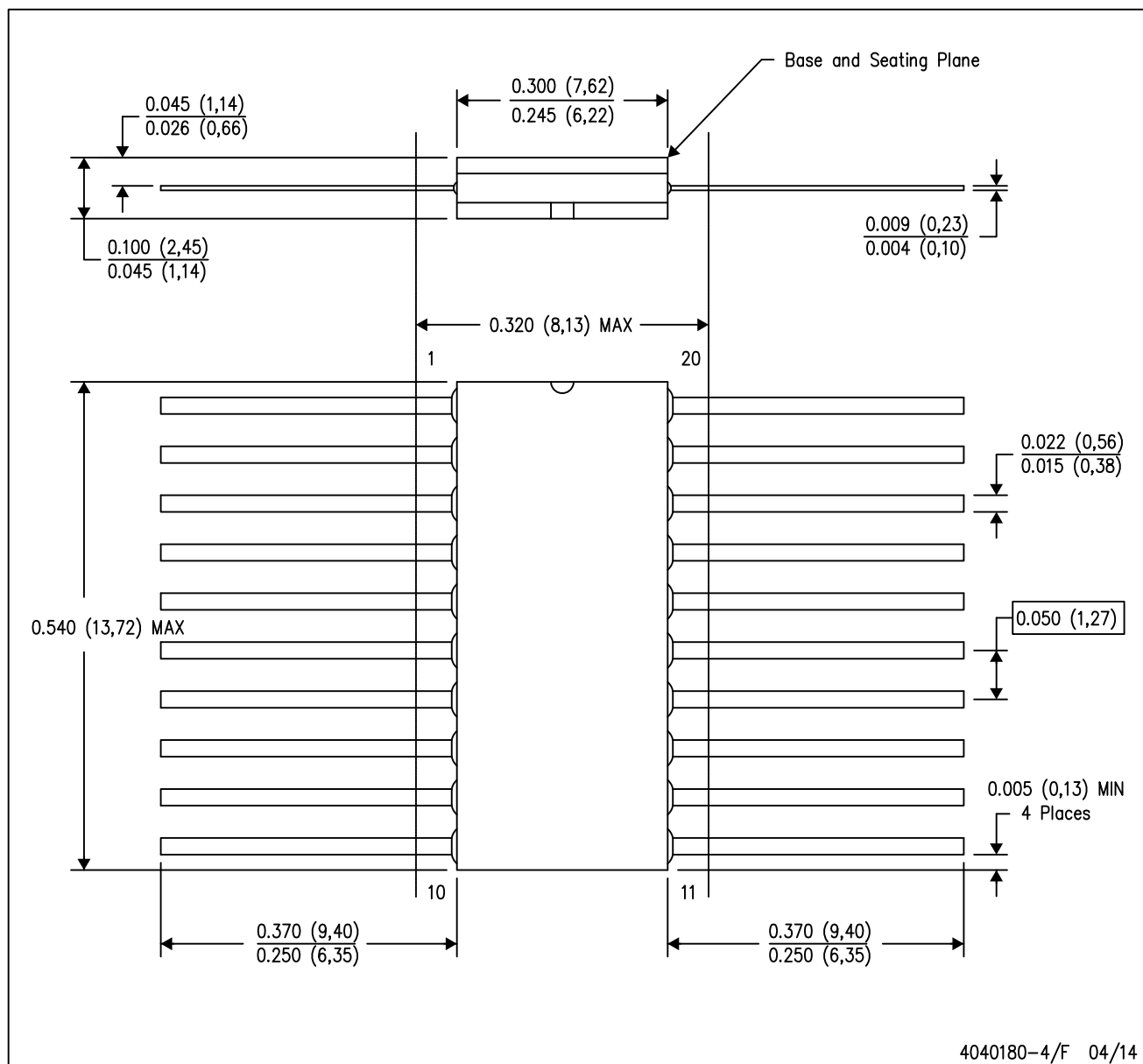


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
8415101SA	W	CFP	20	25	506.98	26.16	6220	NA
84152012A	FK	LCCC	20	55	506.98	12.06	2030	NA
84153012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8415301SA	W	CFP	20	25	506.98	26.16	6220	NA
SN74LS682N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS682N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS684N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS684N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS688N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS688N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS688NE4	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54LS682W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54LS682W.A	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54LS684FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS684FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS688FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS688FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS688W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54LS688W.A	W	CFP	20	25	506.98	26.16	6220	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

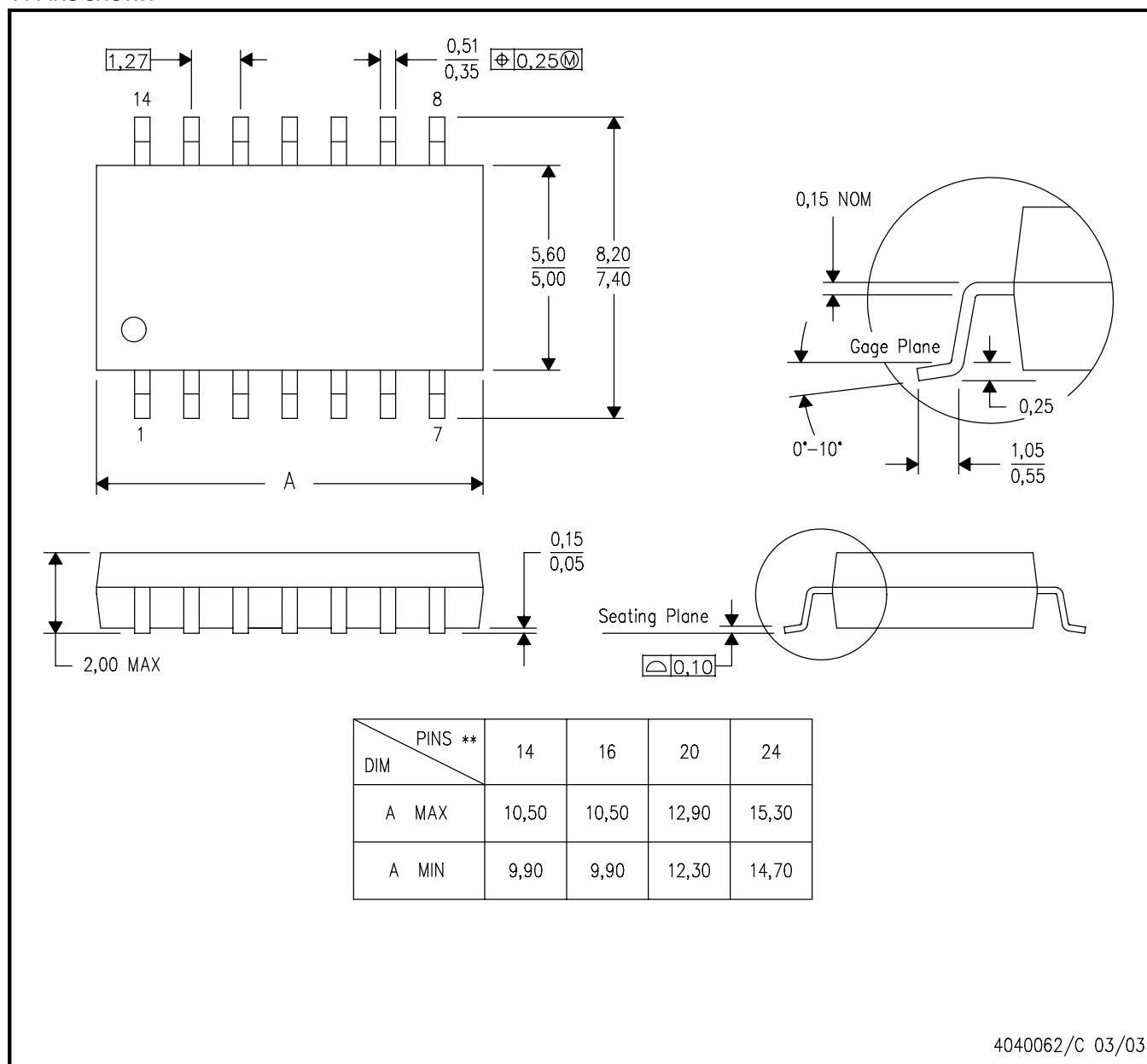
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

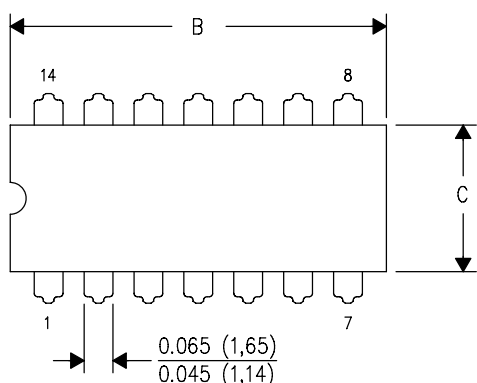


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

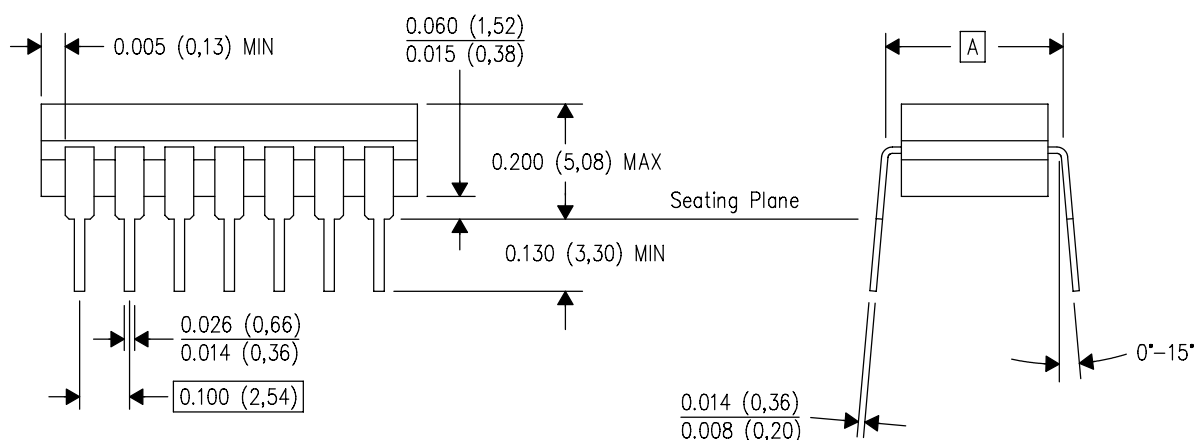
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

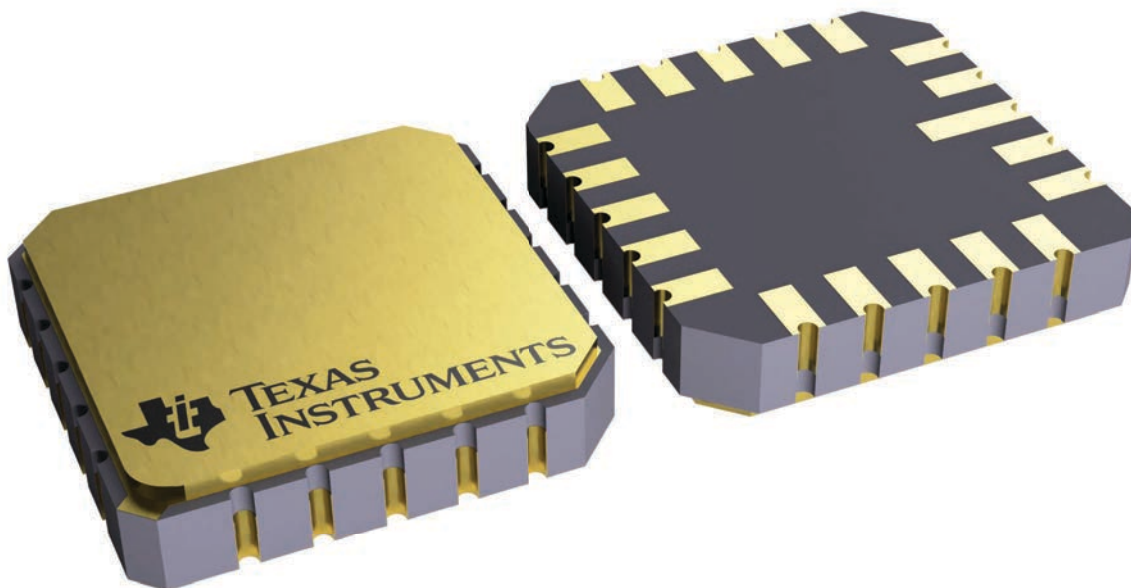
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

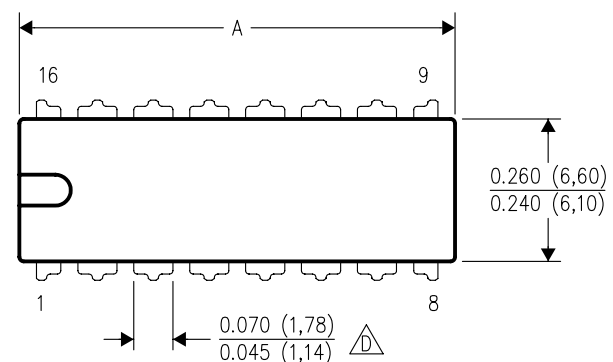


4229370VA\

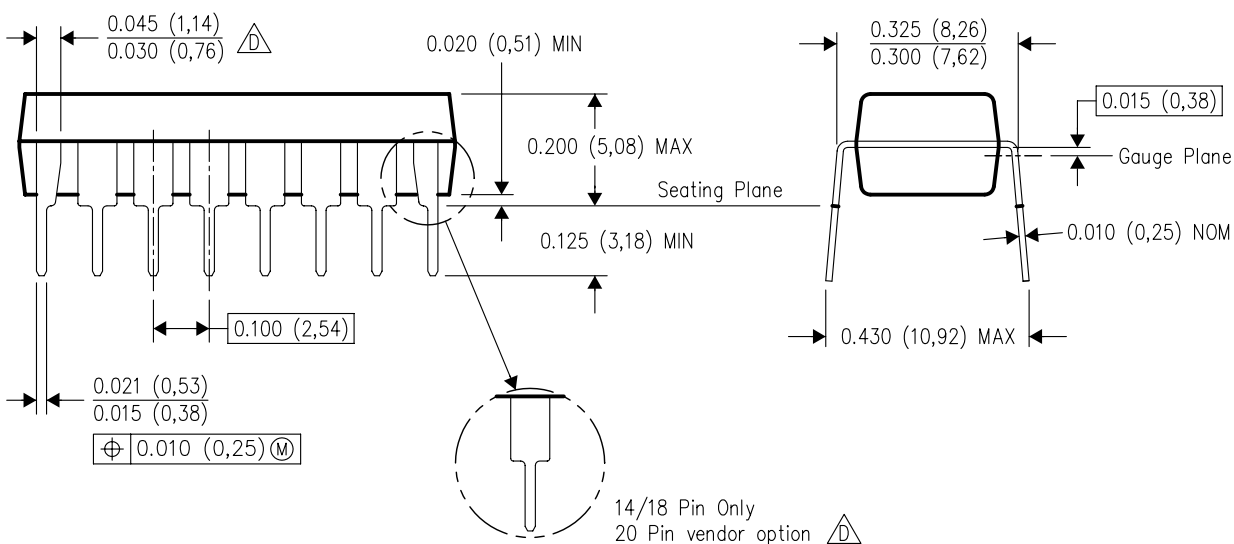
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

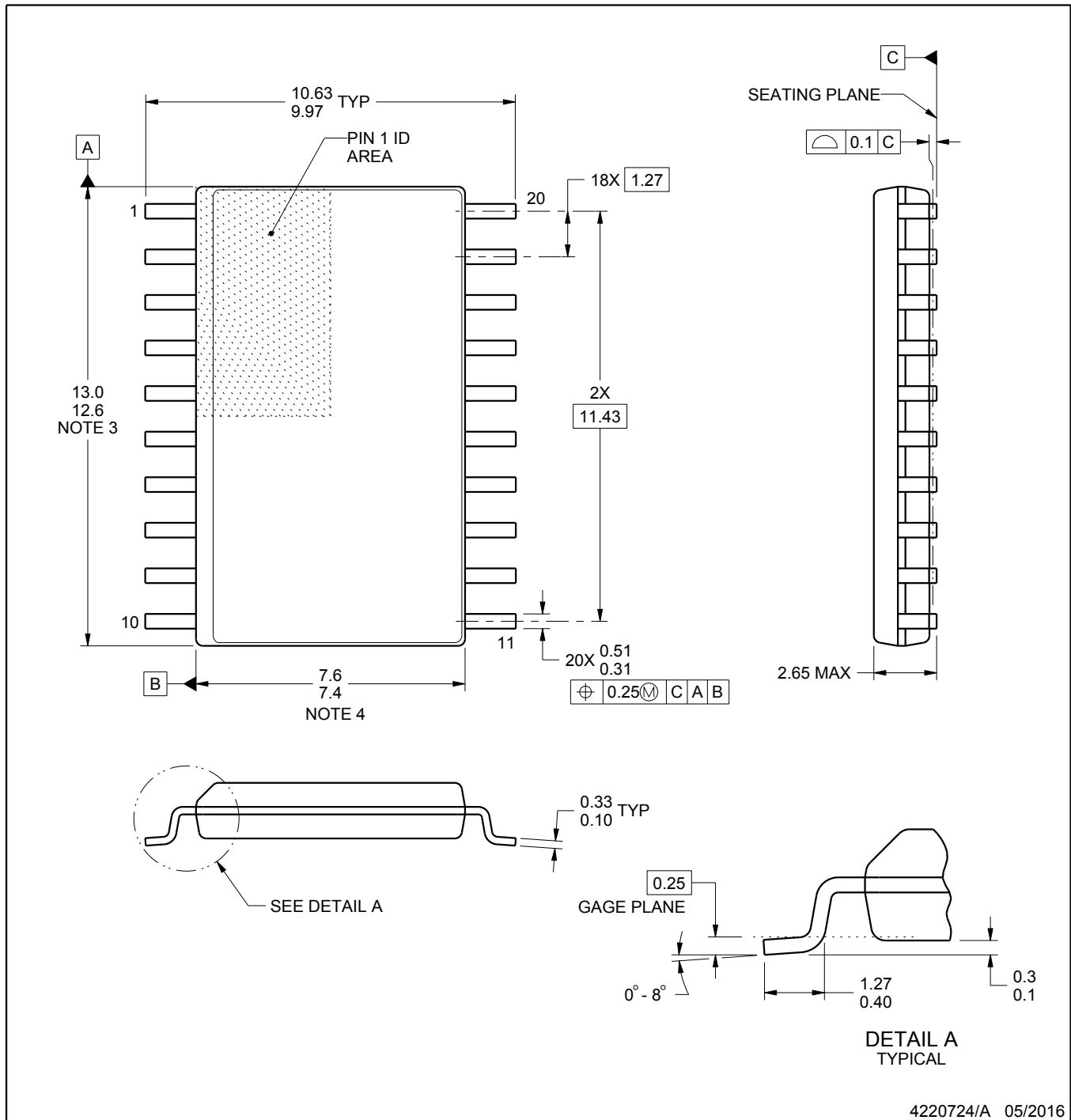
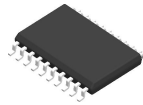


PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



NOTES:

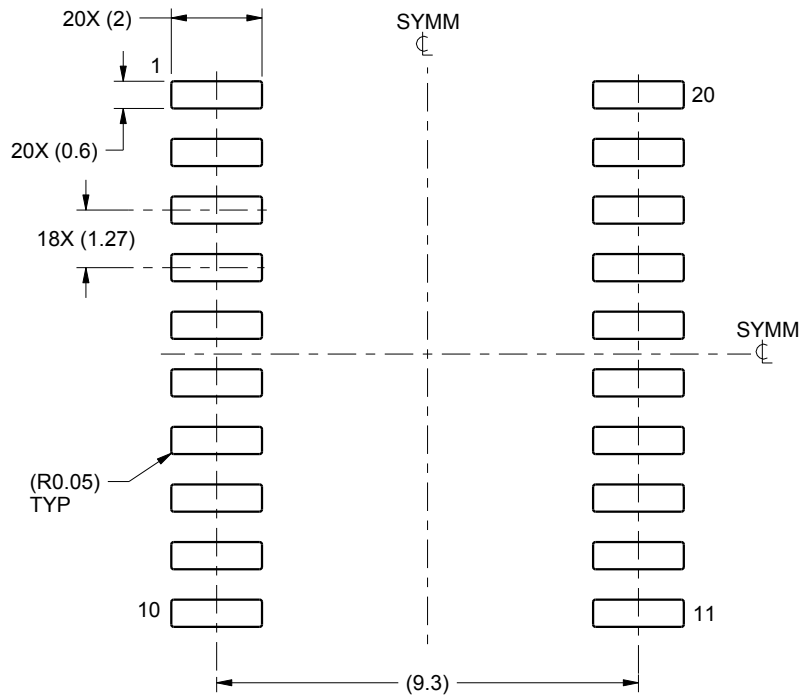
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

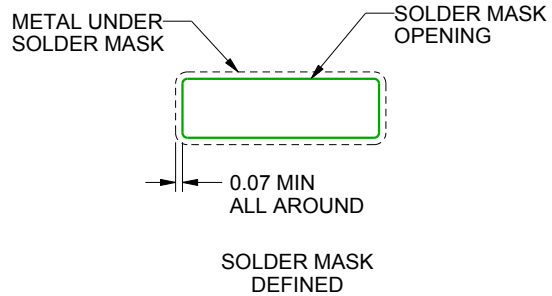
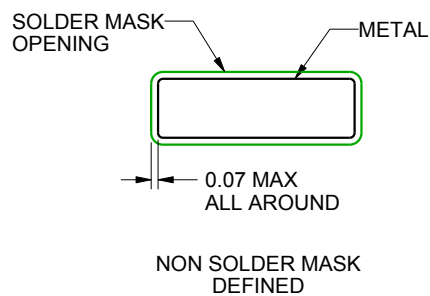
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

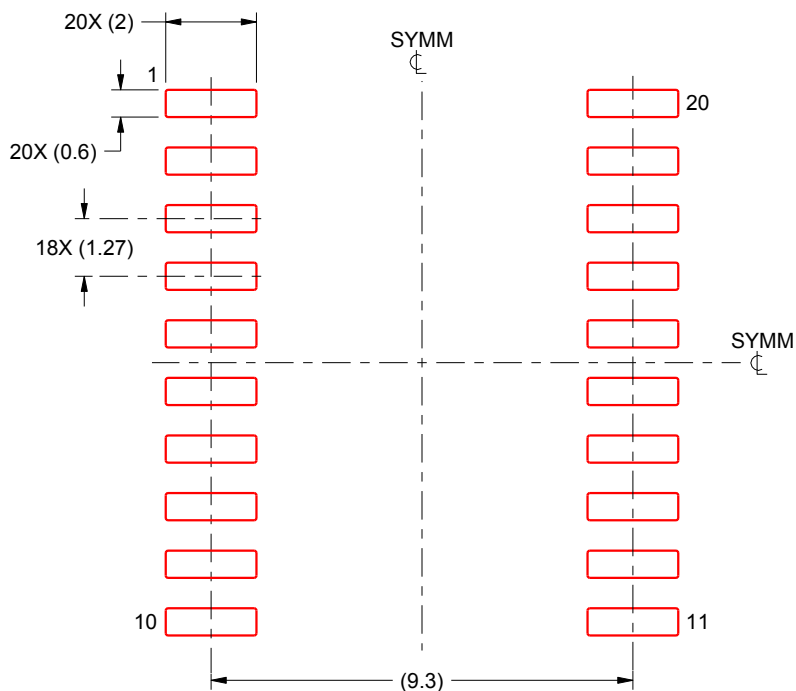
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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