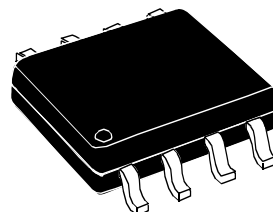


Filtered Video Buffers for STB and DVD Devices

TARGET SPECIFICATION

FEATURES

- Y, C Inputs with 7.1 MHz filters
- 40 dB Stop Band Attenuation at 27 MHz
- RF Signal with 14 dB Notch Filter at 4.5 MHz for Sound Trap
- RF Signal with -170 ns Differential Group Delay between 400 kHz and 3.58 MHz
- 6 dB Gain
- Capabilities of Integrated Output Buffers: Double-adapted Loads (75Ω) on CVBS Output, Single-adapted Loads on Y and C Outputs
- AC-coupled Inputs
- DC-coupled Outputs for Y, CVBS and RFOUT
- DC- or AC-coupled Output for COUT
- Bottom Clamp on Y, Bias Clamp on C
- Crosstalk: 55 dB (typical)



SO8

Order Code: STV6433

DESCRIPTION

The STV6433 is a filtered video output interface for DVD, Satellite and Cable Set-Top Box applications.

After removing D/A conversion noise using integrated low pass filters, the STV6433 adapts the Y and C signals coming from the digital decoder in amplitude and impedance for transmission to the TV set and an auxiliary device (VCR, DVD recorders, etc.) via adapted 75-ohm cables.

A Y+C adder with buffer for providing a CVBS signal to external loads and a pre-processing of a CVBS signal for RF modulator (RFOUT) are included in STV6433.

This pre-processing is a notch filtering at 4.5 MHz (before the addition of the audio signal in the RF modulator) and a 170 ns Y/C delay (to compensate the nominal distortion in the TV IF filter).

The STV6433 is powered by a 5V voltage supply and is fully-compatible with STi55xx digital encoders.

Table of Contents

Chapter 1	Pin Connections	3
Chapter 2	General Information	4
Chapter 3	Electrical Characteristics	5
3.1	Absolute Maximum Ratings	5
3.2	Thermal Data	5
3.3	Electrical Characteristics	5
Chapter 4	Package Mechanical Data	8
Chapter 5	Revision History	9

1 Pin Connections

Figure 1: STV6433 Pinout

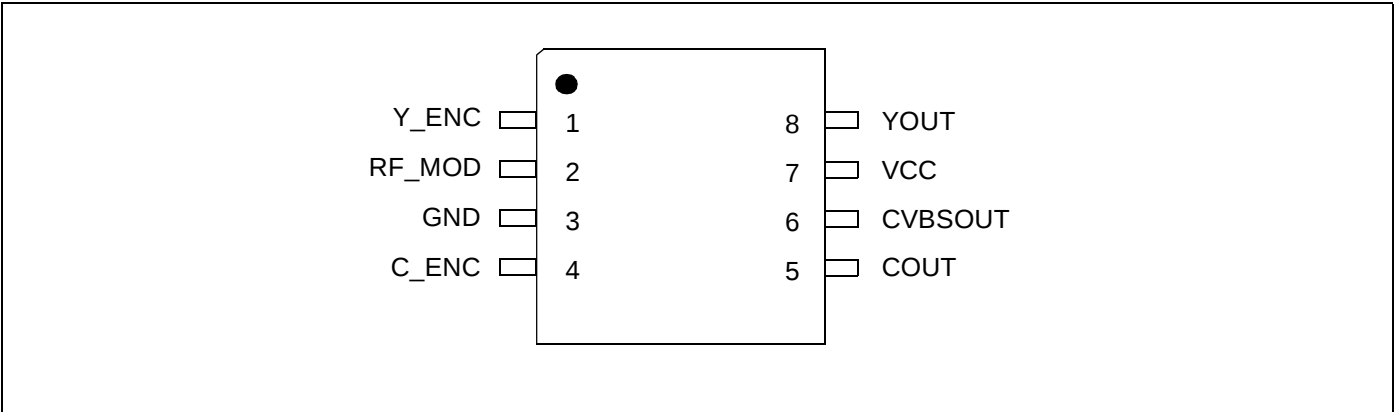
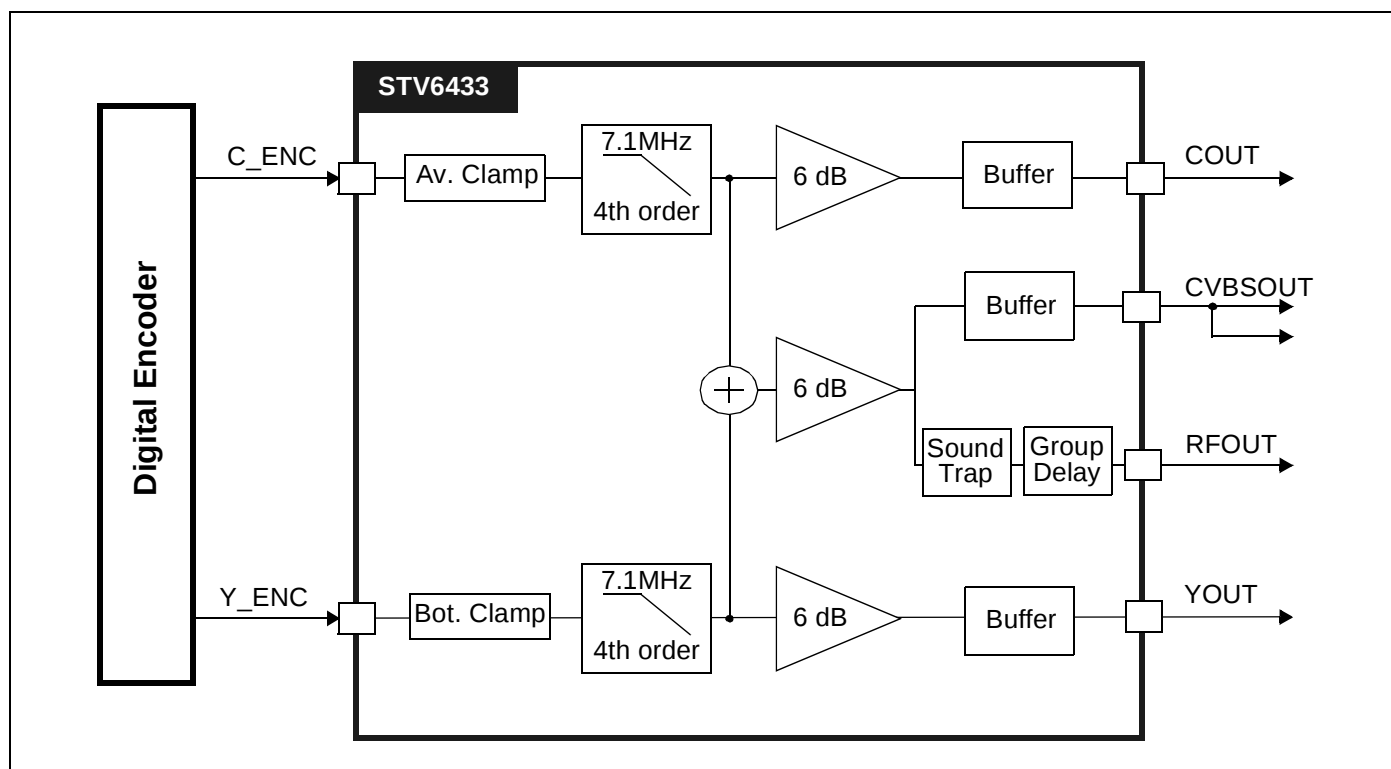


Table 1: STV6433 Pin List

Pin No.	Name	Description
1	Y_ENC	Y Input from Encoder
2	RF_MOD	CVBS Output for RF modulator
3	GND	
4	C_ENC	Chroma Input from Encoder
5	COUT	Chroma Output
6	CVBSOUT	CVBS Output
7	VCC	+5 V Supply
8	YOUT	Y Output

2 General Information

Figure 2: STV6433 Block Diagram



3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Powering	6	V
V_i	Voltage at Pin i to GND	-0.6, V_{CC}	V
V_{ESD}	Maximum ESD voltage allowed. 100 pF capacitor discharged through 1.5 k Ω serial resistor (Human Body Model)	± 4	k
T_{OPER}	Ambient Operating Temperature	0, +70	°C
T_{STG}	Storage Temperature	-55, +150	°C

3.2 Thermal Data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal Resistance (Junction-to-Ambient)	140	°C/W

3.3 Electrical Characteristics

$T_{AMB} = 25^{\circ}\text{C}$, $V_{CC} = 5\text{ V}$, $R_{GENE} = 75\Omega$, $R_{LOAD} (Y, C, CVBS) = 150\Omega$, $R_{LOAD} (RF) = 600\Omega$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating Supply Voltage		4.75	5	5.25	V
I_{CC}	Supply Current (V_{CC})	No Load		30	40	mA
Y and CVBS Section						
V_{DCIN}	DC Input Level, Bottom Clamp Input	Bottom Level		2		V
I_{CLAMP}	Clamping Current, Bottom Clamp Input	at $V_{DCIN} - 400\text{ mV}$	1	2		mA
I_{LEAK}	Input Leakage Current, Bottom Clamp Input	$V_{IN} = V_{DCIN} + 1\text{ V}$		1	10	μA
C_{IN}	Input Capacitance			2		pF
V_{IN}	Maximum Input Signal	$V_{CCV} = 5\text{ V}$			1.5	V_{PP}
DYN	Dynamic Output Signal	$V_{CCV} = 5\text{ V}$			3	V_{PP}
YF1	-1 dB Bandwidth (Flatness) of Y1 and CVBS	1H Signal	4.0	4.5		MHz
YF3	-3 dB Bandwidth of Y1 and CVBS	1H Signal		7.1		MHz
YSBR	Stopband Rejection	27 MHz / 100 kHz		- 40		dB
YOS	Peak Overshoot	2 Vpp Output pulse		5		%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Flatness	Spread of Gain in Video Bands	$V_{IN} = 1 V_{PP}$ Band = 15kHz -5MHz for Y and CVBS			+/-0.5	dB
VCTo	Crosstalk Isolation of Y or CVBS from C	$V_{IN} = 0.5 V_{PP}$ at 3.58 MHz, on C_ENC, $R_{LOAD} = 150\Omega$		55		dB
R _{OUT}	Output Resistance			5	10	W
GY	Gain on Y1, Y2 and CVBS channels	$V_{IN} = 1 V_{PP}$	5.5	6	6.5	dB
DC _{YOUT}	DC Output Voltage (Y and CVBS)	Bottom sync pulse, at IC output pins		0.6		V
DPHI	Differential Phase	$V_{IN} = 1 V_{PP}$ at 3.58 MHz		0.2	3	deg.
DG	Differential Gain	$V_{IN} = 1 V_{PP}$ at 3.58 MHz		0.3	3	%
LNL	Luminance non-linearity			0.5	3	%
VSN	Video S/N Ratio: Y and CVBS channels	NTC-7 weighting 4.4 MHz lowpass		70		dB
Dtpd	Group delay variation from Flatness			9		nS
RFOUT Section						
Tpd	Group Delay RFOUT	f = 3.58 MHz (ref. = 400 kHz)	-205	-170	-135	nS
T _{CLD}	Chroma / Luminance delay	f = 3.58 MHz (ref. = 400 kHz)	-205	-170	-135	nS
DPHIRF	Differential Phase RFOUT	$V_{IN Y,C} = 1 V_{PP}$ at 3.58 MHz		1	3	deg.
DGRF	Differential Gain RFOUT	$V_{IN Y,C} = 1 V_{PP}$ at 3.58 MHz		1.5	3	%
pK	Gain Peaking	f = 2 MHz		0.5	0.75	dB
RFOS	Peak Overshoot	f = 3.58 MHz (ref. = 400 kHz)	-0.5		0.75	dB
AV45	Notch Attenuation	from 4.4 to 4.63 MHz (ref. = 400kHz)	-14			dB
AV42	Notch Attenuation	at 4.2 MHz (ref. = 400 kHz)			-8	dB
RFSN	Video S/N Ratio: RF channel	NTC-7 weighting 4.4 MHz lowpass		60		dB
TPASS	Pass Delay, RFOUT	f = 200 kHz to 3 MHz	-50		+50	nS
Chroma Section						
V _{DCIN}	DC Input Level			3		V
R _{IN}	Input Resistance		30	50		kΩ
C _{IN}	Input Capacitance			2		pF
V _{IN}	Max Input Signal				1	V _{PP}
DYN	Dynamic Output Signal				2	V _{PP}
DC _{COU}	DC Output Voltage (COU)	Without signal		1.6		V
CF1	-1 dB Bandwidth (Flatness)		4	4.5		MHz
CF3	-3 dB Bandwidth			7.1		MHz

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CSBR	Stopband Rejection	$f = 27 \text{ MHz to } 100 \text{ MHz}$		- 40		dB
COS	Peak Overshoot	2Vpp Output pulse		4		%
CCTo	Crosstalk Isolation of C from Y and CVBS Channels	$V_{IN} = 1 V_{PP}$ at 3.58 MHz, on Y or CVBS inputs, $R_{LOAD} = 150\Omega$		55		dB
R_{OUT}	Output Resistance			5	10	W
GC	Gain on C Channel	$V_{IN} = 1 V_{PP}$	5.5	6	6.5	dB
CToYdel	Chroma to Luma Delay, Y/C Source	$V_{IN} = 1 V_{PP} @ 3.58 \text{ MHz},$			20	ns

4 Package Mechanical Data

Figure 3: 8-Pin Small Outline Package (SO8)

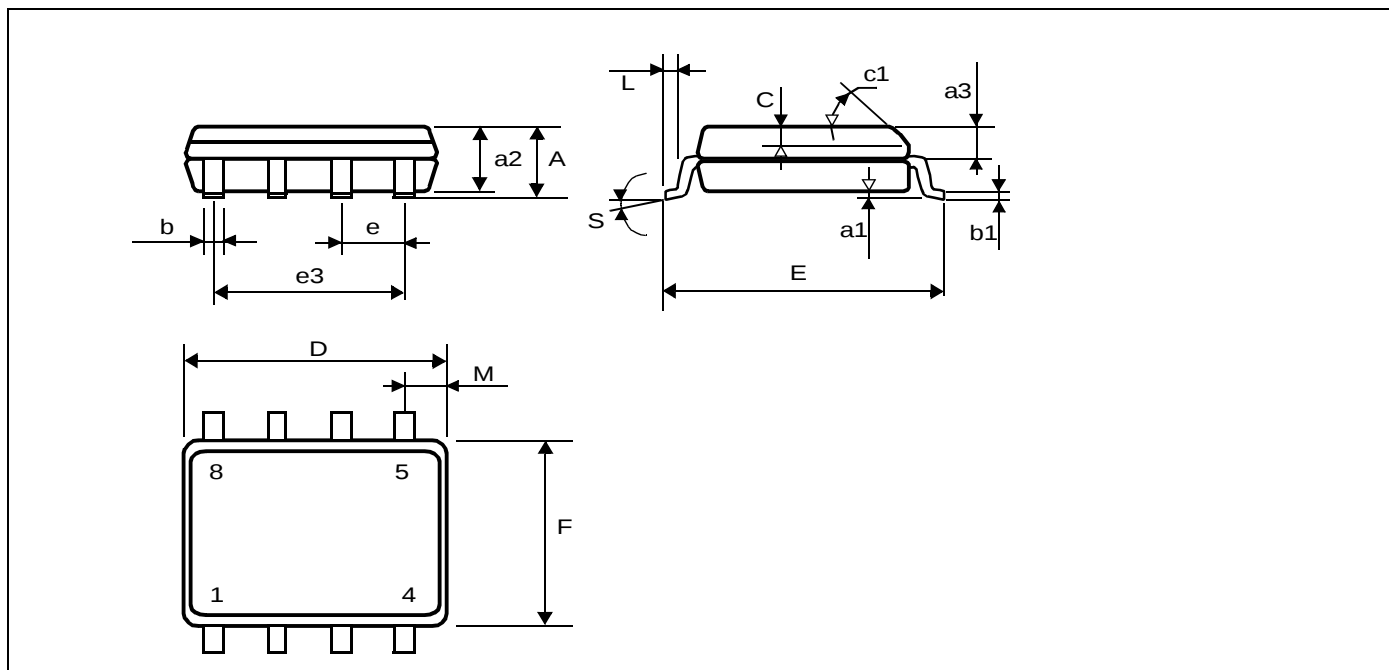


Table 2: SO8 Package Dimensions

Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		1.75				0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.50	0.010		0.020
c1		45°			45°	
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.15		0.157
L	0.40		1.27	0.016		0.050
M			0.60			0.024
S			8°			8°

5 Revision History

Table 3: Summary of Modifications

Revision	Main Changes	Date
1.0	First Issue	March 2002
1.1	Edit of FEATURES on page 1.	January 2003

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

© 2003 STMicroelectronics - All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan
Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

www.st.com