Signetics

Logic Products

74192, 74193, LS192, LS193 Counters

'192 Presettable BCD Decade Up/Down Counter
'193 Presettable 4-Bit Binary Up/Down Counter
Product Specification

FEATURES

- **Synchronous reversible 4-bit binary counting**
- **Asynchronous parallel load**
- **Asynchronous reset (clear)**
- **Expandable without external logic**

DESCRIPTION

The '192 and '193 are 4-bit synchronous up/down counters — the '192 counts in BCD mode and the '193 counts in the binary mode. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either Clock input. If the CP_U clock is pulsed while CP_D is held HIGH, the device will count up . . . if CP_D is pulsed while the CP_U is held HIGH, the device will count down. Only one Clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous reset pin — it may also be loaded in parallel by activating the asynchronous parallel load pin.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
74192	32MHz	65mA
74LS192	32MHz	19mA
74193	32MHz	65mA
74LS193	32MHz	19mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74192N, N74LS192N, N74193N, N74LS193N
Plastic SO	N74LS193D

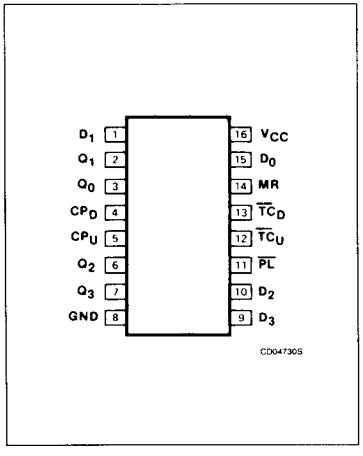
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

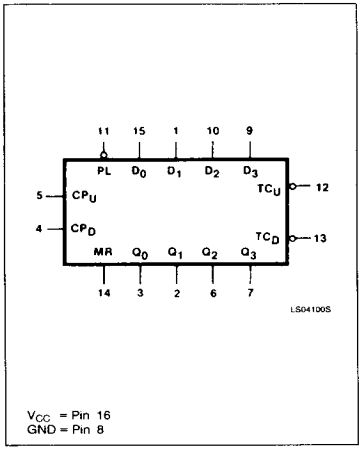
PINS	DESCRIPTION	74	74LS
All	Inputs	1ul	1LSul
All	Outputs	10ul	10LSul

NOTE:
Where a 74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

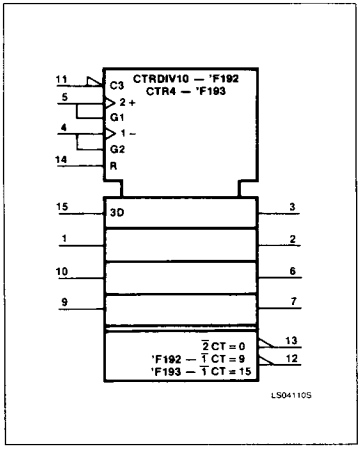
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

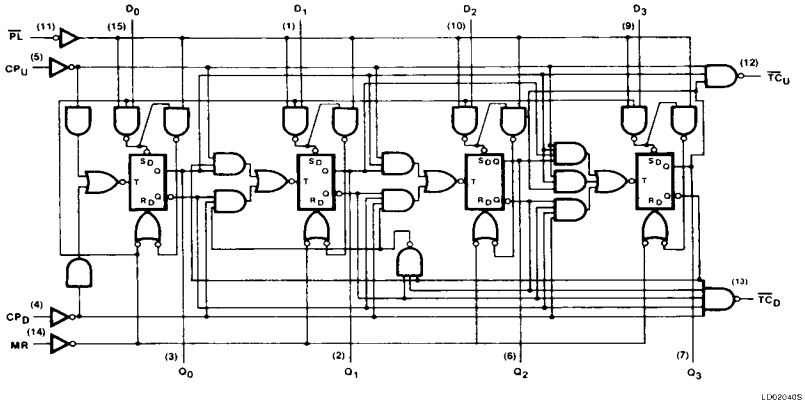
Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the CP_D input will decrease the count by one, while a similar transition on the CPU_U input will advance the count by one.

One clock should be held HIGH while counting with the other, because the circuit will either count by two's or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count down ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state of 9 (for the '192 and 15 for the '193), the next HIGH-to-LOW transition of CP_U will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, duplicating the count up clock, although delayed by two gate delays. Likewise, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the CP_D goes LOW. The $\overline{TC}$ outputs can be used as the Clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a two-gate delay time difference added for each stage that is added.

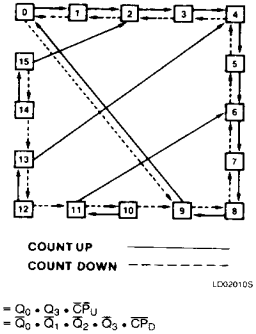
The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel Data inputs ($D_0 - D_3$) is loaded into the counter and appears on the outputs regardless of the conditions of the Clock inputs when the Parallel Load ($\overline{PL}$) input is LOW. A HIGH level on the Master Reset (MR) input will disable the parallel load gates, override both Clock inputs, and set all Q outputs LOW. If one of the Clock input is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

LOGIC DIAGRAM, '192



V_{CC} = Pin 16
GND = Pin 8

STATE DIAGRAM, '192



$\overline{TC}_U = Q_0 \cdot \overline{Q}_3 \cdot \overline{CP}_U$
$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$

Logic Equations For Terminal Count

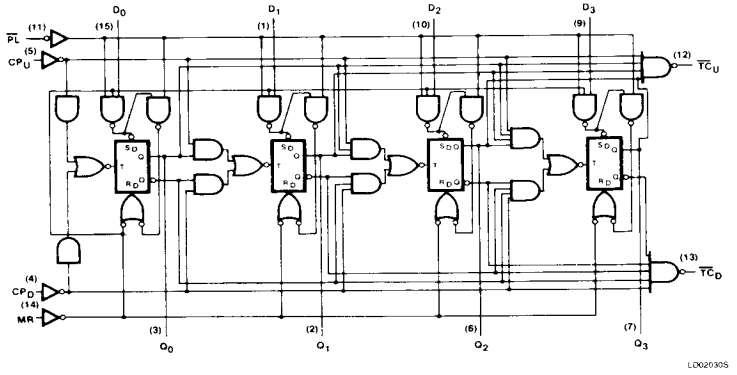
MODE SELECT — FUNCTION TABLE, '192

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	X	X	H	$Q_n = D_n$				L	H
	L	L	H	X	H	X	X	H	$Q_n = D_n$				H	H
Count up	L	H	↑	H	X	X	X	X	Count up				$H^{(a)}$	H
Count down	L	H	H	↑	X	X	X	X	Count down				H	$H^{(b)}$

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH clock transition

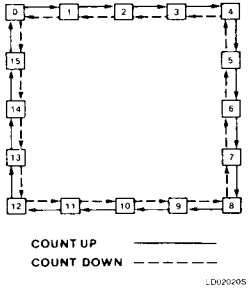
NOTES:
a. $\overline{TC}_U = CP_U$ at terminal count up (HLLH).
b. $\overline{TC}_D = CP_D$ at terminal count down (LLLL).

LOGIC DIAGRAM, '193



V_{CC} = Pin 16
GND = Pin 8

STATE DIAGRAM, '193



$\overline{TC}_U = Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_U$
$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$

Logic Equations For Terminal Count

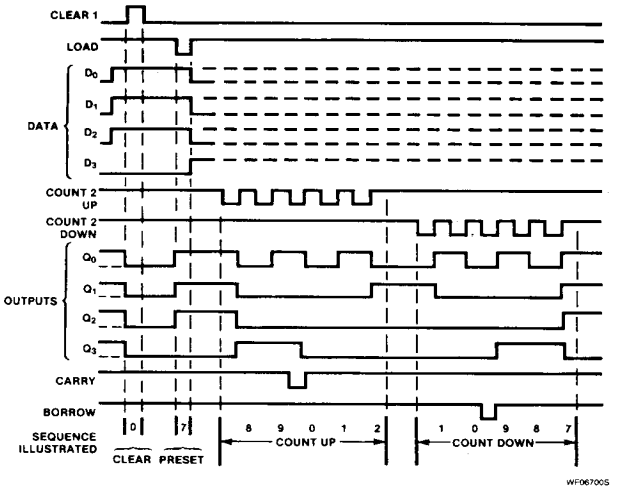
MODE SELECT — FUNCTION TABLE, '193

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	H	H	H	H	L	H
	L	L	H	X	H	H	H	H	H	H	H	H	H	H
Count up	L	H	↑	H	X	X	X	X	Count up				$H^{(c)}$	H
Count down	L	H	H	↑	X	X	X	X	Count down				H	$H^{(d)}$

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH clock transition

NOTES:
c. $TC_U = CP_U$ at terminal count up (HHHH).
d. $TC_D = CP_D$ at terminal count down (LLLL).

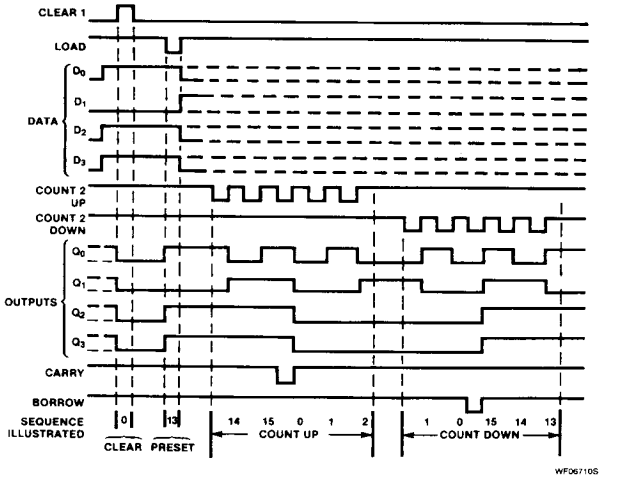
FUNCTIONAL WAVEFORMS (Typical clear, load, and count sequences)



NOTES:
1. Clear overrides load, data, and count inputs.
2. When counting up, count-down input must be high; when counting down, count-up input must be high.

'192 Decade Counter

FUNCTIONAL WAVEFORMS (Typical clear, load, and count sequences)



NOTES:
1. Clear overrides load, data, and count inputs.
2. When counting up, count-down input must be high; when counting down, count-up input must be high.

'193 Binary Counter

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8	V
I_{IK}	Input clamp current			−12			−18	mA
I_{OH}	HIGH-level output current			−800			−400	mA
I_{OL}	LOW-level output current			16			8	mA
T_A	Operating free-air temperature	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74192, '193			74LS192, '193			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA (74LS)					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.5			−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V			1.0				mA
			V_I = 7.0V						0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V			40				=mμA
			V_I = 2.7V						20	=mμA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V				−1.6			−0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−18		−65	−20		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			65	102		19	34	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with Parallel Load and Master Reset inputs grounded, all other outputs at 4.5V and all outputs open.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

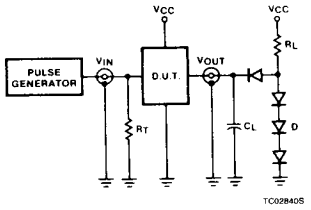
PARAMETER		TEST CONDITIONS	74		74LS		UNIT
			$C_L = 15pF$, $R_L = 400\Omega$		$C_L = 15pF$, $R_L = 2k\Omega$		
			Min	Max	Min	Max	
f_{MAX}	Maximum input count frequency	Waveform 1	25		25		MHz
t_{PLH} t_{PHL}	Propagation delay CP_U input to $\overline{TC}_U$ output	Waveform 2		26 24		26 24	ns
t_{PLH} t_{PHL}	Propagation delay CP_D input to $\overline{TC}_D$ output	Waveform 2		24 24		24 24	ns
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to Q_n outputs	Waveform 1		38 47		38 47	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ input to Q_n output	Waveform 3		40 40		40 40	ns
t_{PHL}	Propagation delay, MR to output	Waveform 4		35		35	ns

NOTE:
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

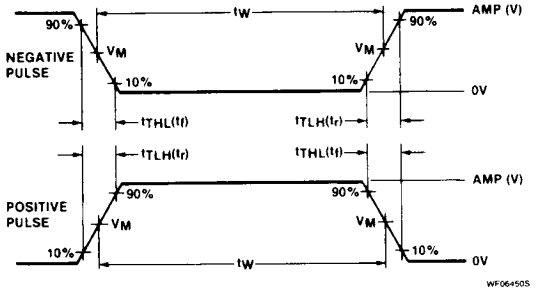
AC SET-UP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	74		74LS		UNIT
			Min	Max	Min	Max	
t_W	CP_U pulse width	Waveform 1	20		20		ns
t_W	CP_D pulse width	Waveform 1	20		20		ns
t_W	$\overline{PL}$ pulse width	Waveform 3	20		20		ns
t_W	MR pulse width	Waveform 4	20		20		ns
t_s	Set-up time, data to $\overline{PL}$	Waveform 5	20		20		ns
t_h	Hold time, data to $\overline{PL}$	Waveform 5	0		5		ns
t_{rec}	Recovery time, $\overline{PL}$ to CP	Waveform 3	40		40		ns
t_{rec}	Recovery time, MR to CP	Waveform 4	40		40		ns

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Totem-Pole Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

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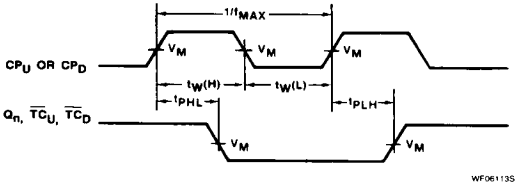
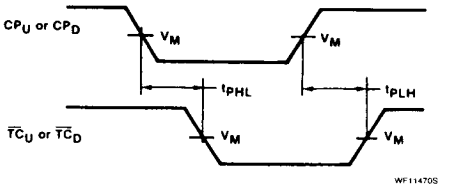
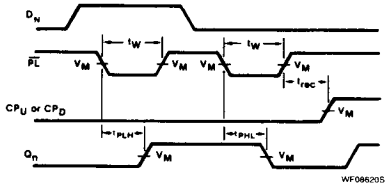
AC WAVEFORMS



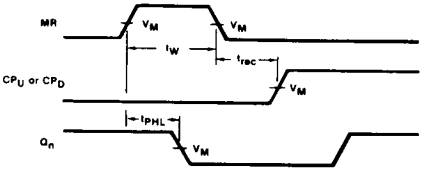
Waveform 1. Clock To Output Delays And Clock Pulse Width



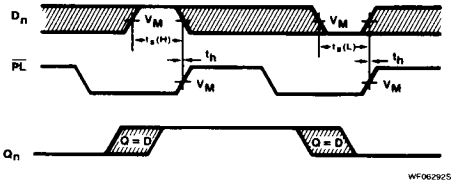
Waveform 2. Clock To Terminal Count Delays



Waveform 3. Parallel Load Pulse Width, Parallel Load To Output Delays, And Parallel Load To Clock Recovery Time



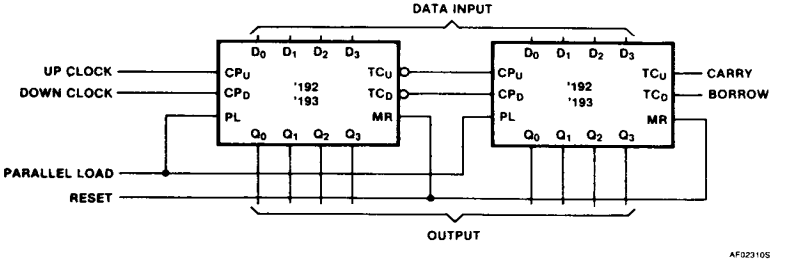
Waveform 4. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



For all waveforms, V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 5. Set-up And Hold Times Data To Parallel Load (PL)

APPLICATION DIAGRAM



8-Bit Up/Down Counter With Parallel Load