

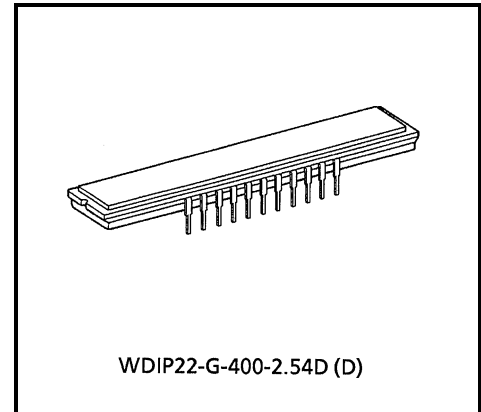
TOSHIBA CCD IMAGE SENSOR CCD (Charge Coupled Device)

## TCD2901D

The TCD2901D is a high sensitive and low dark current 10550 elements×3 line CCD color image sensor which includes CCD drive circuit and clamp circuit. The sensor is designed for scanner. The device contains a row of 10550 elements×3 line photodiodes which provide a 48 lines / mm (1200DPI) across a A4 size paper. The device is operated by 5 V pulse, and 12 V power supply.

### FEATURES

- Number of Image Sensing Elements : 10550 elements×3 line
- Image Sensing Element Size : 4μm by 4μm on 4μm centers
- Photo Sensing Region : High sensitive and low dark current PN photodiode
- Distance Between Photodiode Array : 48μm (12 lines)
- Clock : 2 phase (5 V)
- Power Supply : 12 V Power Supply Voltage
- Internal Circuit : Clamp circuit
- Package : 22 pin CERDIP package
- Color Filter : Red, Green, Blue



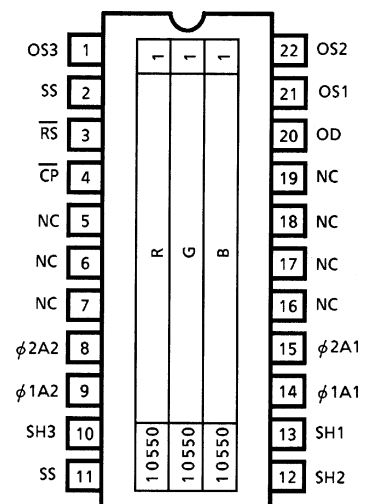
Weight: 5.2g (Typ.)

### MAXIMUM RATINGS (Note 1)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Clock Pulse Voltage	$V_{\phi A}$	-0.3~8	V
Shift Pulse Voltage	$V_{SH}$		
Reset Pulse Voltage	$V_{RS}$		
Clamp Pulse Voltage	$V_{CP}$		
Power Supply Voltage	$V_{OD}$	-0.3~15	V
Operating Temperature	$T_{opr}$	0~60	°C
Storage Temperature	$T_{stg}$	-25~85	°C

Note 1: All voltage are with respect to SS terminals (Ground).

### PIN CONNECTION

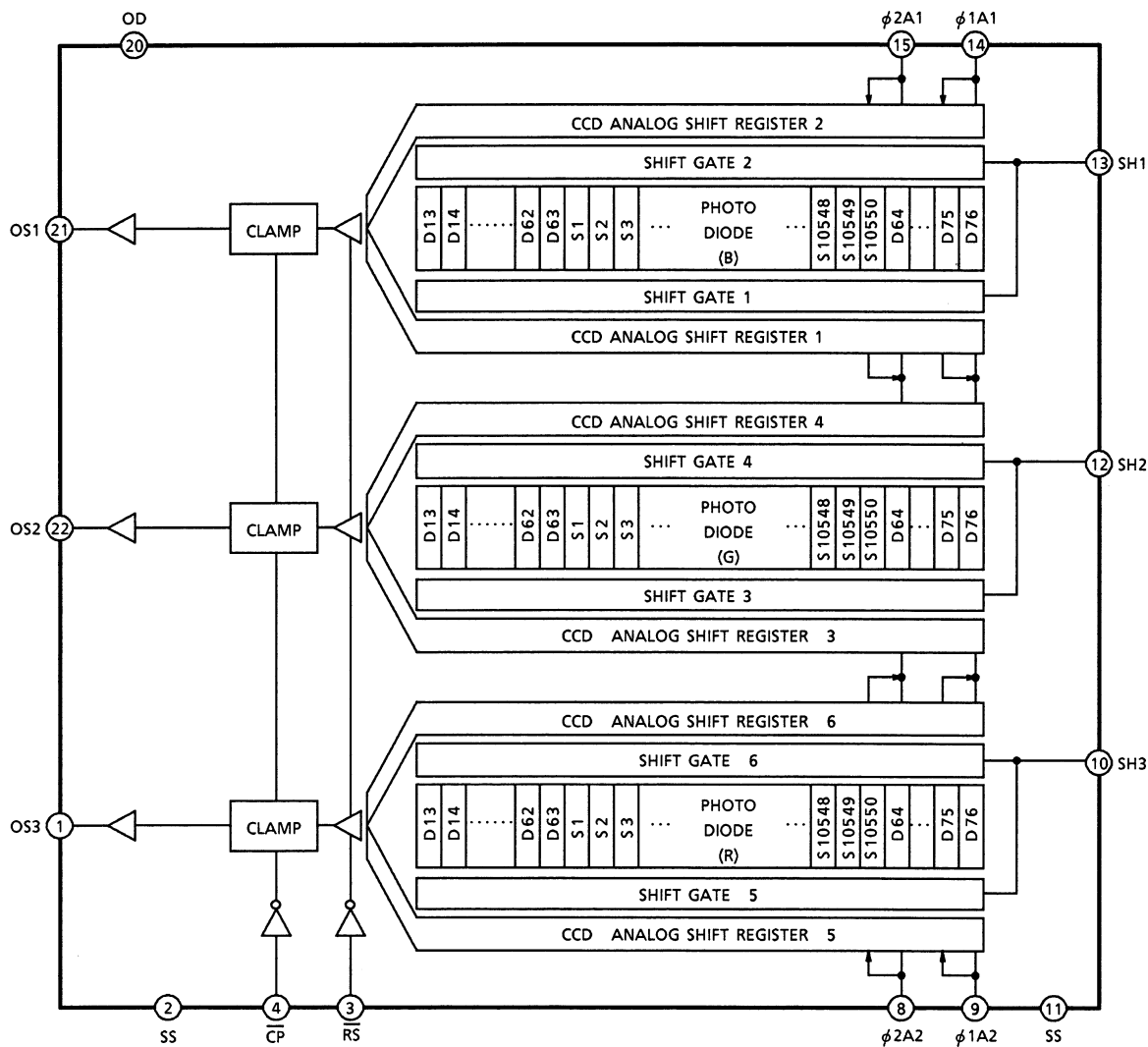


(TOP VIEW)

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CIRCUIT DIAGRAM



PIN NAMES

PIN No.	SYMBOL	NAME	PIN No.	SYMBOL	NAME
1	OS3	Signal Output 3 (Red)	22	OS2	Signal Output 2 (Green)
2	SS	Ground	21	OS1	Signal Output 1 (Blue)
3	RS	Reset Gate	20	OD	Power
4	CP	Clamp Gate	19	NC	Non Connection
5	NC	Non Connection	18	NC	Non Connection
6	NC	Non Connection	17	NC	Non Connection
7	NC	Non Connection	16	NC	Non Connection
8	$\Phi 2A2$	Clock 2 (Phase 2)	15	$\Phi 2A1$	Clock 1 (phase 2)
9	$\Phi 1A2$	Clock 2 (Phase 1)	14	$\Phi 1A1$	Clock 1 (phase 1)
10	SH3	Shift Gate 3	13	SH1	Shift Gate 1
11	SS	Ground	12	SH2	Shift Gate 2

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## OPTICAL / ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V<sub>OD</sub> = 12 V, V<sub>φ</sub> = V<sub>SH</sub> = V<sub>RS</sub> = V<sub>CP</sub> = 5 V (PULSE), f<sub>φ</sub> = 0.5MHz, f<sub>RS</sub> = 1 MHz, t<sub>INT</sub> = 11 ms, LIGHT SOURCE = A LIGHT SOURCE+CM500S FILTER (t = 1 mm), LOAD RESISTANCE = 100 kΩ)

CHARACTERISTIC		SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Sensitivity	Red	R <sub>(R)</sub>	1.7	2.5	3.3	V / (lx·s)	(Note 2)
	Green	R <sub>(G)</sub>	1.6	2.4	3.2		
	Blue	R <sub>(B)</sub>	0.9	1.4	1.9		
Photo Response Non Uniformity		PRNU (1)	—	15	20	%	(Note 3)
		PRNU (3)	—	3	12	mV	(Note 4)
Register Imbalance		RI	—	1	—	%	(Note 5)
Saturation Output Voltage		V <sub>SAT</sub>	2.9	3.5	—	V	(Note 6)
Saturation Exposure		SE	0.91	1.46	—	lx·s	(Note 7)
Dark Signal Voltage		V <sub>DRK</sub>	—	0.5	2.0	mV	(Note 8)
Dark Signal Non Uniformity		DSNU	—	2.0	7.0	mV	(Note 8)
DC Power Dissipation		P <sub>D</sub>	—	260	450	mW	
Total Transfer Efficiency		TTE	92	98	—	%	
Output Impedance		Z <sub>O</sub>	—	0.3	1.0	kΩ	
DC Compensation Output Voltage		V <sub>OS</sub>	4.0	5.0	6.0	V	(Note 9)
Random Noise		N <sub>Dσ</sub>	—	0.8	—	mV	(Note 10)
Reset Noise		V <sub>RSN</sub>	—	0.3	1.0	V	(Note 9)
Masking Noise		V <sub>MS</sub>	—	0.2	1.0	V	(Note 9)

Note 2: Sensitivity is defined for each color of signal outputs average when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

Note 3: PRNU (1) is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

$$\text{PRNU}(1) = \frac{\Delta\bar{\chi}}{\bar{\chi}} \times 100(\%)$$

Where  $\bar{\chi}$  is average of total signal output and  $\Delta\bar{\chi}$  is the maximum deviation from  $\bar{\chi}$ . The amount of incident light is shown below.

$$\begin{aligned}\text{Red} &= 1/2 \cdot \text{SE} \\ \text{Green} &= 1/2 \cdot \text{SE} \\ \text{Blue} &= 1/4 \cdot \text{SE}\end{aligned}$$

Note 4: PRNU (3) is defined as maximum voltage with next pixels, where measured at 5% of SE (Typ.).

Note 5: Register imbalance is defined as follows.

$$\text{RI} = \frac{\sum_{n=1}^{10549} |\chi_n - \chi_{(n+1)}|}{10549 \cdot \bar{\chi}} \times 100(\%)$$

Note 6:  $V_{SAT}$  is defined as minimum saturation output of all effective pixels.

Note 7: Definition of SE

$$SE = \frac{V_{SAT}}{R_G} (lx \cdot s)$$

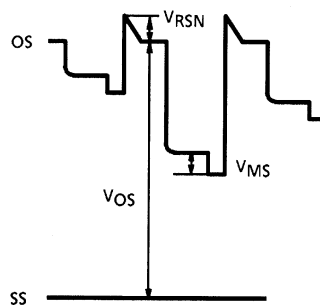
Note 8:  $V_{DRK}$  is defined as average dark signal voltage of all effective pixels.

DSNU is defined as different voltage between  $V_{DRK}$  and  $V_{MDK}$  when  $V_{MDK}$  is maximum dark signal voltage.

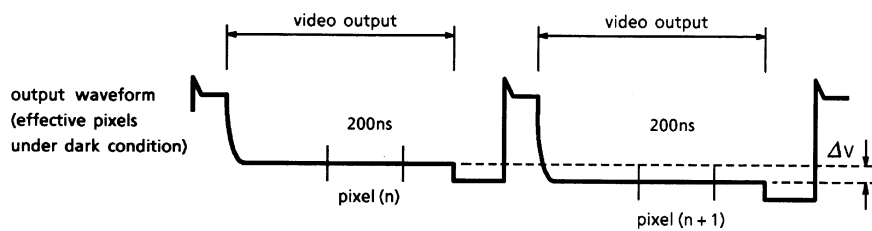


Note 9: DC signal output voltage is defined as follows.

Reset Noise Voltage is defined as follows.



Note 10: Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark conditions) calculated by the following procedure.



- 1) Two adjacent pixels (pixel n and n+1) in one reading are fixed as measurement points.
- 2) Each of the output level at video output periods averaged over 200ns period to get V (n) and V (n+1).
- 3) V (n+1) is subtracted from V (n) to get  $\Delta V$ .

$$\Delta V = V(n) - V(n+1)$$

- 4) The standard deviation of  $\Delta V$  is calculated after procedure 2) and 3) are repeated 30 times (30 readings).

$$\Delta V = \frac{1}{30} \sum_{i=1}^{30} |\Delta V_i| \quad \sigma = \sqrt{\frac{1}{30} \sum_{i=1}^{30} (|\Delta V_i| - \overline{\Delta V})^2}$$

- 5) Procedure 2), 3) and 4) are repeated 10 times to get sigma value.
- 6) 10 sigma values are averaged.

$$\bar{\sigma} = \frac{1}{10} \sum_{j=1}^{10} \sigma_j$$

- 7)  $\bar{\sigma}$  value calculated using the above procedure is observed  $\sqrt{2}$  times larger than that measured relative to the ground level. So we specify random noise as follows.

$$ND\sigma = \frac{1}{\sqrt{2}} \bar{\sigma}$$

## OPERATING CONDITION

CHARACTERISTIC		SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Clock Pulse Voltage	"H" Level	$V_{\phi A}$	4.75	5.0	5.5	V	
	"L" Level		0	—	0.3		
Shift Pulse Voltage	"H" Level	$V_{SH}$	$V_{\phi A} \text{ "H"} - 0.5$	$V_{\phi A} \text{ "H"}$	$V_{\phi A} \text{ "H"}$	V	(Note 11)
	"L" Level		0	0	0.5		
Reset Pulse Voltage	"H" Level	$\overline{V_{RS}}$	4.5	5.0	5.5	V	
	"L" Level		0	0	0.5		
Clamp Pulse Voltage	"H" Level	$\overline{V_{CP}}$	4.5	5.0	5.5	V	
	"L" Level		0	0	0.5		
Power Supply Voltage		$V_{OD}$	11.4	12.0	13.0	V	

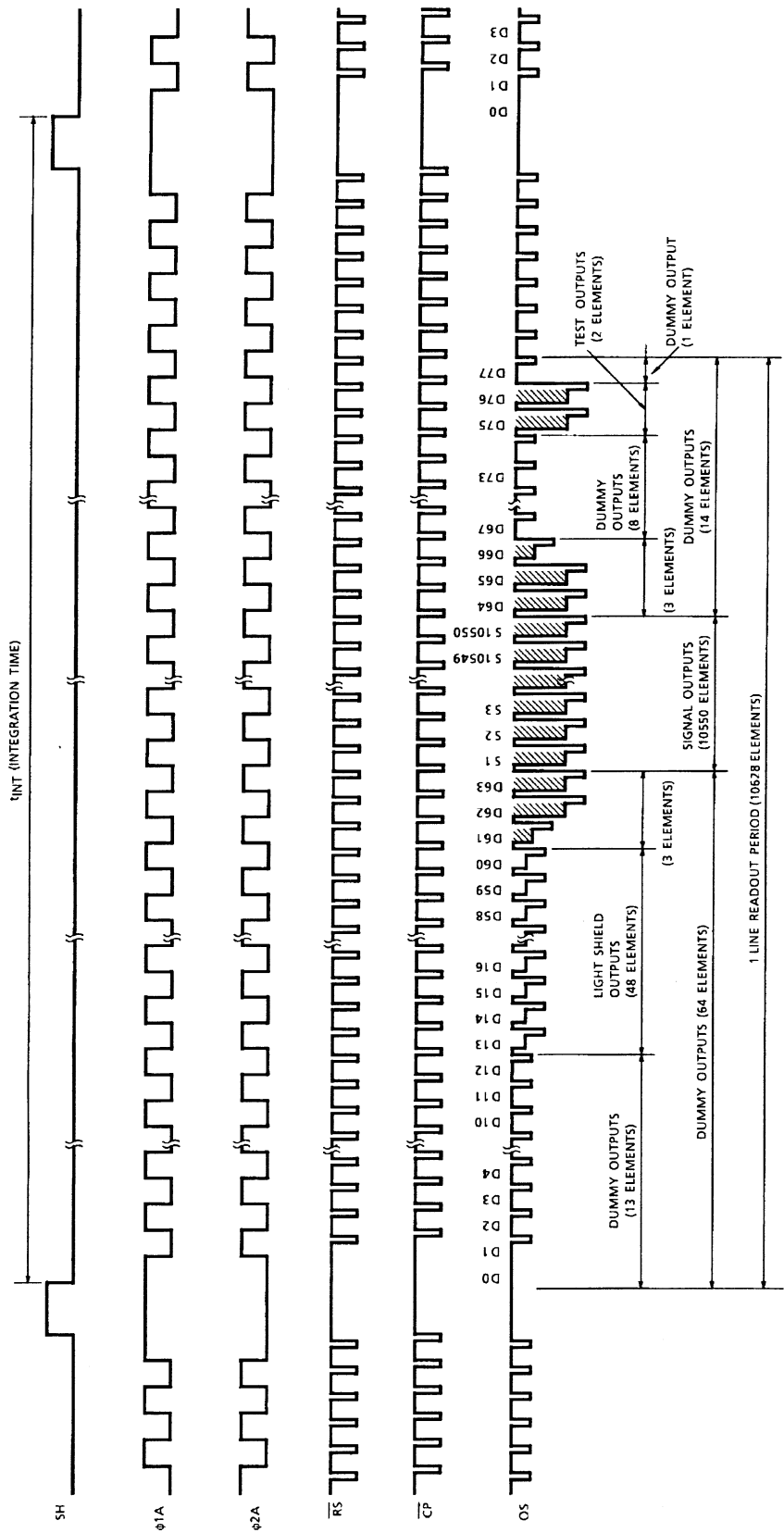
Note 11:  $V_{\phi A}$  "H" means the high level voltage of  $V_{\phi A}$  when SH pulse is high level.

## CLOCK CHARACTERISTICS (Ta = 25°C)

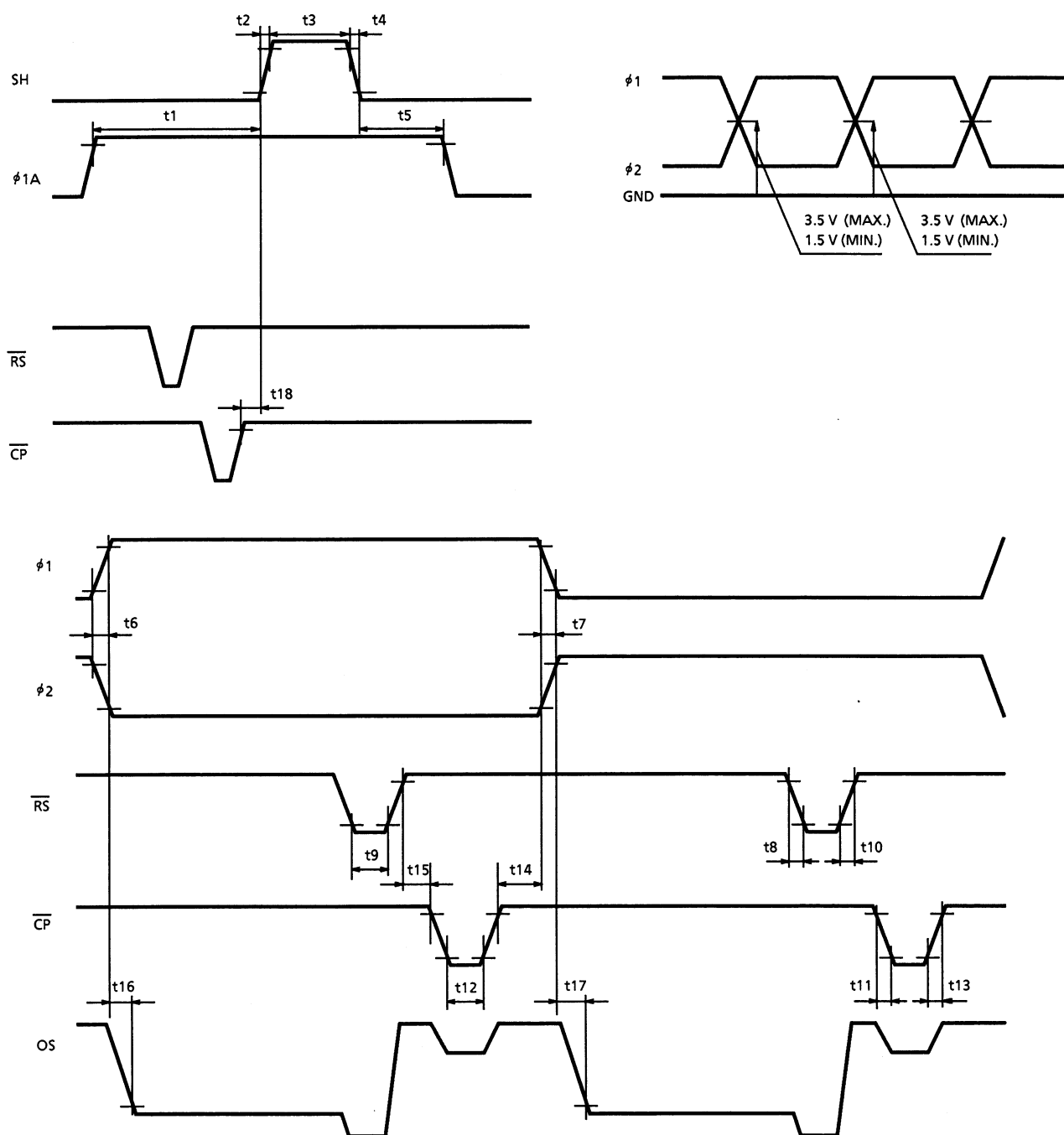
CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT
Clock Pulse Frequency	$f_{\phi A}$	0.15	0.5	2.5	MHz
Reset Pulse Frequency	$\overline{f_{RS}}$	0.3	1.0	5.0	MHz
Clamp Pulse Frequency	$\overline{f_{CP}}$	0.3	1.0	5.0	MHz
Clock Capacitance (Note 12)	$C_{\phi A}$	—	350	450	pF
Shift Gate Capacitance	$C_{SH}$	—	50	100	pF
Reset Gate Capacitance	$\overline{C_{RS}}$	—	10	20	pF
Clamp Gate Capacitance	$\overline{C_{CP}}$	—	10	20	pF

Note 12:  $V_{OD} = 12 \text{ V}$

TIMING CHART



## TIMING REQUIREMENTS



## TIMING REQUIREMENTS (Cont'd)

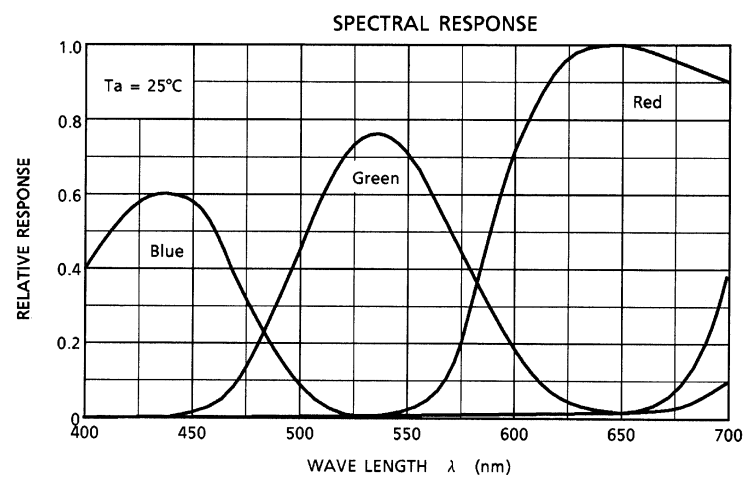
CHARACTERISTIC	SYMBOL	MIN.	TYP. (Note 13)	MAX.	UNIT
Pulse Timing of SH and $\phi_{1A}$	t1	110	1000	—	ns
	t5	200	1000	—	
SH Pulse Rise Time, Fall Time	t2, t4	0	50	—	ns
SH Pulse width	t3	1000	2000	—	ns
$\phi_1$ , $\phi_2$ Pulse Rise Time, Fall Time	t6, t7	0	50	—	ns
$\overline{RS}$ Pulse Rise Time, Fall Time	t8, t10	0	20	—	ns
$\overline{RS}$ Pulse width	t9	45 (Note 15)	100	—	ns
$\overline{CP}$ Pulse Rise Time, Fall Time	t11, t13	0	20	—	ns
$\overline{CP}$ Pulse width	t12	40	100	—	ns
Pulse Timing of $\phi_{1A}$ , $\phi_{2A}$ and $\overline{CP}$	t14	20	40		ns
Pulse Timing of $\overline{RS}$ and $\overline{CP}$	t15	45	100		ns
Video Data Delay Time (Note 14)	t16, t17	—	80	—	ns
Pulse Timing of SH and $\overline{CP}$	t18	0	500	—	ns

Note 13: TYP. is the case of  $f_{\overline{RS}} = 1.0$  MHz.

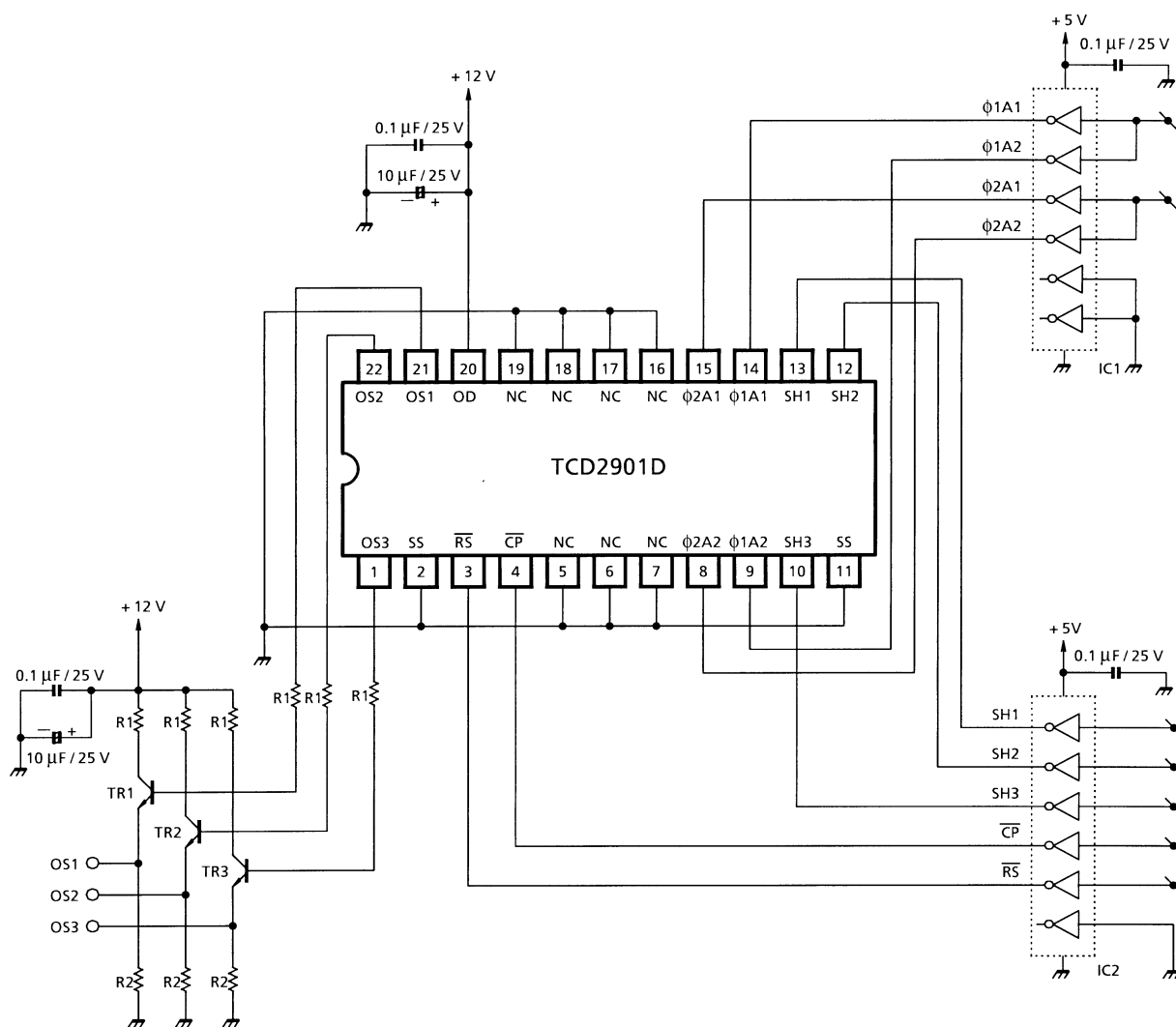
Note 14: Load resistance is 100 k $\Omega$ .

Note 15: In line clamp operation, t9 is 70 ns (MIN.).

TYPICAL SPECTRAL RESPONSE



## TYPICAL DRIVE CIRCUIT



IC1, 2 : TC74AC04AP  
 TR1, 2, 3 : 2SC1815-Y  
 R1 : 150  $\Omega$   
 R2 : 1500  $\Omega$

**CAUTION****1. Window Glass**

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.

Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N<sub>2</sub>.

Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

**2. Electrostatic Breakdown**

Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

**3. Incident Light**

CCD sensor is sensitive to infrared light.

Note that infrared light component degrades resolution and PRNU of CCD sensor.

**4. Lead Frame Forming**

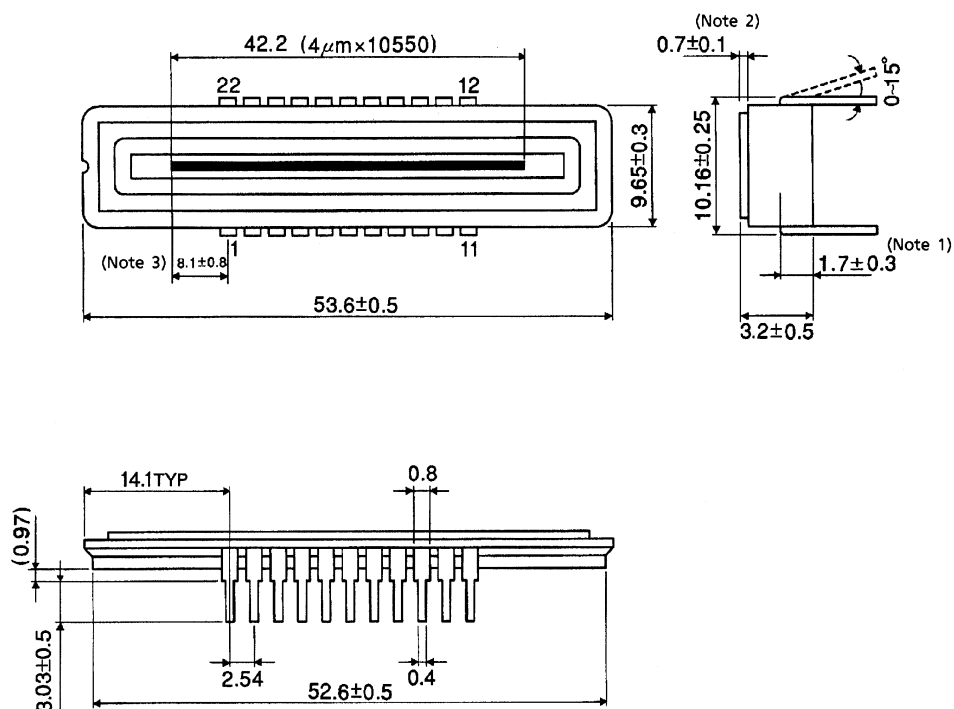
Since this package is not strong against mechanical stress, you should not reform the lead frame.

We recommend to use a IC-inserter when you assemble to PCB.

## PACKAGE DIMENSIONS

WDIP22-G-400-2.54D (D)

Unit : mm



Note 1: TOP OF CHIP TO BOTTOM OF PACKAGE

Note 2: GLASS THICKNESS (n = 1.5)

Note 3: No.1 SENSOR ELEMENT (S1) TO CENTER OF No.1 PIN.

Weight: 5.2g (Typ.)