



rev F

Low Frequency EMI Reduction IC

Features

- FCC approved method of EMI attenuation
- Provides up to 20 dB of EMI suppression
- Generates a low EMI spread spectrum clock of the input frequency
- Optimized for 10 MHz to 35MHz input frequency range
- Internal loop filter minimizes external components and board space
- 4 selectable spread ranges
- SSON control pin for spread spectrum enable and disable options
- Characterizes to work with **EMI-Lator**®, EMC simulation program.
- Low cycle-to-cycle jitter
- Wide operating range (3V to 5V)
- 16 mA output drives
- TTL or CMOS compatible outputs
- Low power CMOS design
- Available in 8 pin SOIC and TSSOP

reduction of EMI of all clock dependent signals. The P2010 allows significant system cost savings by reducing the number of circuit board layers and shielding that are traditionally required to pass EMI regulations.

The P2010 uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all-digital method.

The P2010 modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock and, more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called “spread spectrum clock generation”.

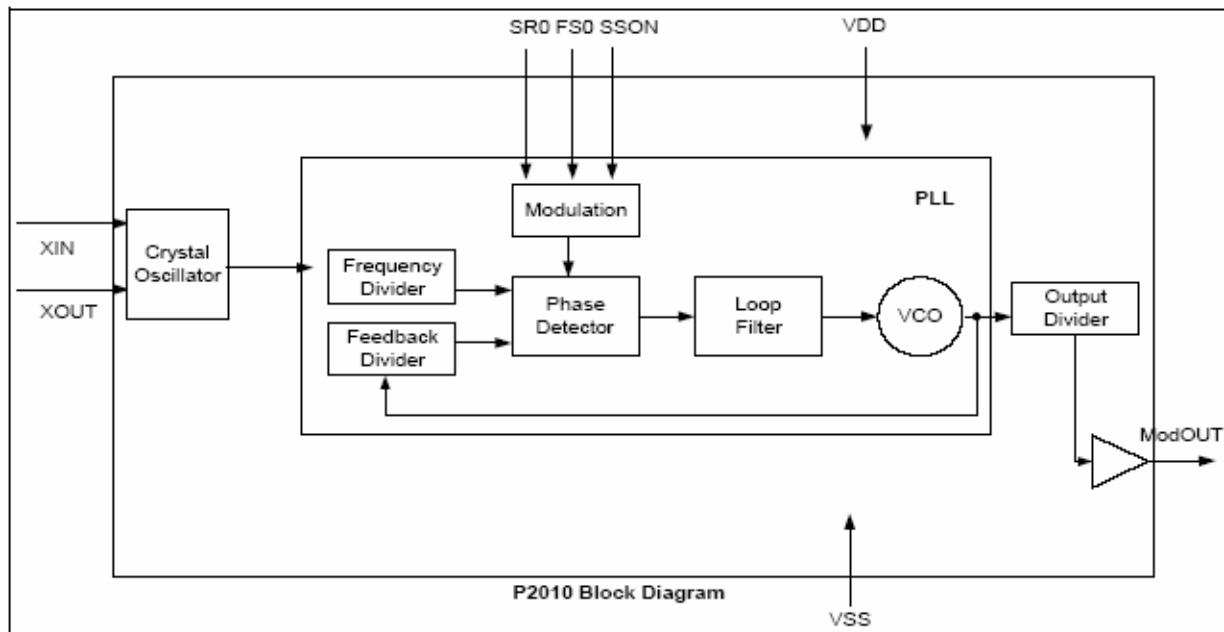
Product Description

The P2010 is a selectable spread spectrum frequency modulator designed specifically for PC peripheral and embedded controller markets. The P2010 reduces electromagnetic interference (EMI) at the clock source which provides system wide

Applications

The P2010 is targeted towards the embedded controller market and PC peripheral markets including scanners, facsimile, MFP’s, printers, PDA, IA, and GPS devices.

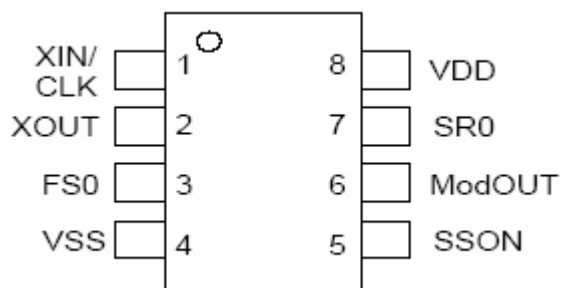
Block Diagram





rev F

Pin Configuration



Pin Description

Pin#	Pin Name	Type	Description
1	XIN/CLK	I	Connect to crystal or externally generated clock signal.
2	XOUT	I	Connect to crystal. No connect if externally generated clock signal is used.
3	FS0	I	Digital logic input used to select Input Frequency Range (see Table 1). This pin has an internal pull-up resistor.
4	VSS	P	Ground Connection. Connect to system ground.
5	SSON	I	Digital logic input used to enable Spread Spectrum function (Active Low). Spread Spectrum function enable when low. This pin has an internal pull-low resistor.
6	ModOUT	O	Spread Spectrum Clock Output.
7	SR0	I	Digital logic input used to select Spreading Range (see Table 1). This pin has an internal pull-up resistor.
8	VDD	P	Connect to +3.3V or +5.0V

Table 1 - Spread Range Selection

FS0	SR0	Spreading Range	Input Frequency	Modulation rate
1	0	+/- 1.50%	10 MHz to 20 MHz	$(F_{in}/10) \times 20.83 \text{ KHz}$
1	1	+/- 2.50%	10 MHz to 20 MHz	$(F_{in}/10) \times 20.83 \text{ KHz}$
0	0	+/- 1.25%	20 MHz to 35 MHz	$(F_{in}/10) \times 20.83 \text{ KHz}$
0	1	+/- 2.00%	20 MHz to 35 MHz	$(F_{in}/10) \times 20.83 \text{ KHz}$



rev F

Spread Spectrum Selection

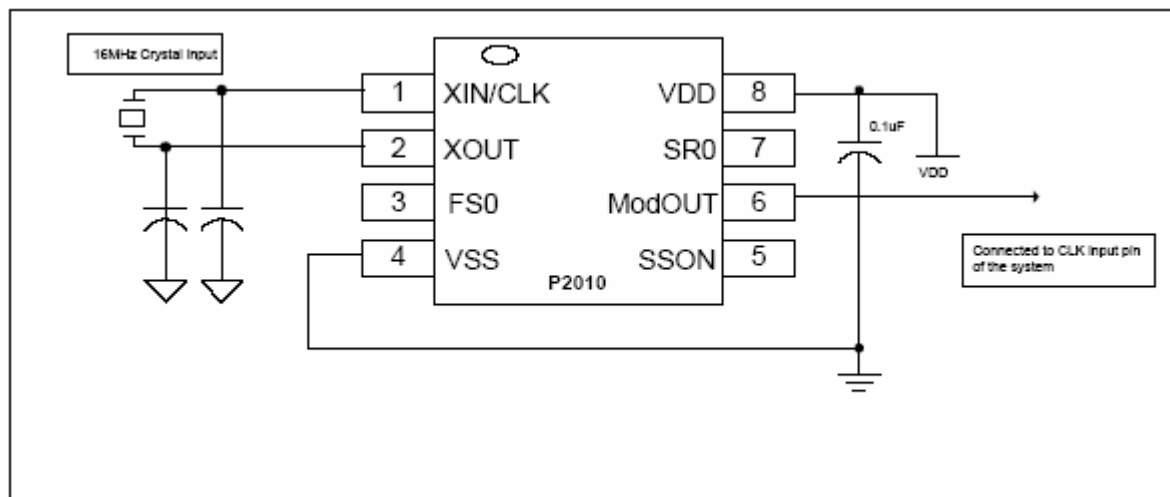
Table 1 illustrates the possible spread spectrum options. The optimal setting should minimize system EMI to the fullest without affecting system performance. The spreading is described as a percentage deviation of the center frequency (Note: the center frequency is the frequency of the external reference input on CLKIN, Pin 1).

Example of a typical printer or scanner application that operates on a clock frequency of 16 MHz:

A spreading selection of FS0=1 and SR0=1 provides a percentage deviation of $\pm 2.50\%$ * (see Table 1) of F_{cen} . This results in the frequency on ModOUT being swept from 16.40 MHz to 15.60 MHz at a modulation rate of 33.33 KHz (see Table 1). This particular example (see Figure below) given here is a common EMI reduction method for scanner, printer, or embedded applications and has already been adopted by most of the leading manufacturers.

NOTE: Spreading range selection varies from different system manufacturers and their designs.

P2010 Application Schematic for Flat-Bed Scanner

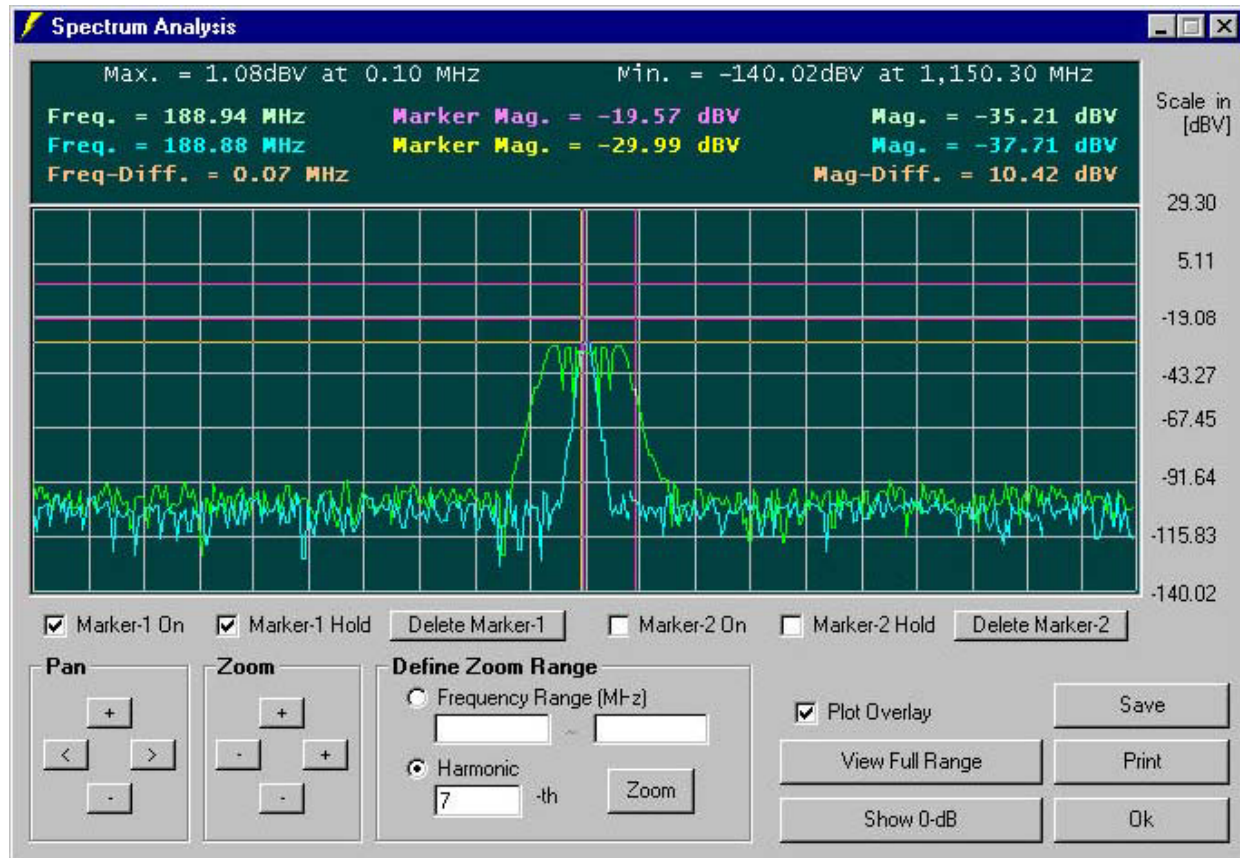




rev F

EMC Software Simulation

By using Alliance Semiconductor's proprietary EMC simulation software – EMI-lator®, radiated system level EMI analysis can be made easier to allow a quantitative assessment on Alliance's EMI reduction products. The simulation engine of this EMC software has already been characterized to correlate with the electrical characteristics of Alliance EMI reduction IC's. The figure below is an example of the simulation result. Please visit our web site at www.alsc.com for information on how to obtain a free copy and demonstration of EMI-lator®.

Simulation Result from EMI-lator®



rev F

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	-0.5 to + 7.0	V
T_{STG}	Storage temperature	-65 to +125	°C
T_A	Operating temperature	0 to +70	°C

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	GND –	-	0.8	V
V_{IH}	Input High Voltage	2.0	-	$V_{DD} + 0.3$	V
I_{IL}	Input Low Current (pull-up resistor on inputs SR0, 1)	-	-	-35	μA
I_{IH}	Input High Current (pull-down resistor on input SSON)	-	-	35	μA
V_{OL}	Output Low Voltage ($V_{DD}=3.3V$, $I_{OL} = 20\text{ mA}$)	-	-	0.4	V
V_{OH}	Output High Voltage ($V_{DD}=3.3V$, $I_{OH} = 20\text{ mA}$)	2.5	-	-	V
I_{DD}	Static Supply Current	-	0.6	-	mA
I_{CC}	Dynamic Supply Current (3.3V and 15pF loading)	4	6	8	mA
V_{DD}	Operating Voltage	2.7	3.3	5.5	V
t_{ON}	Power Up Time (First locked clock cycle after power up)		0.18		ms
Z_{OUT}	Clock Output Impedance		50		Ω

AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input Frequency when	10	20	30	MHz
t_{LH}^*	Output rise time (Measured at 0.8V to 2.0V)	0.7	0.9	1.1	ns
t_{HL}^*	Output fall time (Measured at 0.8V to 2.0V)	0.6	0.8	1.0	ns
t_{JC}	Jitter (cycle to cycle)	-	-	360	ps
t_D	Output duty cycle	45	50	55	%

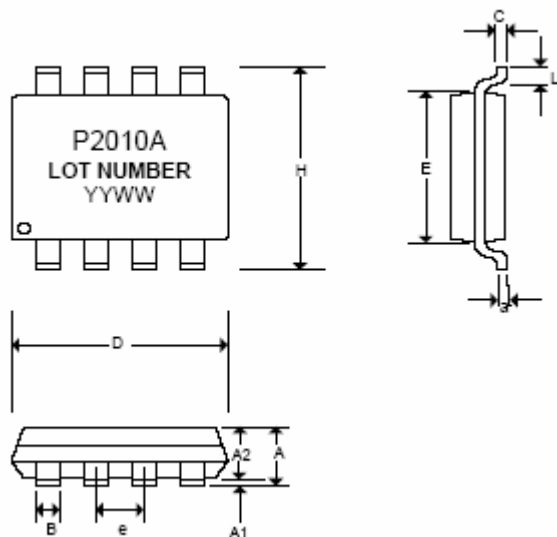
* t_{LH} and t_{HL} are measured into a capacitive load of 15pF



rev F

Package Information

Mechanical Package Outline 8-Pin SOIC



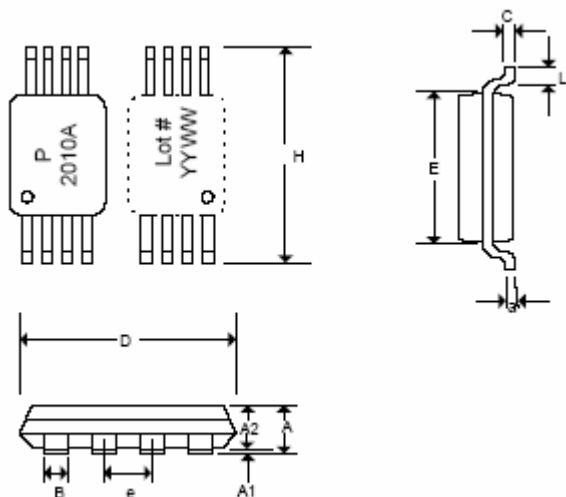
Symbol	Dimensions in inches			Dimensions in millimeters		
	Min	Nor	Max	Min	Nor	Max
A	0.057	0.064	0.071	1.45	1.63	1.80
A1	0.004	0.007	0.010	0.10	0.18	0.25
A2	0.053	0.061	0.069	1.35	1.55	1.75
B	0.012	0.016	0.020	0.31	0.41	0.51
C	0.004	0.006	0.01	0.10	0.15	0.25
D	0.186	0.194	0.202	4.72	4.92	5.12
E	0.148	0.156	0.164	3.75	3.95	4.15
e	0.050 BSC			1.27 BSC		
H	0.224	0.236	0.248	5.70	6.00	6.30
L	0.012	0.020	0.028	0.30	0.50	0.70
a	0°	5°	8°	0°	5°	8°

Note: Controlling dimensions are millimeters



rev F

Mechanical Package Outline 8-Pin TSSOP



Symbol	Dimensions in inches			Dimensions in millimeters		
	Min	Nor	Max	Min	Nor	Max
A			0.047			1.10
A1	0.002		0.006	0.05		0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
B	0.007		0.012	0.19		0.30
C	0.004		0.008	0.09		0.20
D	0.114	0.118	0.122	2.90	3.00	3.10
E	0.169	0.173	0.177	4.30	4.40	4.50
e	0.026 BSC			0.65 BSC		
H	0.244	0.252	0.260	6.20	6.40	6.60
L	0.018	0.024	0.030	0.45	0.60	0.75
a	0°	5°	8°	0°	5°	8°

Note: Controlling dimensions are millimeters

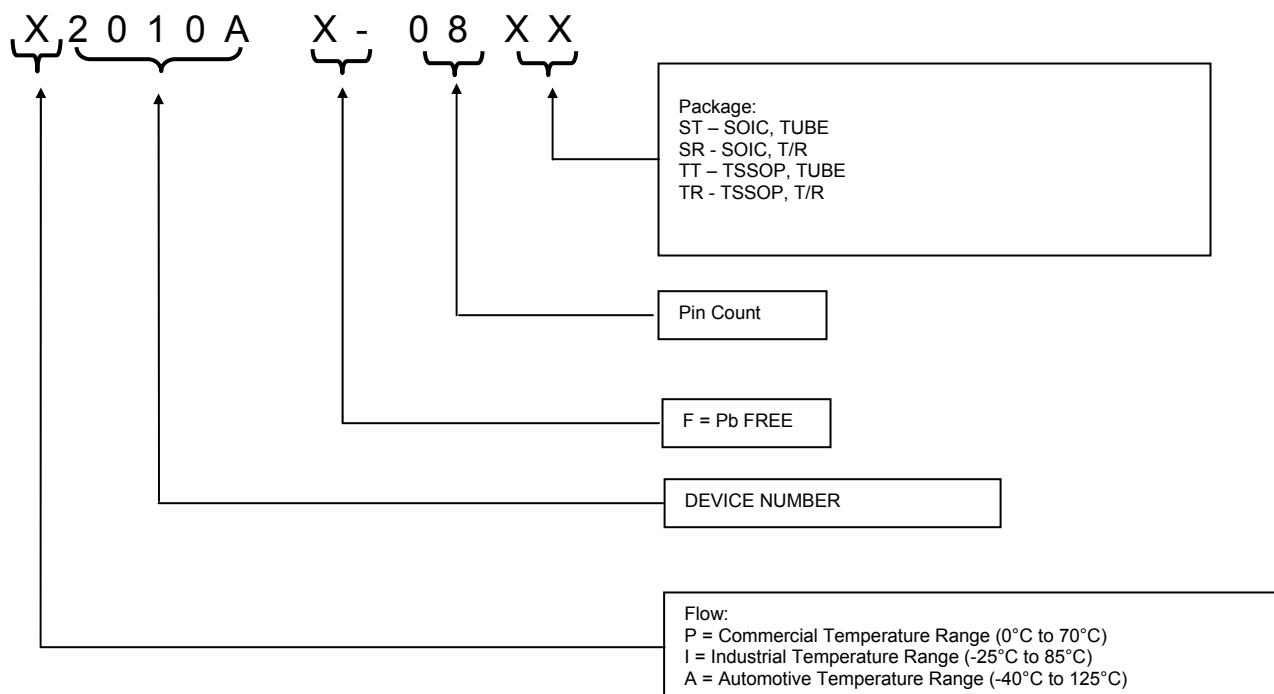


rev F

Ordering Codes

Part Number	Marking	Package Type	Qty per reel	Temperature (°C)
P2010A-08ST	P2010A	8 PIN SOIC, TUBE		0 TO 70
P2010A-08SR	P2010A	8 PIN SOIC, TAPE & REEL	2,500	0 TO 70
P2010A-08TT	P2010A	8 PIN TSSOP, TUBE		0 TO 70
P2010A-08TR	P2010A	8 PIN TSSOP, TAPE & REEL	2,500	0 TO 70

Device Ordering Information



Licensed under US patent Nos 5,488,627 and 5,631,920.
 Preliminary datasheet. Specification subject to change without notice.



rev F



Alliance Semiconductor Corporation
2595, Augustine Drive,
Santa Clara, CA 95054
Tel# 408-855-4900
Fax: 408-855-4999
www.alsc.com

Copyright © Alliance Semiconductor
All Rights Reserved
Part Number: P2010A
Document Version: F

© Copyright 2003 Alliance Semiconductor Corporation. All rights reserved. Our three-point logo, our name and Intelliwatt are trademarks or registered trademarks of Alliance. All other brand and product names may be the trademarks of their respective companies. Alliance reserves the right to make changes to this document and its products at any time without notice. Alliance assumes no responsibility for any errors that may appear in this document. The data contained herein represents Alliance's best data and/or estimates at the time of issuance. Alliance reserves the right to change or correct this data at any time, without notice. If the product described herein is under development, significant changes to these specifications are possible. The information in this product data sheet is intended to be general descriptive information for potential customers and users, and is not intended to operate as, or provide, any guarantee or warrantee to any user or customer. Alliance does not assume any responsibility or liability arising out of the application or use of any product described herein, and disclaims any express or implied warranties related to the sale and/or use of Alliance products including liability or warranties related to fitness for a particular purpose, merchantability, or infringement of any intellectual property rights, except as express agreed to in Alliance's Terms and Conditions of Sale (which are available from Alliance). All sales of Alliance products are made exclusively according to Alliance's Terms and Conditions of Sale. The purchase of products from Alliance does not convey a license under any patent rights, copyrights; mask works rights, trademarks, or any other intellectual property rights of Alliance or third parties. Alliance does not authorize its products for use as critical components in life-supporting systems where a malfunction or failure may reasonably be expected to result in significant injury to the user, and the inclusion of Alliance products in such life-supporting systems implies that the manufacturer assumes all risk of such use and agrees to indemnify Alliance against all claims arising from such use.