

MOSFET – Power, Dual N-Channel, for 1-2 Cells Lithium-ion Battery Protection

24 V, 45 mΩ, 6 A

EFC4612R-S

This Power MOSFET features a low on-state resistance. This device is suitable for applications such as power switches of portable machines. Best suited for 1–2 cells lithium-ion battery applications.

Features

- 2.5 V Drive
- Common-Drain Type
- ESD Diode-Protected Gate
- Pb-Free, Halide Free and RoHS Compliant

Applications

- 1–2 Cells Lithium-ion Battery Charging and Discharging Switch

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS at $T_A = 25^\circ\text{C}$

Parameter	Symbol	Value	Unit
Source to Source Voltage	V_{SSS}	24	V
Gate to Source Voltage	V_{GSS}	± 12	V
Source Current (DC)	I_S	6	A
Source Current (Pulse) $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$	I_{SP}	60	A
Total Dissipation (Note 2)	P_T	1.6	W
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

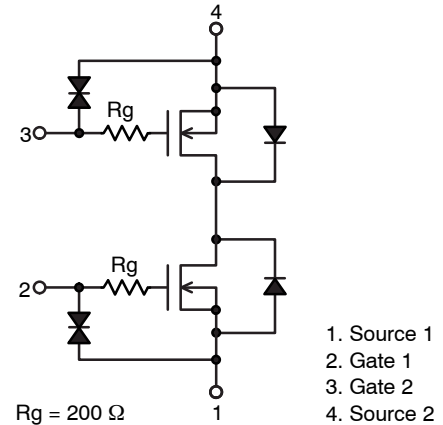
THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction to Ambient (Note 1)	$R_{\theta JA}$	78.1	$^\circ\text{C/W}$

1. Surface mounted on ceramic substrate (5000 mm² × 0.8 mm).

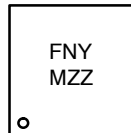
V_{SSS}	$R_{SS(on)}$ Max	I_S Max
24 V	45 mΩ @ 4.5 V	6 A
	48 mΩ @ 4.0 V	
	50 mΩ @ 3.7 V	
	57 mΩ @ 3.1 V	
	72 mΩ @ 2.5 V	

ELECTRICAL CONNECTION N-Channel



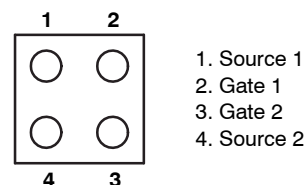
WLCSP4, 1.3 × 1.3 /
EFCP1313-4CC-037
CASE 567DP

MARKING DIAGRAM



FN = Specific Device Code
Y = Year
M = Month
ZZ = Assembly Lot Number

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

EFC4612R-S

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Source to Source Breakdown Voltage	$V_{(BR)SSS}$	$I_S = 1\text{ mA}$, $V_{GS} = 0\text{ V}$ (Figure 1)	24	–	–	V
Zero-Gate Voltage Source Current	I_{SSS}	$V_{SS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$ (Figure 1)	–	–	1	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 8\text{ V}$, $V_{SS} = 0\text{ V}$ (Figure 2)	–	–	± 10	μA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{SS} = 10\text{ V}$, $I_S = 1\text{ mA}$ (Figure 3)	0.5	–	1.3	V
Forward Transconductance	g_{FS}	$V_{SS} = 10\text{ V}$, $I_S = 3\text{ A}$ (Figure 4)	–	3.1	–	S
Static Source to Source On-State Resistance	$R_{SS(on)1}$	$V_{GS} = 4.5\text{ V}$, $I_S = 3\text{ A}$ (Figure 5)	24	39	45	$\text{m}\Omega$
	$R_{SS(on)2}$	$V_{GS} = 4.0\text{ V}$, $I_S = 3\text{ A}$ (Figure 5)	25	41	48	$\text{m}\Omega$
	$R_{SS(on)3}$	$V_{GS} = 3.7\text{ V}$, $I_S = 3\text{ A}$ (Figure 5)	27.5	43	50	$\text{m}\Omega$
	$R_{SS(on)4}$	$V_{GS} = 3.1\text{ V}$, $I_S = 3\text{ A}$ (Figure 5)	31.5	48	57	$\text{m}\Omega$
	$R_{SS(on)5}$	$V_{GS} = 2.5\text{ V}$, $I_S = 3\text{ A}$ (Figure 5)	33.5	58	72	$\text{m}\Omega$
Turn-ON Delay Time	$t_d(on)$	$V_{SS} = 10\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_S = 3\text{ A}$ (Figure 6)	–	20	–	ns
Rise Time	t_r		–	230	–	ns
Turn-OFF Delay Time	$t_d(off)$		–	130	–	ns
Fall Time	t_f		–	210	–	ns
Total Gate Charge	Q_g	$V_{SS} = 10\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_S = 6\text{ A}$ (Figure 7)	–	7	–	nC
Forward Source to Source Voltage	$V_{F(S-S)}$	$I_S = 3\text{ A}$, $V_{GS} = 0\text{ V}$ (Figure 8)	–	0.8	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Test Circuit are Example of Measuring FET1 Side

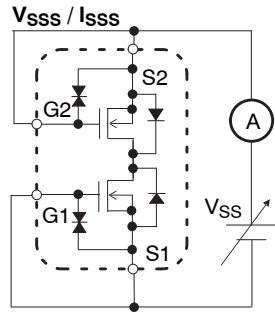


Figure 1. Test Circuit 1

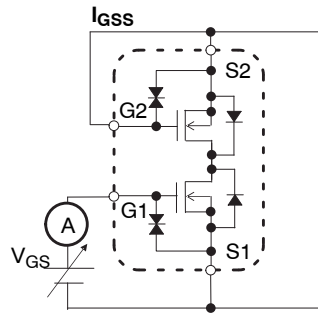


Figure 2. Test Circuit 2

When FET1 is measured, Gate and Source of FET2 are short-circuited.

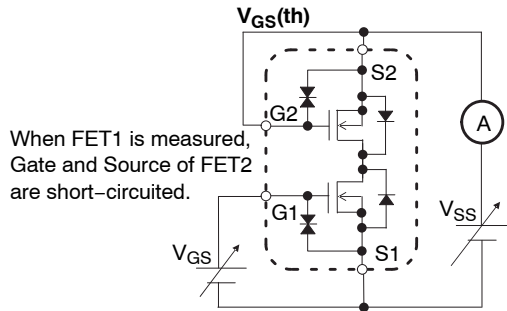


Figure 3. Test Circuit 3

When FET1 is measured, Gate and Source of FET2 are short-circuited.

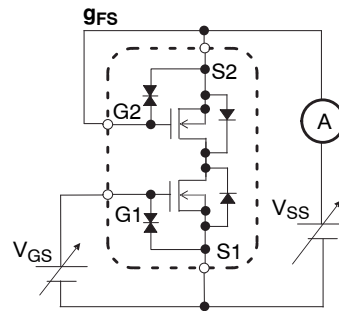


Figure 4. Test Circuit 4

When FET1 is measured, Gate and Source of FET2 are short-circuited.

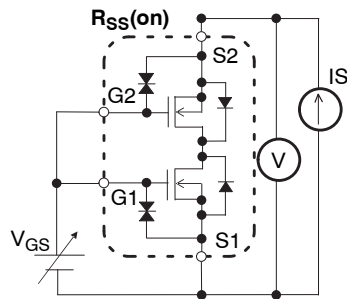


Figure 5. Test Circuit 5

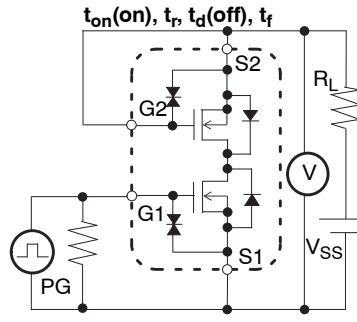


Figure 6. Test Circuit 6

When FET1 is measured, Gate and Source of FET2 are short-circuited.

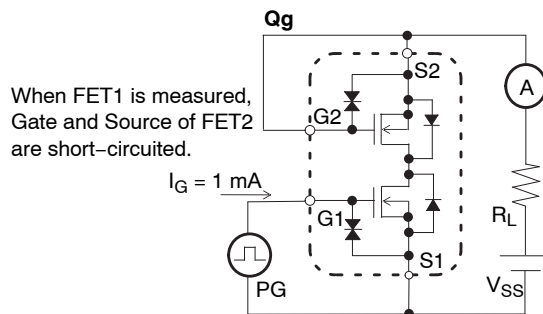


Figure 7. Test Circuit 7

When FET1 is measured, Gate and Source of FET2 are short-circuited.

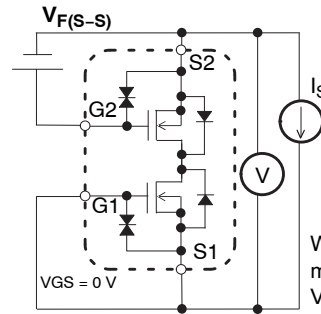


Figure 8. Test Circuit 8

When FET1 is measured, +4.5 V is added to VGS of FET2.

NOTE: When FET2 is measured, the position of FET1 and FET2 is switched.

TYPICAL CHARACTERISTICS

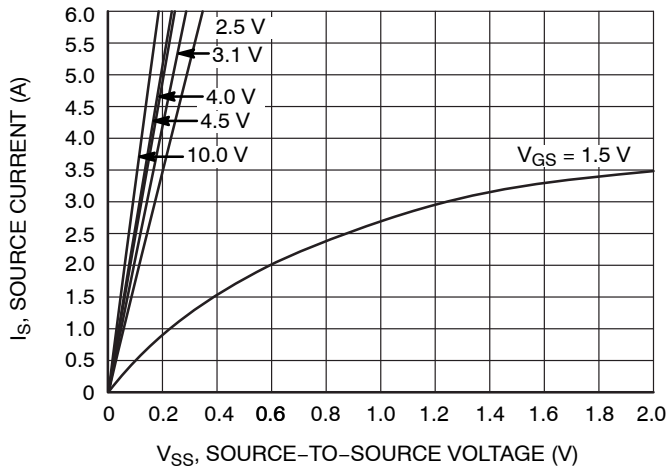


Figure 9. I_S - V_{SS}

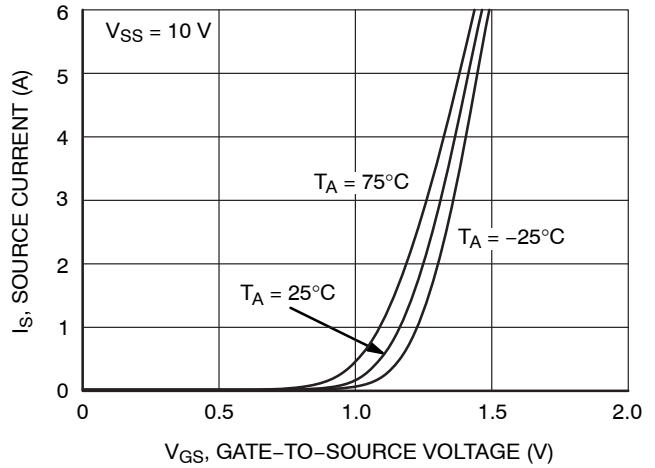


Figure 10. I_S - V_{GS}

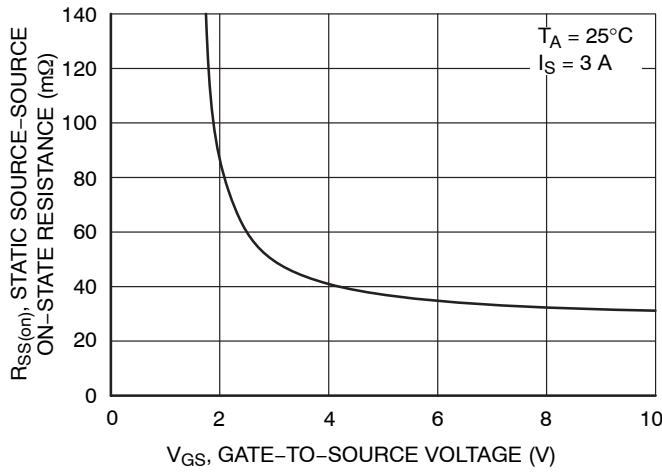


Figure 11. $R_{SS(on)}$ - V_{GS}

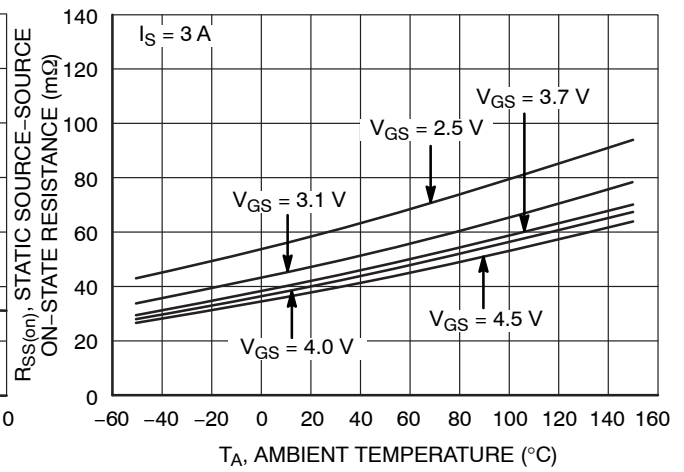


Figure 12. $R_{SS(on)}$ - T_A

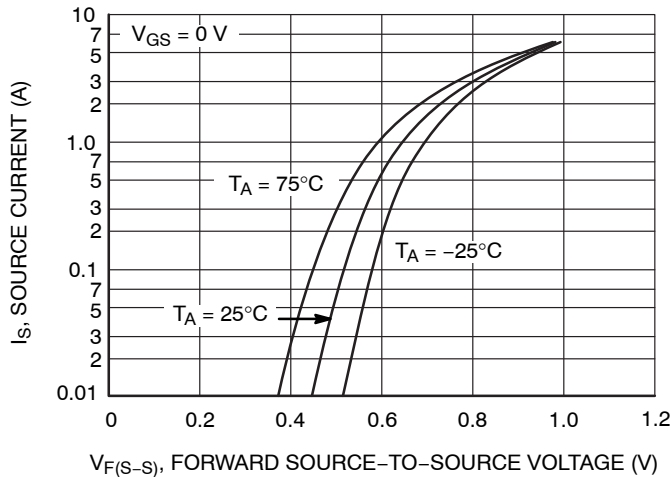


Figure 13. I_S - $V_{F(S-S)}$

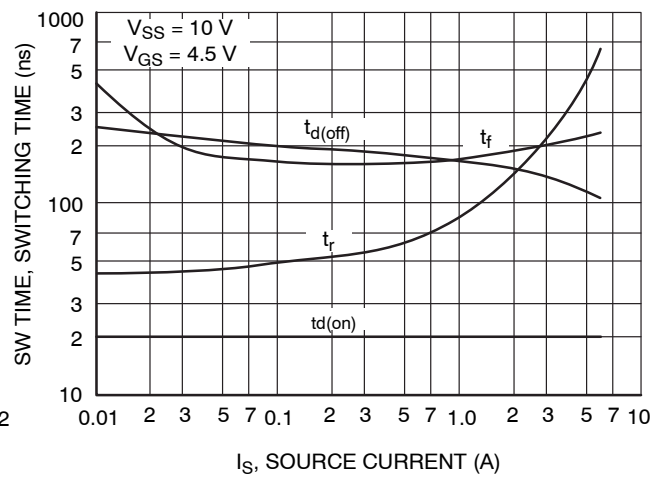


Figure 14. SW Time - I_S

EFC4612R-S

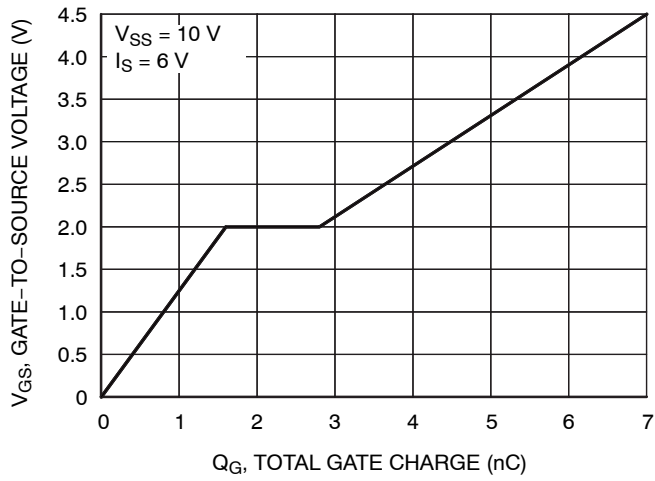


Figure 15. $V_{GS} - Q_g$

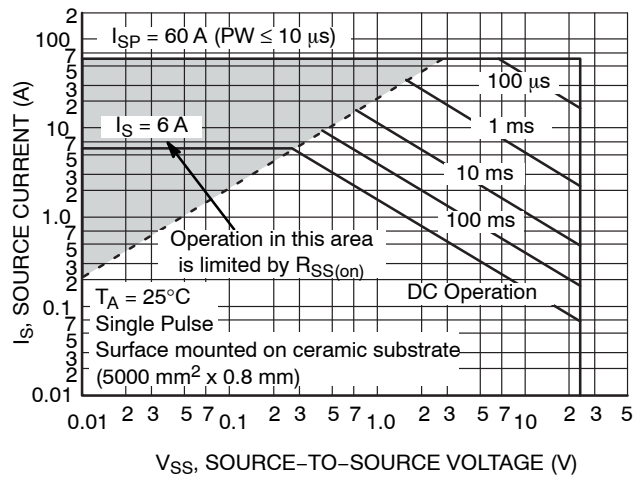


Figure 16. SOA

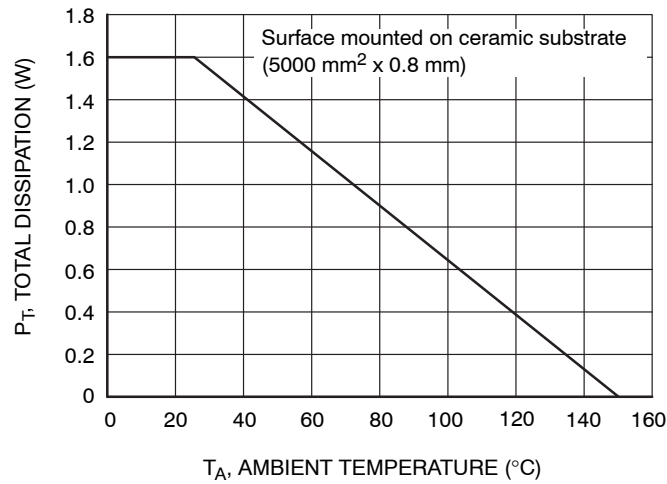


Figure 17. $P_T - T_A$

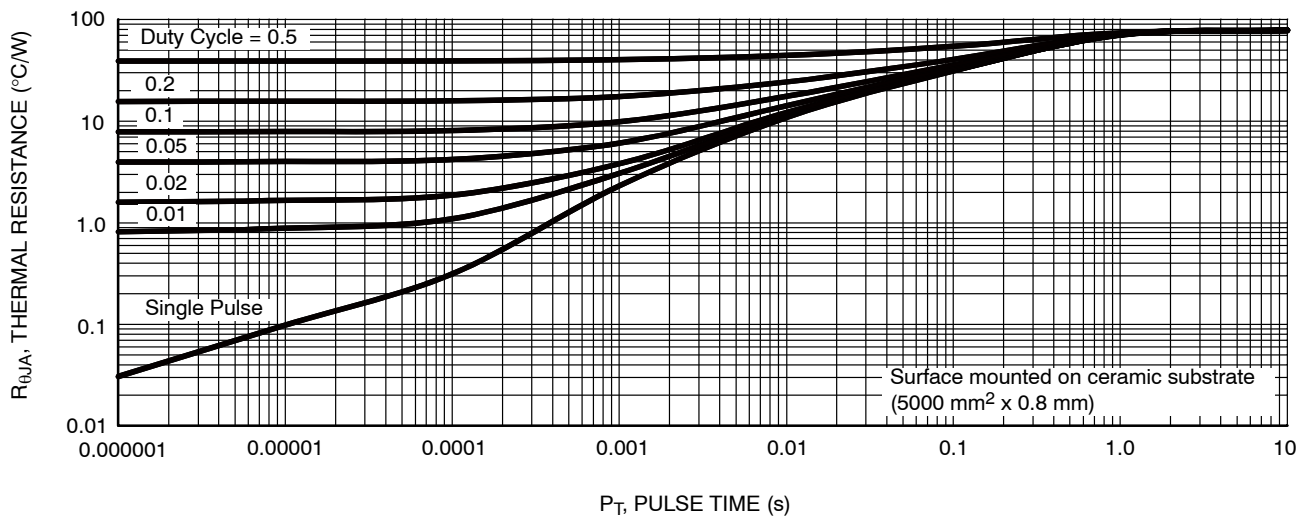


Figure 18. $R_{\theta JA} - \text{Pulse Time}$

EFC4612R-S

ORDERING INFORMATION

Device	Marking	Package	Shipping [†] (Qty / Packing)
EFC4612R-S-TR	FN	WLCSP4, 1.3 × 1.3 / EFCP1313-4CC-037 (Pb-Free and Halide Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

PACKAGE DIMENSION

(Unit: mm)

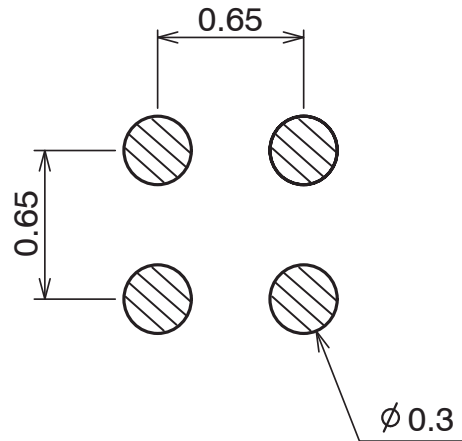


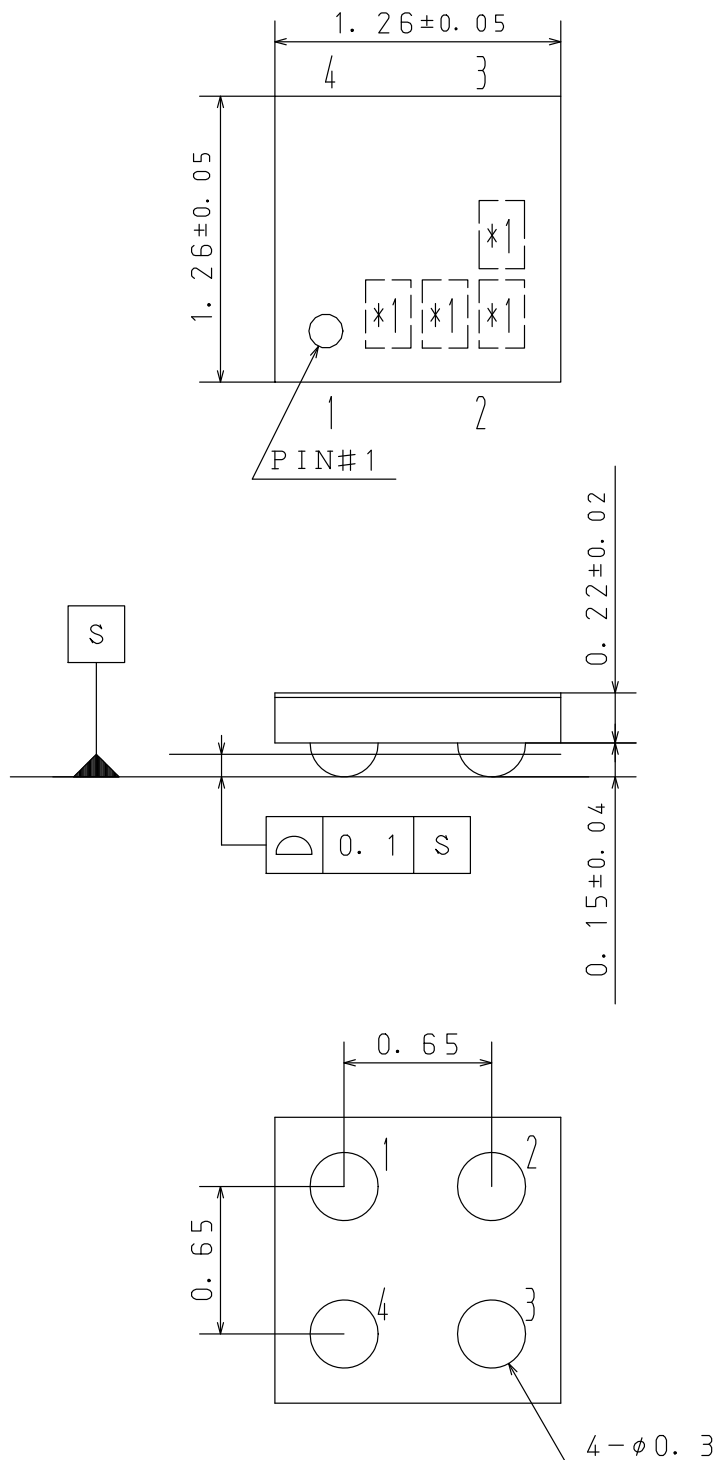
Figure 19. Recommended Soldering Footprint

WLCSP4, 1.3x1.3 / EFCP1313-4CC-037

CASE 567DP

ISSUE 0

DATE 29 FEB 2012



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