19-1601; Rev 2; 11/05

EVALUATION KIT AVAILABLE

622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

General Description

The MAX3665 low-power transimpedance preamplifier for 622Mbps SDH/SONET applications consumes only 70mW at V_{CC} = 3.3V. Operating from a single +3.3V or +5.0V supply, it converts a small photodiode current to a measurable differential voltage. A DC cancellation circuit provides a true differential output swing over a wide range of input current levels, thus reducing pulse-width distortion. The differential outputs are back-terminated with 50Ω per side.

The overall transimpedance gain is nominally 8kΩ. For input signal levels beyond approximately 50µAp-p, the amplifier will limit the output swing to 250mV. The MAX3665's low 55nA input noise provides a typical sensitivity of -33.2dBm in 1300nm, 622Mbps receivers.

The MAX3665 is designed to be used in conjunction with the MAX3676 clock recovery and data retiming IC with limiting amplifier. Together they form a complete 3.3V or 5.0V 622Mbps SDH/SONET receiver.

In die form, the MAX3665 is designed to fit on a header with a PIN diode. It includes a filter connection that provides positive bias for the photodiode through a 1.5kΩ resistor to V_{CC}. The device is available in an 8-pin µMAX® package.

Applications

SDH/SONET Receivers

PIN Photodiode Preamplifiers and Receivers

Regenerators for SDH/SONET

Features

- +3.3V or +5.0V Single-Supply Operation
- 55nA$_{RMS}$ Input-Referred Noise
- 70mW Power Consumption at V_{CC} = 3.3V
- 8kΩ Gain
- 450µA Peak Input Current
- 260ps (max) Deterministic Jitter
- Differential Output Drives 100Ω Load
- 470MHz Bandwidth

Ordering Information

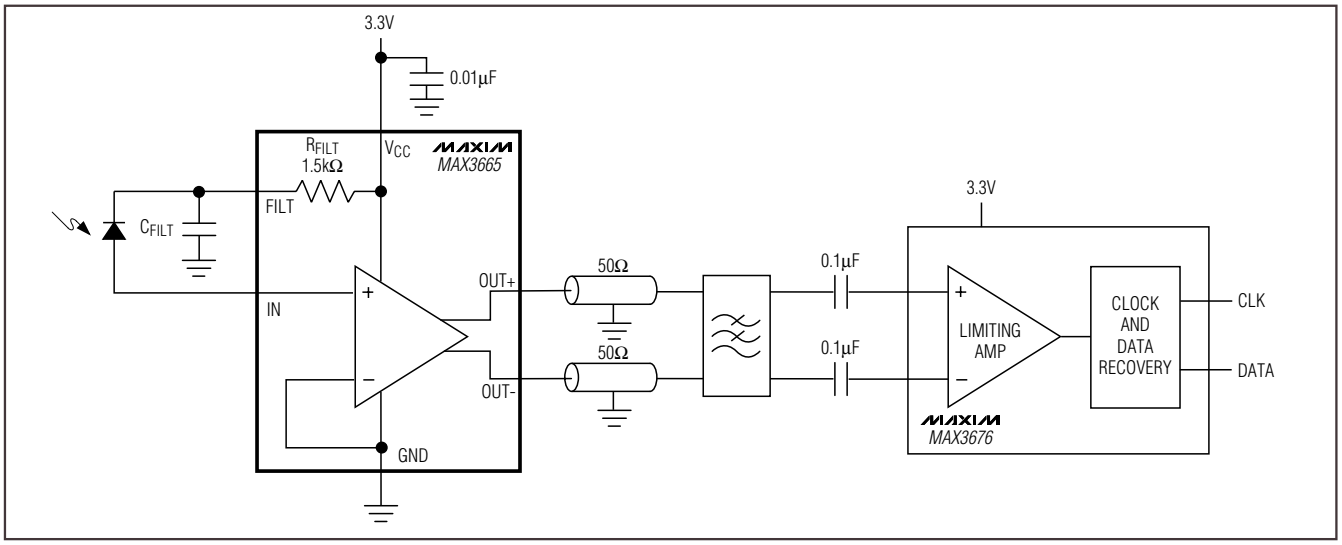
PART	TEMP RANGE	PIN-PACKAGE
MAX3665EUA	-40°C to +85°C	8 µMAX
MAX3665E/D	(see Note)	Dice

Note: *Dice are designed to operate over a -40°C to +140°C junction temperature (T_j) range, but are tested and guaranteed at T_A = +25°C.*

Pin Configuration appears at end of data sheet.

µMAX is a registered trademark of Maxim Integrated Products, Inc.

Typical Application Circuit



622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

ABSOLUTE MAXIMUM RATINGS

V_{CC} .....-0.5V to +6.5V
Continuous Current at IN .....±5mA
Voltage at OUT+, OUT- .....(V_{CC} - 1.5V) to (V_{CC} + 0.5V)
Voltage at FILT .....-0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +85°C)
8-Pin µMAX (derate 4.5mW/°C above +85°C) 295mW
Operating Junction Temperature (die) .....-55°C to +150°C
Processing Temperature (die) .....+400°C
Storage Temperature Range .....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.3V ±10% or +5.0V ±10%, 100Ω load between OUT+ and OUT-, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Bias Voltage	V_{IN}	I_{IN} = 0 to 300µA		0.8	0.95	V
Gain Nonlinearity		I_{IN} = 0 to 10µA$_{P-P}$			±5	%
Supply Current	I_{CC}	I_{IN} = 0		21	30	mA
Small-Signal Transimpedance	z_{21}	Differential output	7	8		kΩ
Output Common-Mode Voltage				V_{CC} - 0.15		V
Differential Output Offset	ΔV_{OUT}	I_{IN} = 300µA		±5		mV
Output Impedance (per side)	Z_{OUT}		48	50	52	Ω
Maximum Output Voltage	$V_{OUT(MAX)}$	I_{IN} = 450µA$_{P-P}$		260	450	mV$_{P-P}$
Filter Resistor	R_{FILT}			1.5		kΩ

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.3V ±10% or +5.0V ±10%, 100Ω load between OUT+ and OUT-, source capacitance = 0.5pF, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Notes 1 and 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal Bandwidth	BW_{-3dB}	Relative to gain at 10MHz	404	470		MHz
Low-Frequency Cutoff		-3dB with I_{IN} = 5µA		20	40	kHz
Deterministic Jitter	J_D	2^{13} - 1 PRBS with 100 CIDs		100	260	ps
RMS Noise Referred to Input	i_n			55	72	nA
Power-Supply Rejection Ratio	PSRR	f < 1MHz, differential referred to output, ΔV_{CC} = 30mV$_{P-P}$ (Note 3)	36	47		dB

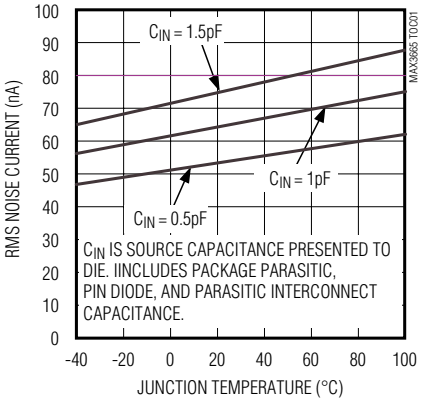
Note 1: AC characteristics are guaranteed by design.
Note 2: Measured with a 3-pole filter at the output. C_{IN} = 0.5pF, I_{IN} = 0, C_{FILT} = 1000pF.
Note 3: PSRR = -20log (ΔV_{OUT} / ΔV_{CC}).

622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

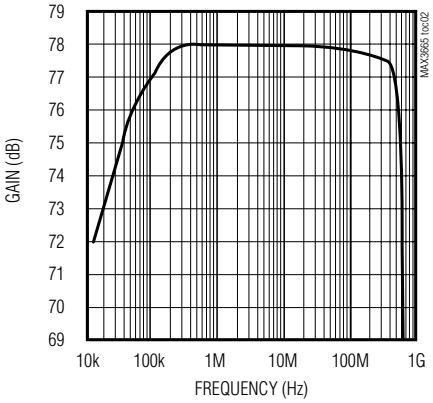
Typical Operating Characteristics

(V_{CC} = +3.3V, includes off-chip filter, see Figure 3b, T_A = +25°C, unless otherwise noted.)

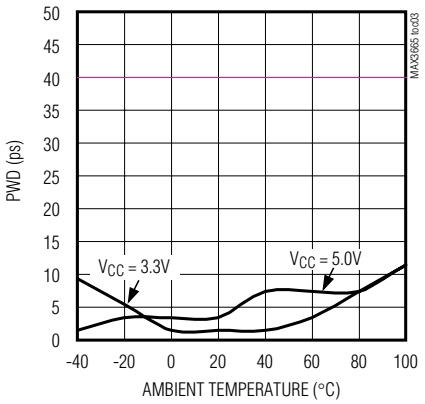
INPUT-REFERRED NOISE vs. TEMPERATURE



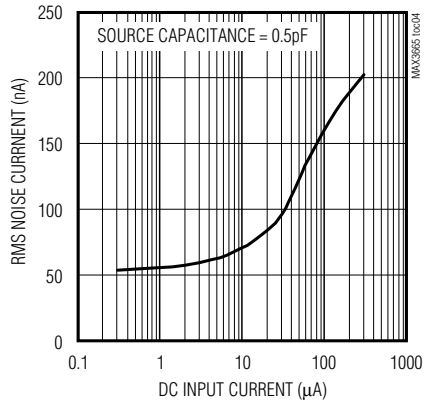
SMALL-SIGNAL GAIN vs. FREQUENCY



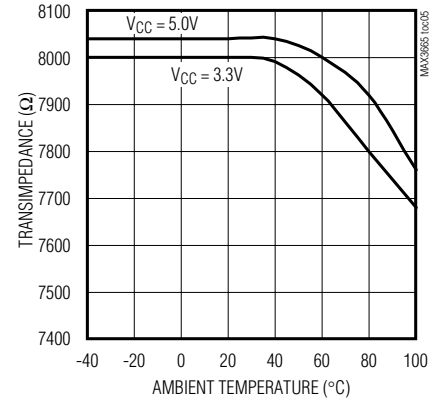
PULSE-WIDTH DISTORTION vs. TEMPERATURE (INPUT = 100µAP-P)



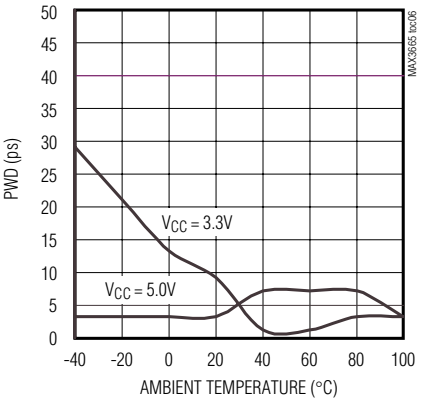
INPUT-REFERRED NOISE vs. DC INPUT CURRENT



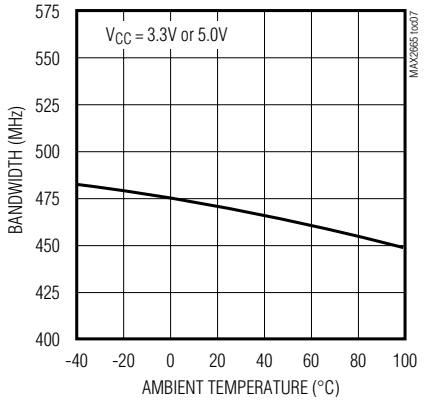
SMALL-SIGNAL TRANSIMPEDANCE vs. TEMPERATURE



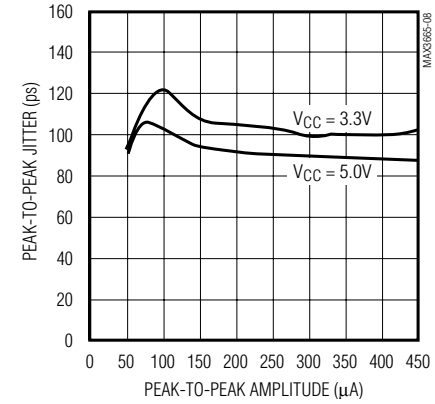
PULSE-WIDTH DISTORTION vs. TEMPERATURE (INPUT = 450µAP-P)



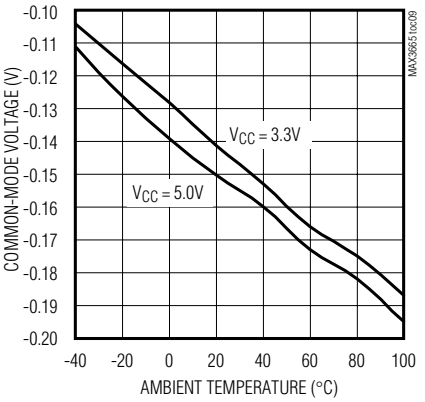
BANDWIDTH vs. TEMPERATURE



DATA-DEPENDENT JITTER vs. INPUT SIGNAL AMPLITUDE



OUTPUT COMMON-MODE VOLTAGE (REFERENCED TO VCC) vs. TEMPERATURE

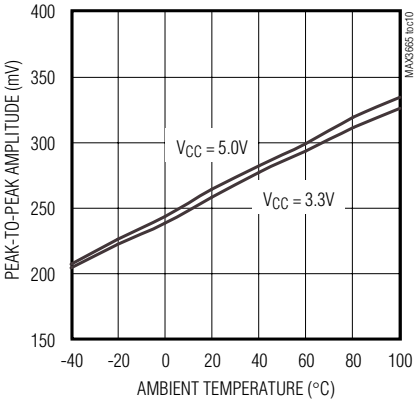


622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamplifier for SDH/SONET

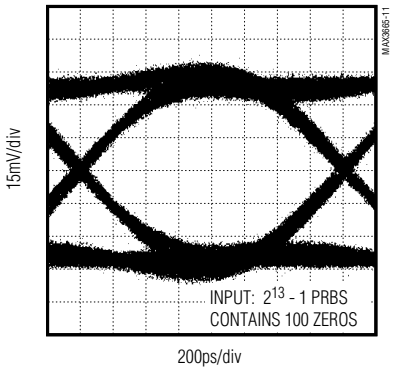
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, includes off-chip filter, see Figure 3b, T_A = +25°C, unless otherwise noted.)

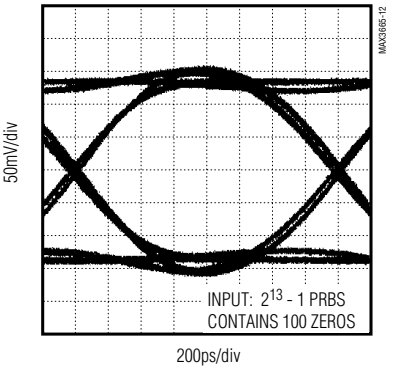
DIFFERENTIAL OUTPUT AMPLITUDE vs. TEMPERATURE (INPUT = 450µAP-P)



EYE DIAGRAM (INPUT = 10µAP-P)



EYE DIAGRAM (INPUT = 450µAP-P)



Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	+3.3V or +5.0V Supply Voltage
2	IN	Signal Input (From Photodiode)
3	N.C.	No Connection. Not internally connected.
4	FILT	On-Chip Resistor for Filtering Photodiode Supply Voltage
5, 8	GND	Ground
6	OUT+	Noninverting Voltage Output. Current flowing into IN causes V_{OUT+} to increase.
7	OUT-	Inverting Voltage Output. Current flowing into IN causes V_{OUT-} to decrease.

Detailed Description

The MAX3665 is a transimpedance amplifier designed for 622Mbps SDH/SONET applications. It comprises a transimpedance amplifier, a paraphase amplifier with CML differential outputs, and a DC cancellation loop. Figure 1 shows a functional diagram of the MAX3665.

Transimpedance Amplifier

The signal current at IN flows into the summing node of a high-gain amplifier. Shunt feedback through R_F converts this current to a voltage. Diodes D1 and D2 clamp the output voltage for large input currents.

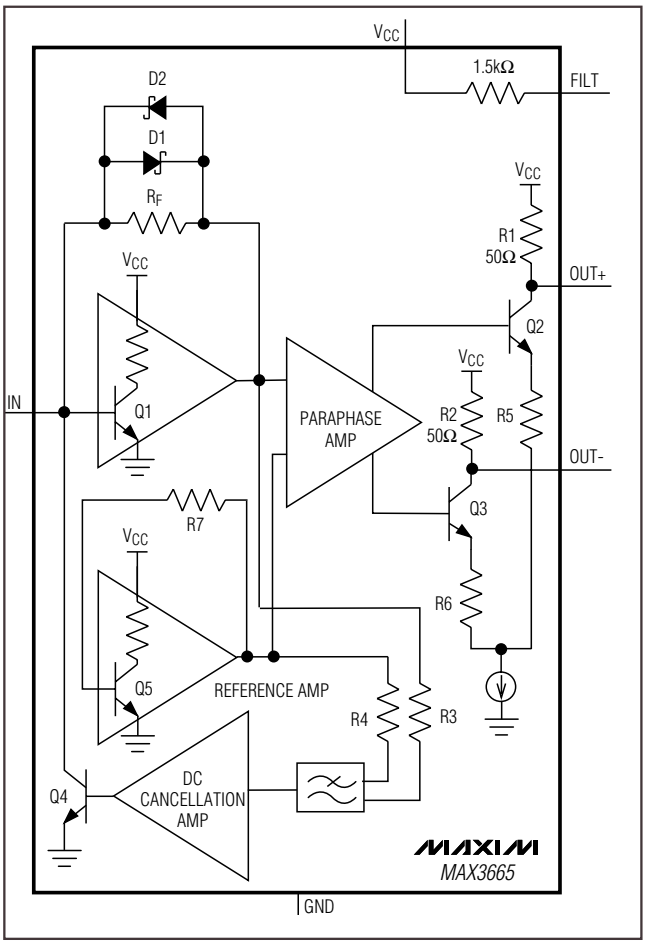


Figure 1. Functional Diagram

Paraphase Amplifier

The paraphase amplifier converts single-ended inputs to differential outputs, and introduces a voltage gain. This signal drives a differential pair of transistors, Q2 and Q3, which form the output stage. Resistors R1 and R2 provide back-termination at the output, absorbing reflections between the MAX3665 and its load.

The differential outputs are designed to drive a 100Ω load between OUT+ and OUT-. They can also drive higher output impedances, resulting in increased gain and output voltage swing.

DC Cancellation Loop

The DC cancellation loop removes the DC component of the input signal by using low-frequency feedback. This feature centers the signal within the MAX3665's dynamic range, reducing pulse-width distortion on large input signals.

The output of the transimpedance amplifier is sensed through resistors R3 and R4 and then filtered, amplified, and fed back to the base of transistor Q4. The transistor draws the DC component of the input signal away from the transimpedance amplifier's summing node.

Connect a 400pF or larger capacitor (C_{FILT}) between FILT and case ground for TO header, die-mounted operation. Increasing C_{FILT} improves PSRR. The DC cancellation loop can sink up to 300µA of current at the input.

The MAX3665 minimizes pulse-width distortion for data sequences that exhibit a 50% mark density. A mark density other than 50% causes the device to generate pulse-width distortion.

DC cancellation current is drawn from the input and adds noise. For low-level signals with little or no DC component, this is not a problem. Preamplifier noise will increase for signals with a significant DC component.

Applications Information

The MAX3665 is a low-noise, wide-bandwidth transimpedance amplifier that is ideal for 622Mbps SDH/SONET receivers. Its features allow easy design into a fiber optic module, in three simple steps.

Step 1: Selecting a Preamplifier for a 622Mbps Receiver

Fiber optic systems place requirements on the bandwidth, gain, and noise of the transimpedance preamplifier. The MAX3665 optimizes these characteristics for SDH/SONET receiver applications that operate at 622Mbps.

In general, the bandwidth of a fiber optic preamplifier should be 0.6 to 1 times the data rate. Therefore, in a 622Mbps system, the bandwidth should be between 375MHz and 622MHz. Lower bandwidth causes pattern-dependent jitter and a lower signal-to-noise ratio, while higher bandwidth increases thermal noise. The MAX3665 typical bandwidth is 470MHz, making it ideal for 622Mbps applications.

The preamplifier's transimpedance must be high enough to ensure that expected input signals generate output levels exceeding the sensitivity of the limiting amplifier (quantizer) in the following stage. The MAX3676 clock recovery and limiting amplifier IC has an input sensitivity of $3.6mV_{P-P}$, which means that $3.6mV_{P-P}$ is the minimum signal amplitude required to produce a fully limited output. Therefore, when used with the MAX3665, which has an 8kΩ transimpedance, the minimum detectable photodetector current is $450nA_{P-P}$.

It is common to relate peak-to-peak input signals to average optical power. The relationship between optical input power and output current for a photodetector is called the responsivity (ρ), with units amperes per watt (A/W). The photodetector peak-to-peak current is related to the peak-to-peak optical power as follows:

$$I_{P-P} = (P_{P-P})(\rho)$$

Based on the assumption that SDH/SONET signals maintain a 50% mark density, the following equations relate peak-to-peak optical power to average optical power and extinction ratio (Figure 2):

Average Optical Power = P_{AVG} = (P0 + P1) / 2

Extinction Ratio = r_e = P1 / P0

Peak-to-Peak Signal Amplitude = P_{P-P} = P1 - P0

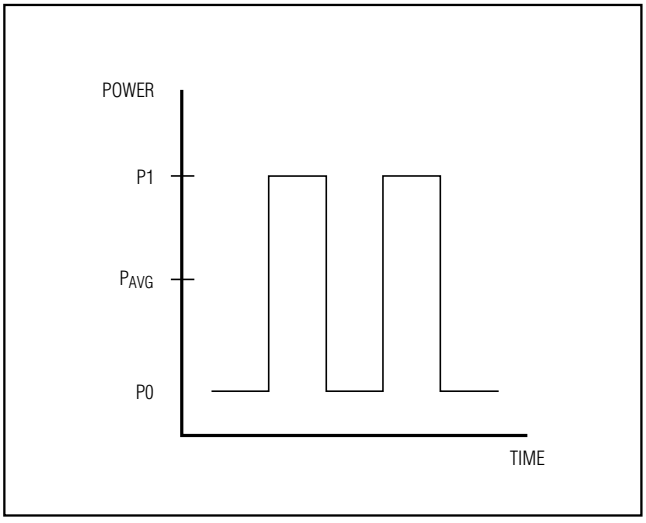


Figure 2. Optical Power Definitions

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Therefore,

$$P_{AVG} = P_{P-P} (1 / 2)[(r_e + 1) / (r_e - 1)]$$

Sensitivity is a key specification of the receiver module. The ITU/Bellcore specifications for SDH/SONET receivers require a link sensitivity of -27dBm with a bit error rate (BER) of 10^{-10}. There is an additional 1dB power penalty to accommodate various system losses; therefore, the sensitivity of a 622Mbps receiver must be better than -28dBm.

Although several parameters affect sensitivity (such as the quantizer sensitivity and preamplifier gain, as previously discussed), most fiber optic receivers are designed so that noise is the dominant factor. Noise from the high-gain transimpedance amplifier, in particular, determines the sensitivity. The noise generated by the MAX3665 can be modeled with a Gaussian distribution. In this case, a BER of 10^{-10} corresponds to a peak-to-peak signal amplitude to RMS noise ratio (SNR) of 12.7. The MAX3665's typical input-referred noise, i_n, (bandwidth-limited to 470MHz) is $55nA_{RMS}$. Therefore, the minimum input for a BER of 10^{-10} is (12.7 • 55nA) = $699nA_{P-P}$. Rearranging the previous equations in these terms results in the following relationship:

$$\text{Optical Sensitivity (dBm)} = 10\log[(i_n / \rho)(SNR)(1/2)(r_e + 1) / (r_e - 1)(1000)]$$

At room temperature, with r_e = 10, SNR = 12.7, i_n = 55nA, and ρ = 0.9A/W, the MAX3665 sensitivity is -33.2dBm. For worst-case conditions, noise increases to 72nA and sensitivity decreases to -32.1dBm. The MAX3665 provides 5.1dB margin over the SDH/SONET specifications, even at +85°C.

The MAX3665's overload current (I_{MAX}) is greater than $450\mu A_{P-P}$. The pulse-width distortion and input current are closely related. If the clock recovery circuit can accept more pulse-width distortion, a higher input current might be acceptable. For worst-case responsivity and extinction ratio, ρ = 1A/W and $r_e = \infty$, the input overload is:

$$\text{Overload (dBm)} = -10\log (I_{MAX})(1 / 2)(1000)$$

For I_{MAX} = 450µA, the MAX3665 overload is -6.5dBm.

Step 2: Designing Filters

The MAX3665's noise performance is a strong function of the circuit's bandwidth, which changes over temperature and varies from lot to lot. The receiver sensitivity can be improved by adding filters to limit this bandwidth. Filter designs can range from a one-pole filter using a single capacitor, to more complex filters using inductors. Figure 3 illustrates two examples: the simple filter provides moderate roll-off with minimal components, while the complex filter provides a sharper roll-off. Parasitics on the PC board will affect the filter characteristics. Refer to the MAX3665 EV kit data sheet for a layout example of the filter shown in Figure 3b.

Supply voltage noise at the cathode of the photodiode produces a current $I = C_{PHOTO} (\Delta V/\Delta t)$, which reduces the receiver sensitivity. C_{PHOTO} is the photodiode capacitance.

The FILT resistor of the MAX3665, combined with an external capacitor (see *Typical Operating Circuit*) can be used to reduce this noise. The external capacitor (C_{FILT}) is placed in parallel with the photodiode. Current generated by supply noise is divided between C_{FILT} and C_{PHOTO}. The input noise current due to supply noise is (assuming the filter capacitor is much larger than the photodiode capacitance):

$$I_{NOISE} = \frac{(V_{NOISE})(C_{PHOTO})}{(R_{FILT})(C_{FILT})}$$

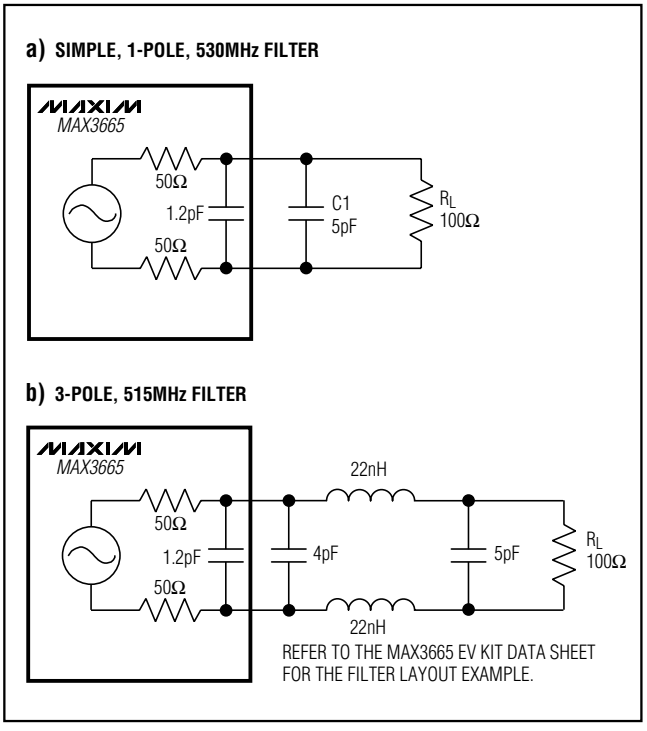

Figure 3. Filter Design Examples

If the amount of tolerable noise is known, then the filter capacitor can be easily selected:

$$C_{FILT} = \frac{(V_{NOISE})(C_{PHOTO})}{(R_{FILT})(I_{NOISE})}$$

For example, with maximum noise voltage = $100mV_{P-P}$, C_{PHOTO} = 0.5pF, R_{FILT} = 1.5kΩ, and I_{NOISE} selected to be 6nA (1/10 of MAX3665 input-referred noise):

$$C_{FILT} = (0.1)\left(0.5 \cdot 10^{-12}\right) / \left[(1500)\left(6 \cdot 10^{-4}\right)\right] = 5.6nF$$

Figure 4 shows the suggested layout for a TO-46 header

Step 3: Designing a Low-Capacitance Input

Noise performance and bandwidth are adversely affected by stray capacitance on the input node. Select a low-capacitance photodiode and use good high-frequency design and layout techniques to minimize capacitance on this pin. The MAX3665 is optimized for 0.5pF of capacitance on the input—approximately the capacitance of a photodetector diode sharing a common header with the MAX3665 in die form.

Photodiode capacitance changes significantly with bias voltage. With a +3.3V supply voltage, the reverse voltage on the PIN diode is only 2.5V. If a higher voltage supply is available, apply it to the diode to significantly reduce capacitance.

Take great care to reduce input capacitance. With the µMAX version of the MAX3665, the package capacitance is about 0.3pF, and the PC board between the MAX3665 input and the photodiode can add parasitic capacitance. Keep the input line short, and remove power and ground planes beneath it. Packaging the MAX3665 into a header with the photodiode provides the best possible performance. It reduces parasitic capacitance to a minimum, resulting in the lowest noise and the best bandwidth.

Wire Bonding

For high current density and reliable operation, the MAX3665 uses gold metallization. Make connections to the die with gold wire only, and use ball-bonding techniques (wedge-bonding is not recommended). Die-pad size is 4 mils square. Die thickness is 16 mils.

VCC and Ground

Use good high-frequency design and layout techniques. The use of a multilayer circuit board with separate ground and V_{CC} planes is recommended. Take care to bypass V_{CC} and to connect the GND pin to the ground plane with the shortest possible traces.

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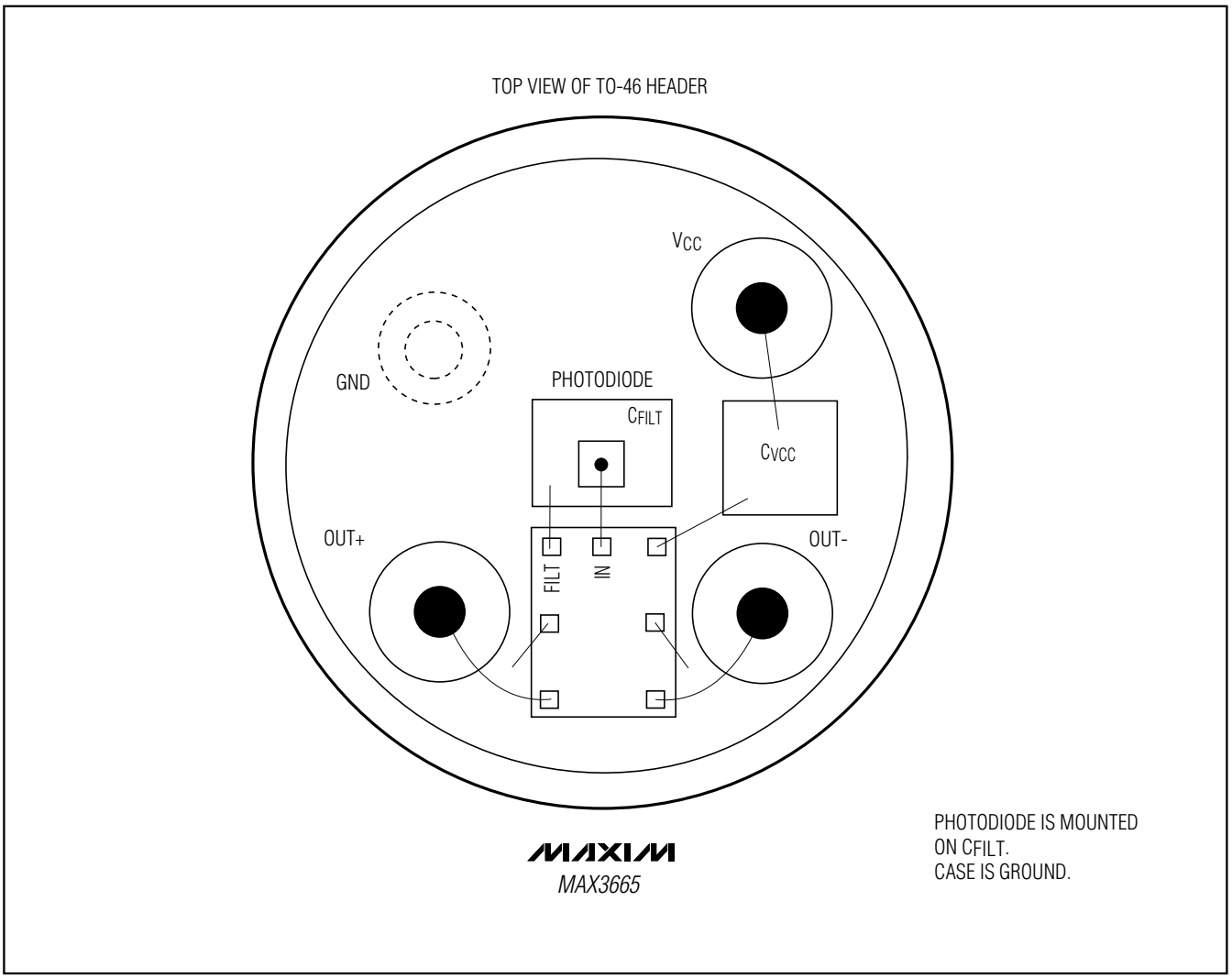

Figure 4. Suggested Layout for TO-46 Header

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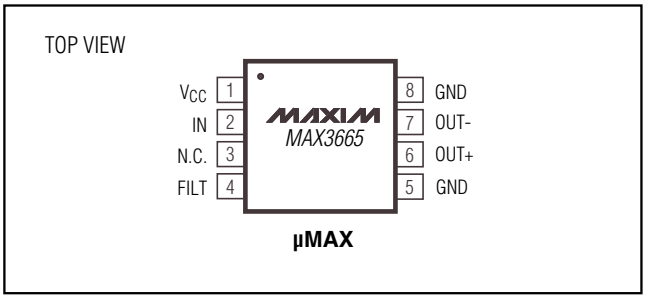
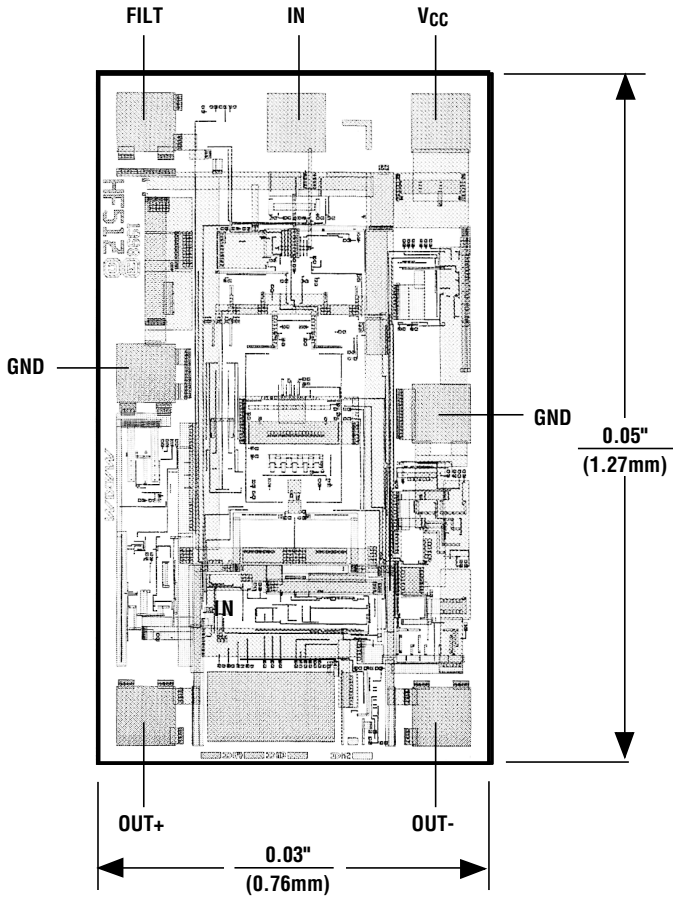
Pin Configuration



Chip Topography



TRANSISTOR COUNT: 443

SUBSTRATE CONNECTED TO GND

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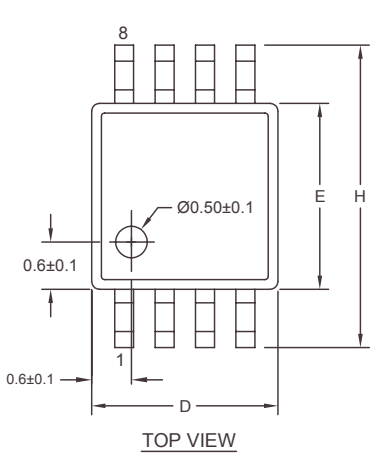
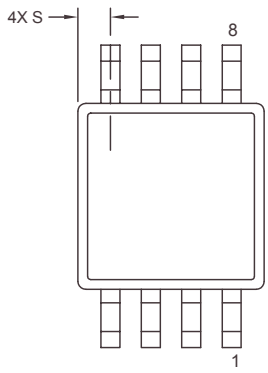
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

8LUMAXD.EPS

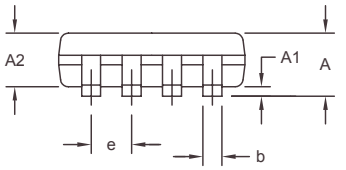


TOP VIEW

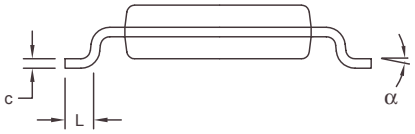


BOTTOM VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC	



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-AA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP

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	21-0036	J	1/1