REJ03B0013-0141
Rev.1.41
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1. Overview

The M32C/83 Group (M32C/83, M32C/83T) microcomputer is a single-chip control unit that utilizes high-performance silicon gate CMOS technology with the M32C/80 Series CPU core. The M32C/83 Group (M32C/83, M32C/83T) is available in 144-pin and 100-pin plastic molded LQFP/QFP packages.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It includes a multiplier and DMAC adequate for office automation, communication devices and industrial equipments, and other high-speed processing applications.

1.1 Applications

Automobiles, audio, cameras, office equipment, communications equipment, portable equipment, etc.

1.2 Performance Overview

Tables 1.1 and 1.2 list performance overview of the M32C/83 Group (M32C/83, M32C/83T).

Table 1.1 M32C/83 Group (M32C/83, M32C/83T) Performance (144-Pin Package)

Characteristic		Performance	
		M32C/83	M32C/83T
CPU	Basic Instructions	108 instructions	
	Minimum Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, VCC=4.2 to 5.5 V)(3) 50 ns (f(BCLK)=20 MHz, VCC=3.0 to 5.5 V)	31.3 ns (f(BCLK)=32 MHz, VCC=4.2 to 5.5 V)(3)
	Operating Mode	Single-chip mode, Memory expansion mode and Microprocessor mode	Single-chip mode
	Address Space	16 Mbytes	
	Memory Capacity	See Table 1.3	
Peripheral Function	I/O Port	123 I/O pins and 1 input pin	
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit	
	Intelligent I/O	Time measurement function: 16 bits x 12 channels Waveform generating function: 16 bits x 28 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing, Clock synchronous variable length serial I/O, IEBus(1), 8-bit or 16-bit Clock synchronous serial I/O)	
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I2C bus(2)	
	CAN Module	1 channel Supporting CAN 2.0B specification	
	A/D Converter	10-bit A/D converter: 2 circuit, 34 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	4 channels	
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions	
	DRAM	CAS before RAS refresh, Self-reflesh, EDO, EP	
	CRC Calculation Circuit	CRC-CCITT	
	X/Y Converter	16 bits x 16 bits	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	42 internal and 8 external sources, 5 software sources, Interrupt priority level: 7	
	Clock Generation Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally	
	Oscillation Stop Detect Function	Main clock oscillation stop detect function	
Electrical Characteristics	Supply Voltage	4.2 to 5.5 V (f(BCLK)=32 MHz) 3.0 to 5.5 V (f(BCLK)=20 MHz, through VDC) 3.0 to 3.6 V (f(BCLK)=20 MHz, not through VDC)	4.2 to 5.5 V (f(BCLK)=32 MHz)
	Power Consumption	41 mA (VCC=5 V, f(BCLK)=32 MHz) 38 mA (VCC=5 V, f(BCLK)=30 MHz) 26 mA (VCC=3.3 V, f(BCLK)=20 MHz) 470 µA (VCC=5 V, f(XCIN)=32 kHz, in wait mode) 340 µA (VCC=3.3 V, f(XCIN)=32 kHz, through VDC, in wait mode) 5.0 µA (VCC=3.3 V, f(XCIN)=32 kHz, not through VDC, in wait mode) 0.4 µA (VCC=5 V, stop mode) 0.4 µA (VCC=3.3 V, stop mode)	41 mA (VCC=5 V, f(BCLK)=32 MHz) 38 mA (VCC=5 V, Vf(BCLK)=30 MHz) 470 µA (VCC=5 V, f(XCIN)=32 kHz, in wait mode) 0.4 µA (VCC=5 V, stop mode)
Flash Memory	Program/Erase Supply Voltage	3.3 ± 0.3 V or 5.0 ± 0.5 V	5.0 ± 0.5 V
	Program and Erase Endurance	100 times	
Operating Ambient Temperature		–20 to 85°C, –40 to 85°C (optional)	–40 to 85°C (T version)
Package		144-pin plastic molded LQFP	

NOTES:
1. IEBus is a trademark of NEC Electronics Corporation.
2. I2C bus is a trademark of Koninklijke Philips Electronics N. V.
3. Contact our sales office if 30-MHz or higher frequency is required.

All options are on a request basis.

Table 1.2 M32C/83 Group (M32C/83, M32C/83T) Performance (100-Pin Package)

Characteristic		Performance	
		M32C/83	M32C/83T
CPU	Basic Instructions	108 instructions	
	Minimum Instruction Execution Time	31.3 ns (f(BCLK) = 32 MHz, VCC = 4.2 to 5.5 V) 50 ns (f(BCLK) = 20 MHz, VCC = 3.0 to 5.5 V)	31.3 ns (f(BCLK) = 32 MHz, VCC=4.2 to 5.5 V)
	Operating Mode	Single-chip mode, Memory expansion mode and Microprocessor mode	Single-chip mode
	Address Space	16 Mbytes	
	Memory Capacity	See Table 1.3	
Peripheral Function	I/O Port	87 I/O pins and 1 input pin	
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit	
	Intelligent I/O	Time measurement function: 16 bits x 5 channels Waveform generating function: 16 bits x 10 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing, Clock synchronous variable length serial I/O, IEBus(1))	
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I2C bus(2)	
	CAN Module	1 channel Supporting CAN 2.0B specification	
	A/D Converter	10-bit A/D converter: 2 circuits, 26 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	4 channels	
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions	
	CRC Calculation Circuit	CRC-CCITT	
	X/Y Converter	16 bits x 16 bits	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	42 internal and 8 external sources, 5 software sources Interrupt priority level: 7	
	Clock Generation Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally	
	Oscillation Stop Detect Function	Main clock oscillation stop detect function	
Electrical Characteristics	Supply Voltage	4.2 to 5.5 V (f(BCLK)=32 MHz) 3.0 to 5.5 V (f(BCLK)=20 MHz, through VDC) 3.0 to 3.6 V (f(BCLK)=20 MHz, not through VDC)	4.2 to 5.5 V (f(BCLK)=32 MHz)
	Power Consumption	41 mA (VCC=5 V, f(BCLK)=32 MHz) 38 mA (VCC=5 V, f(BCLK)=30 MHz) 26 mA (VCC=3.3 V, f(BCLK)=20 MHz) 470 µA (VCC=5 V, f(XCIN)=32 kHz, in wait mode) 340 µA (VCC=3.3 V, f(XCIN)=32 kHz, through VDC, in wait mode) 5.0 µA (VCC=3.3 V, f(XCIN)=32 kHz, not through VDC, in wait mode) 0.4 µA (VCC=5 V, stop mode) 0.4 µA (VCC=3.3 V, stop mode)	41 mA (VCC=5 V, f(BCLK)=32 MHz) 38 mA (VCC=5 V, Vf(BCLK)=30 MHz) 470 µA (VCC=5 V, f(XCIN)=32 kHz, in wait mode) 0.4 µA (VCC=5 V, stop mode)
Flash Memory	Program/Erase Supply Voltage	3.3 ± 0.3 V or 5.0 ± 0.5 V	5.0 ± 0.5 V
	Program and Erase Endurance	100 times	
Operating Ambient Temperature		–20 to 85°C, –40 to 85°C (optional)	–40 to 85°C (T version)
Package		100-pin plastic molded LQFP/QFP	

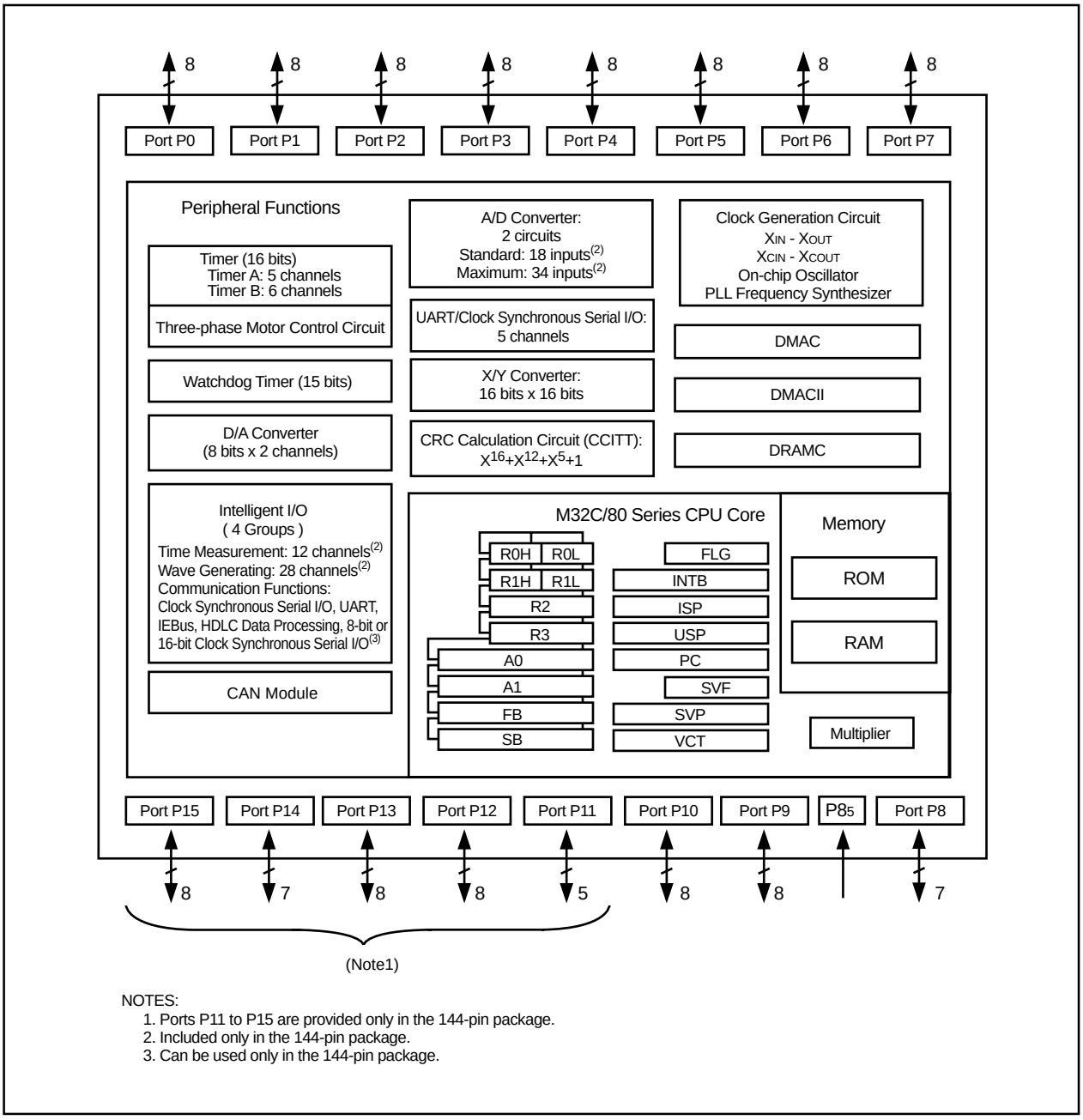
NOTES:

1. IEBus is a trademark of NEC Electronics Corporation.
2. I2C bus is a trademark of Koninklijke Philips Electronics N. V.
3. Contact our sales office if 30-MHz or higher frequency is required.

All options are on a request basis.

1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/83 Group (M32C/83, M32C/83T) microcomputer.



NOTES:
1. Ports P11 to P15 are provided only in the 144-pin package.
2. Included only in the 144-pin package.
3. Can be used only in the 144-pin package.

Figure 1.1 M32C/83 Group (M32C/83, M32C/83T) Block Diagram

1.4 Product Information

Table 1.3 lists the product information. Figure 1.2 shows the product numbering system.

Table 1.3 M32C/83 Group (1) (M32C/83) **As of January, 2006**

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30835FJGP	PLQP0144KA-A (144P6Q-A)	512K	31K	Flash Memory
M30833FJGP	PLQP0100KB-A (100P6Q-A)			
M30833FJFP	PRQP0100JB-A (100P6S-A)			

Table 1.3 M32C/83 Group (2) (T Version, M32C/83T) **As of January, 2006**

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30833FJTGP	PLQP0100KB-A (100P6Q-A)	512K	31K	Flash Memory T Version (High-reliability 85ºC Version)

Please contact our sales office for V version information.

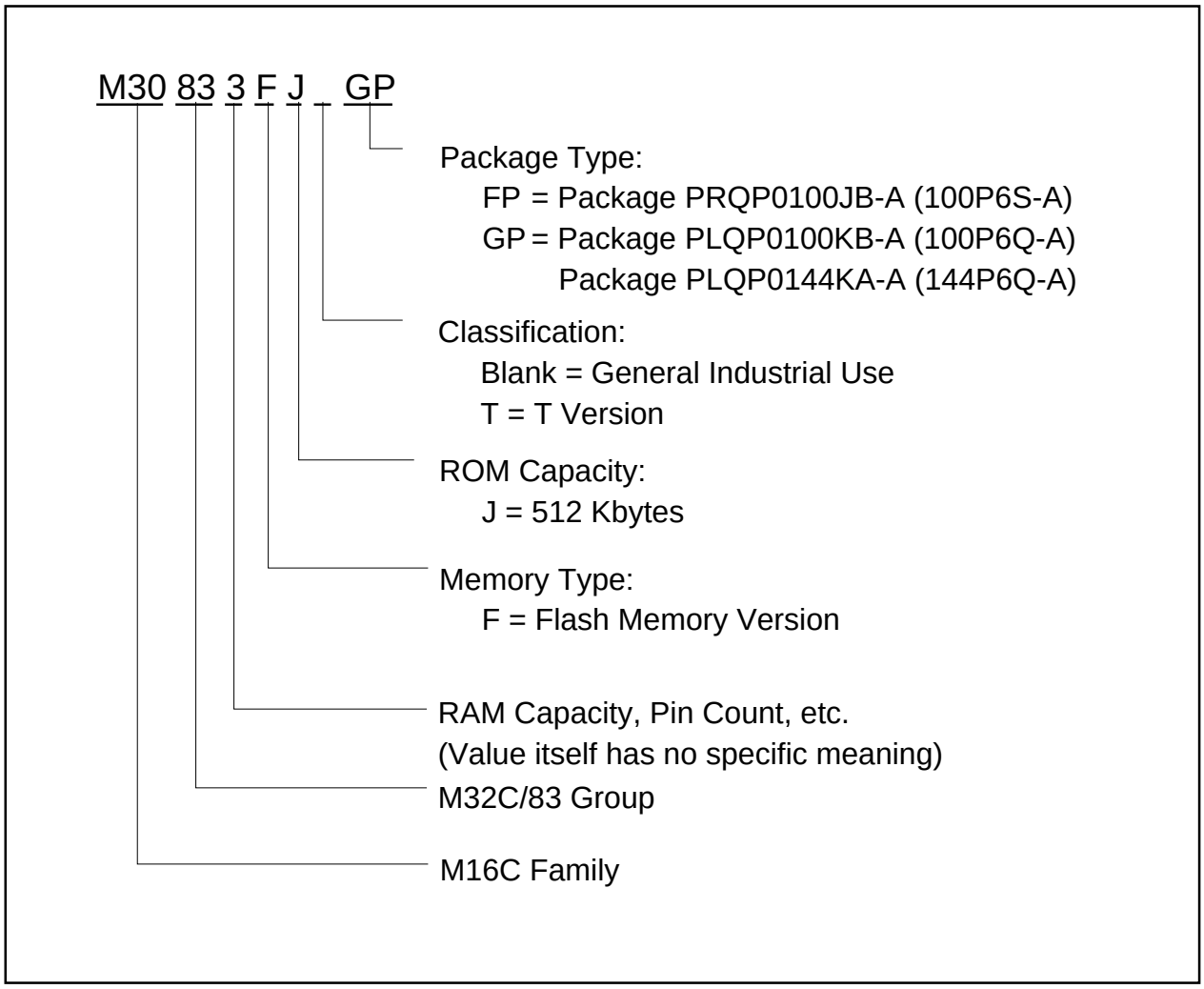


Figure 1.2 Product Numbering System

1.5 Pin Assignment

Figures 1.3 to 1.5 show pin assignments (top view).

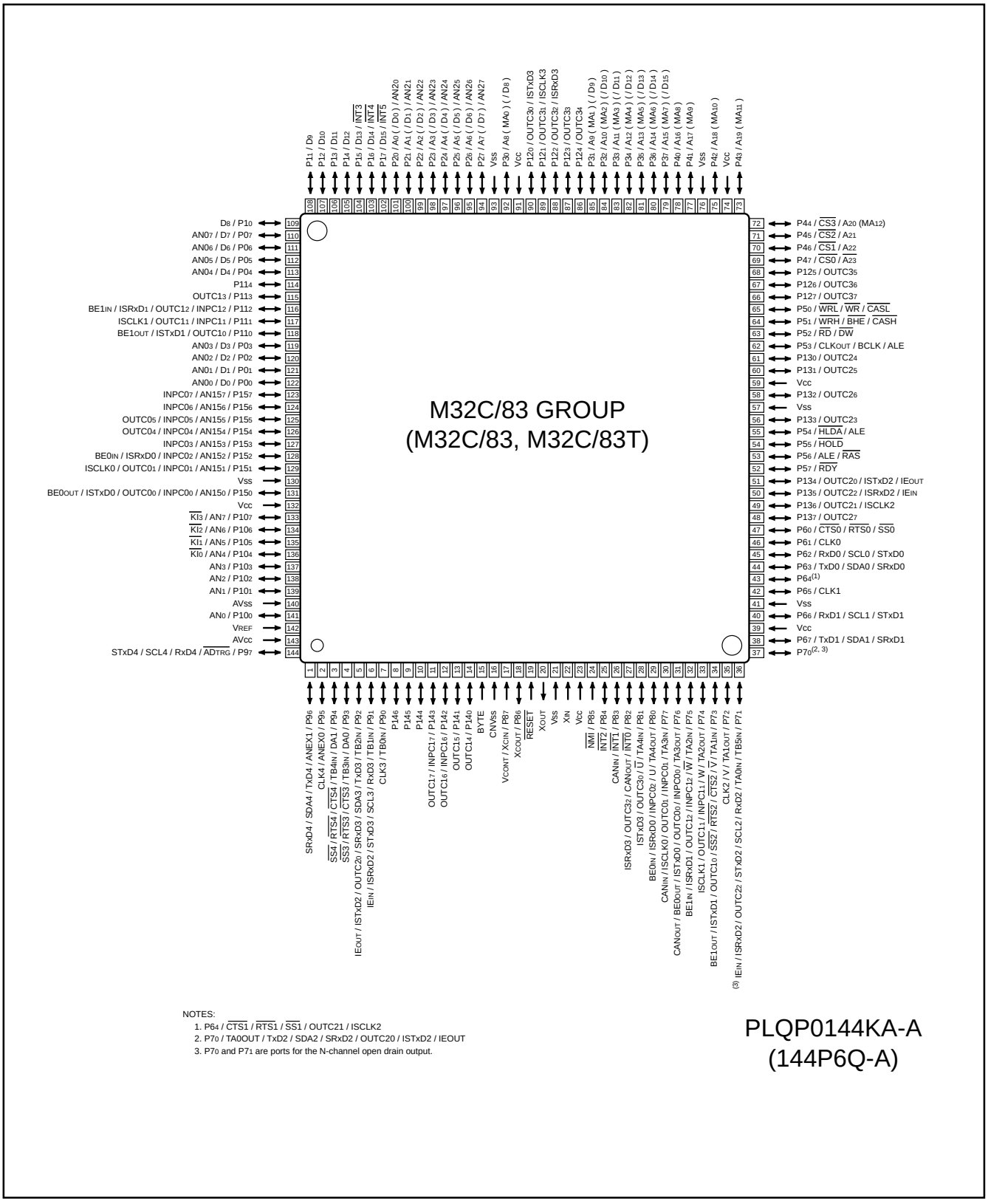


Figure 1.3 Pin Assignment for 144-Pin Package

Table 1.4 Pin Characteristics for 144-Pin Package

Pin No	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
1		P9$_6$			TxD4/SDA4/SRxD4		ANEX1	
2		P9$_5$			CLK4		ANEX0	
3		P9$_4$		TB4$_{IN}$	$\overline{CTS4}$/$\overline{RTS4}$/$\overline{SS4}$		DA1	
4		P9$_3$		TB3$_{IN}$	$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$		DA0	
5		P9$_2$		TB2$_{IN}$	TxD3/SDA3/SRxD3	OUTC2$_0$/IE$_{OUT}$/ISTxD2		
6		P9$_1$		TB1$_{IN}$	RxD3/SCL3/STxD3	IE$_{IN}$/ISRxD2		
7		P9$_0$		TB0$_{IN}$	CLK3			
8		P14$_6$						
9		P14$_5$						
10		P14$_4$						
11		P14$_3$				INPC1$_7$/OUTC1$_7$		
12		P14$_2$				INPC1$_6$/OUTC1$_6$		
13		P14$_1$				OUTC1$_5$		
14		P14$_0$				OUTC1$_4$		
15	BYTE							
16	CNV$_{SS}$							
17	X$_{CIN}$/V$_{CONT}$	P8$_7$						
18	X$_{COUT}$	P8$_6$						
19	$\overline{RESET}$							
20	X$_{OUT}$							
21	V$_{SS}$							
22	X$_{IN}$							
23	V$_{CC}$							
24		P8$_5$	$\overline{NMI}$					
25		P8$_4$	$\overline{INT2}$					
26		P8$_3$	$\overline{INT1}$		CAN$_{IN}$			
27		P8$_2$	$\overline{INT0}$		CAN$_{OUT}$	OUTC3$_2$/ISRxD3		
28		P8$_1$		TA4$_{IN}$/$\overline{U}$		OUTC3$_0$/ISTxD3		
29		P8$_0$		TA4$_{OUT}$/U		INPC0$_2$/ISRxD0/BE0$_{IN}$		
30		P7$_7$		TA3$_{IN}$	CAN$_{IN}$	INPC0$_1$/OUTC0$_1$/ISCLK0		
31		P7$_6$		TA3$_{OUT}$	CAN$_{OUT}$	INPC0$_0$/OUTC0$_0$/ISTxD0/BE0$_{OUT}$		
32		P7$_5$		TA2$_{IN}$/$\overline{W}$		INPC1$_2$/OUTC1$_2$/ISRxD1/BE1$_{IN}$		
33		P7$_4$		TA2$_{OUT}$/W		INPC1$_1$/OUTC1$_1$/ISCLK1		
34		P7$_3$		TA1$_{IN}$/$\overline{V}$	$\overline{CTS2}$/$\overline{RTS2}$/$\overline{SS2}$	OUTC1$_0$/ISTxD1/BE1$_{OUT}$		
35		P7$_2$		TA1$_{OUT}$/V	CLK2			
36		P7$_1$		TB5$_{IN}$/TA0$_{IN}$	RxD2/SCL2/STxD2	OUTC2$_2$/ISRxD2/IE$_{IN}$		
37		P7$_0$		TA0$_{OUT}$	TxD2/SDA2/SRxD2	OUTC2$_0$/ISTxD2/IE$_{OUT}$		
38		P6$_7$			TxD1/SDA1/SRxD1			
39	V$_{CC}$							
40		P6$_6$			RxD1/SCL1/STxD1			
41	V$_{SS}$							
42		P6$_5$			CLK1			
43		P6$_4$			$\overline{CTS1}$/$\overline{RTS1}$/$\overline{SS1}$	OUTC2$_1$/ISCLK2		
44		P6$_3$			TxD0/SDA0/SRxD0			
45		P6$_2$			RxD0/SCL0/STxD0			
46		P6$_1$			CLK0			
47		P6$_0$			$\overline{CTS0}$/$\overline{RTS0}$/$\overline{SS0}$			
48		P13$_7$				OUTC2$_7$		

NOTES:

1. Bus control pins in M32C/83T cannot be used.

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
49		P13$_6$				OUTC2$_1$/ISCLK2		
50		P13$_5$				OUTC2$_2$/ISRxD2/IE$_{IN}$		
51		P13$_4$				OUTC2$_0$/ISTxD2/IE$_{OUT}$		
52		P5$_7$						$\overline{RDY}$
53		P5$_6$						ALE/$\overline{RAS}$
54		P5$_5$						$\overline{HOLD}$
55		P5$_4$						$\overline{HLDA}$/ALE
56		P13$_3$				OUTC2$_3$		
57	V$_{SS}$							
58		P13$_2$				OUTC2$_6$		
59	V$_{CC}$							
60		P13$_1$				OUTC2$_5$		
61		P13$_0$				OUTC2$_4$		
62		P5$_3$						CLK$_{OUT}$/BCLK/ALE
63		P5$_2$						$\overline{RD}$/$\overline{DW}$
64		P5$_1$						$\overline{WRH}$/$\overline{BHE}$/$\overline{CASH}$
65		P5$_0$						$\overline{WRL}$/$\overline{WR}$/$\overline{CASL}$
66		P12$_7$				OUTC3$_7$		
67		P12$_6$				OUTC3$_6$		
68		P12$_5$				OUTC3$_5$		
69		P4$_7$						$\overline{CS0}$/A$_{23}$
70		P4$_6$						$\overline{CS1}$/A$_{22}$
71		P4$_5$						$\overline{CS2}$/A$_{21}$
72		P4$_4$						$\overline{CS3}$/A$_{20}$(MA$_{12}$)
73		P4$_3$						A$_{19}$(MA$_{11}$)
74	V$_{CC}$							
75		P4$_2$						A$_{18}$(MA$_{10}$)
76	V$_{SS}$							
77		P4$_1$						A$_{17}$(MA$_9$)
78		P4$_0$						A$_{16}$(MA$_8$)
79		P3$_7$						A$_{15}$(MA$_7$)(/D$_{15}$)
80		P3$_6$						A$_{14}$(MA$_6$)(/D$_{14}$)
81		P3$_5$						A$_{13}$(MA$_5$)(/D$_{13}$)
82		P3$_4$						A$_{12}$(MA$_4$)(/D$_{12}$)
83		P3$_3$						A$_{11}$(MA$_3$)(/D$_{11}$)
84		P3$_2$						A$_{10}$(MA$_2$)(/D$_{10}$)
85		P3$_1$						A$_9$(MA$_1$)(/D$_9$)
86		P12$_4$				OUTC3$_4$		
87		P12$_3$				OUTC3$_3$		
88		P12$_2$				OUTC3$_2$/ISRxD3		
89		P12$_1$				OUTC3$_1$/ISCLK3		
90		P12$_0$				OUTC3$_0$/ISTxD3		
91	V$_{CC}$							
92		P3$_0$						A$_8$(MA$_0$)(/D$_8$)
93	V$_{SS}$							
94		P2$_7$					AN2$_7$	A$_7$(/D$_7$)
95		P2$_6$					AN2$_6$	A$_6$(/D$_6$)
96		P2$_5$					AN2$_5$	A$_5$(/D$_5$)

NOTES:

1. Bus control pins in M32C/83T cannot be used.

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
97		P2$_4$					AN2$_4$	A$_4$(/D$_4$)
98		P2$_3$					AN2$_3$	A$_3$(/D$_3$)
99		P2$_2$					AN2$_2$	A$_2$(/D$_2$)
100		P2$_1$					AN2$_1$	A$_1$(/D$_1$)
101		P2$_0$					AN2$_0$	A$_0$(/D$_0$)
102		P1$_7$	$\overline{\text{INT5}}$					D$_{15}$
103		P1$_6$	$\overline{\text{INT4}}$					D$_{14}$
104		P1$_5$	$\overline{\text{INT3}}$					D$_{13}$
105		P1$_4$						D$_{12}$
106		P1$_3$						D$_{11}$
107		P1$_2$						D$_{10}$
108		P1$_1$						D$_9$
109		P1$_0$						D$_8$
110		P0$_7$					AN0$_7$	D$_7$
111		P0$_6$					AN0$_6$	D$_6$
112		P0$_5$					AN0$_5$	D$_5$
113		P0$_4$					AN0$_4$	D$_4$
114		P11$_4$						
115		P11$_3$				OUTC1$_3$		
116		P11$_2$				INPC1$_2$/OUTC1$_2$/ISRxD1/BE1$_{IN}$		
117		P11$_1$				INPC1$_1$/OUTC1$_1$/ISCLK1		
118		P11$_0$				OUTC1$_0$/ISTxD1/BE1$_{OUT}$		
119		P0$_3$					AN0$_3$	D$_3$
120		P0$_2$					AN0$_2$	D$_2$
121		P0$_1$					AN0$_1$	D$_1$
122		P0$_0$					AN0$_0$	D$_0$
123		P15$_7$				INPC0$_7$	AN15$_7$	
124		P15$_6$				INPC0$_6$	AN15$_6$	
125		P15$_5$				INPC0$_5$/OUTC0$_5$	AN15$_5$	
126		P15$_4$				INPC0$_4$/OUTC0$_4$	AN15$_4$	
127		P15$_3$				INPC0$_3$	AN15$_3$	
128		P15$_2$				INPC0$_2$/ISRxD0/BE0$_{IN}$	AN15$_2$	
129		P15$_1$				INPC0$_1$/OUTC0$_1$/ISCLK0	AN15$_1$	
130	V$_{SS}$							
131		P15$_0$				INPC0$_0$/OUTC0$_0$/ISTxD0/BE0$_{OUT}$	AN15$_0$	
132	V$_{CC}$							
133		P10$_7$	$\overline{\text{KI}_3}$				AN$_7$	
134		P10$_6$	$\overline{\text{KI}_2}$				AN$_6$	
135		P10$_5$	$\overline{\text{KI}_1}$				AN$_5$	
136		P10$_4$	$\overline{\text{KI}_0}$				AN$_4$	
137		P10$_3$					AN$_3$	
138		P10$_2$					AN$_2$	
139		P10$_1$					AN$_1$	
140	AV$_{SS}$							
141		P10$_0$					AN$_0$	
142	V$_{REF}$							
143	AV$_{CC}$							
144		P9$_7$			RxD4/SCL4/STxD4		$\overline{\text{ADTRG}}$	

NOTES:

1. Bus control pins in M32C/83T cannot be used.

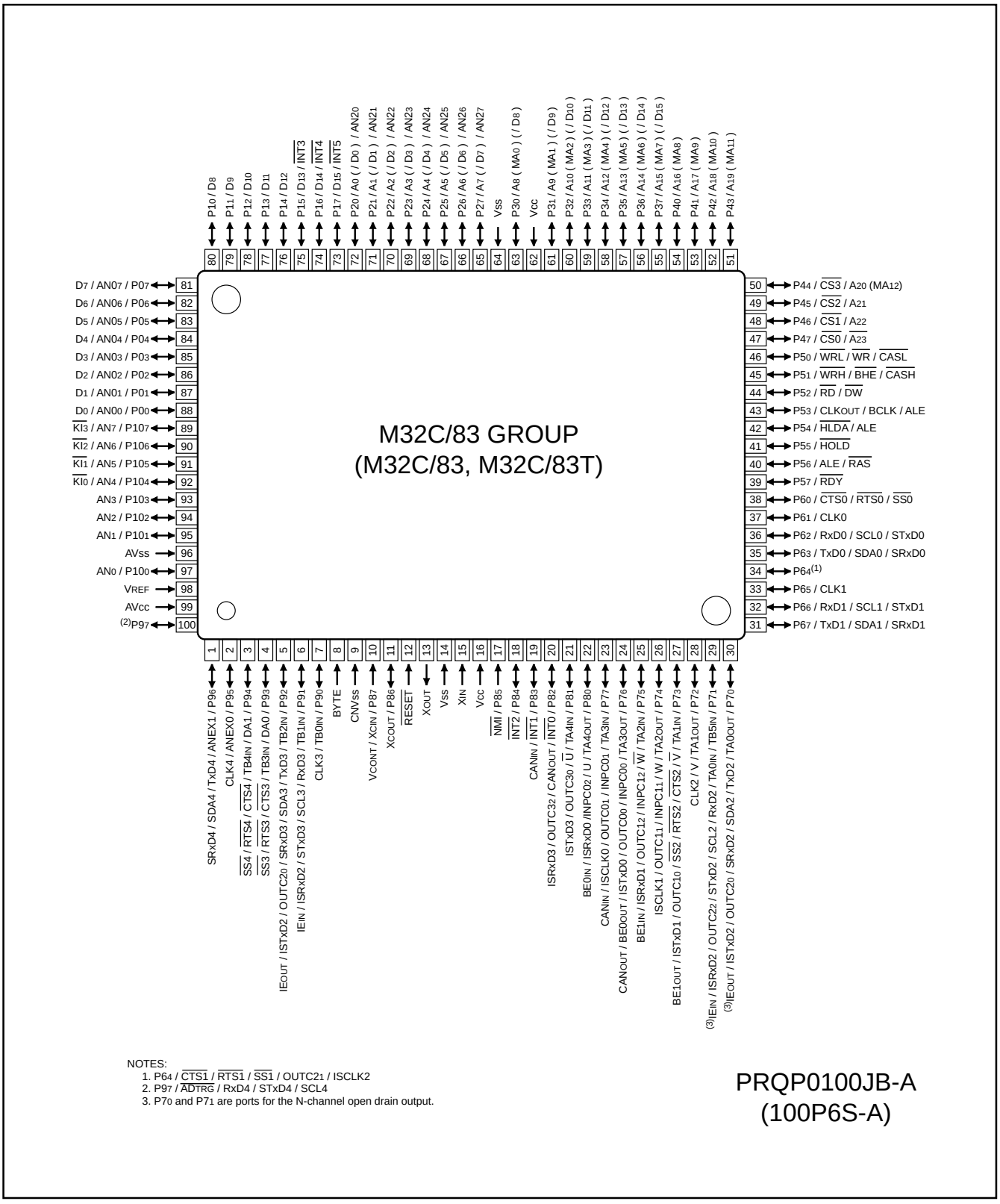


Figure 1.4 Pin Assignment for 100-Pin Package

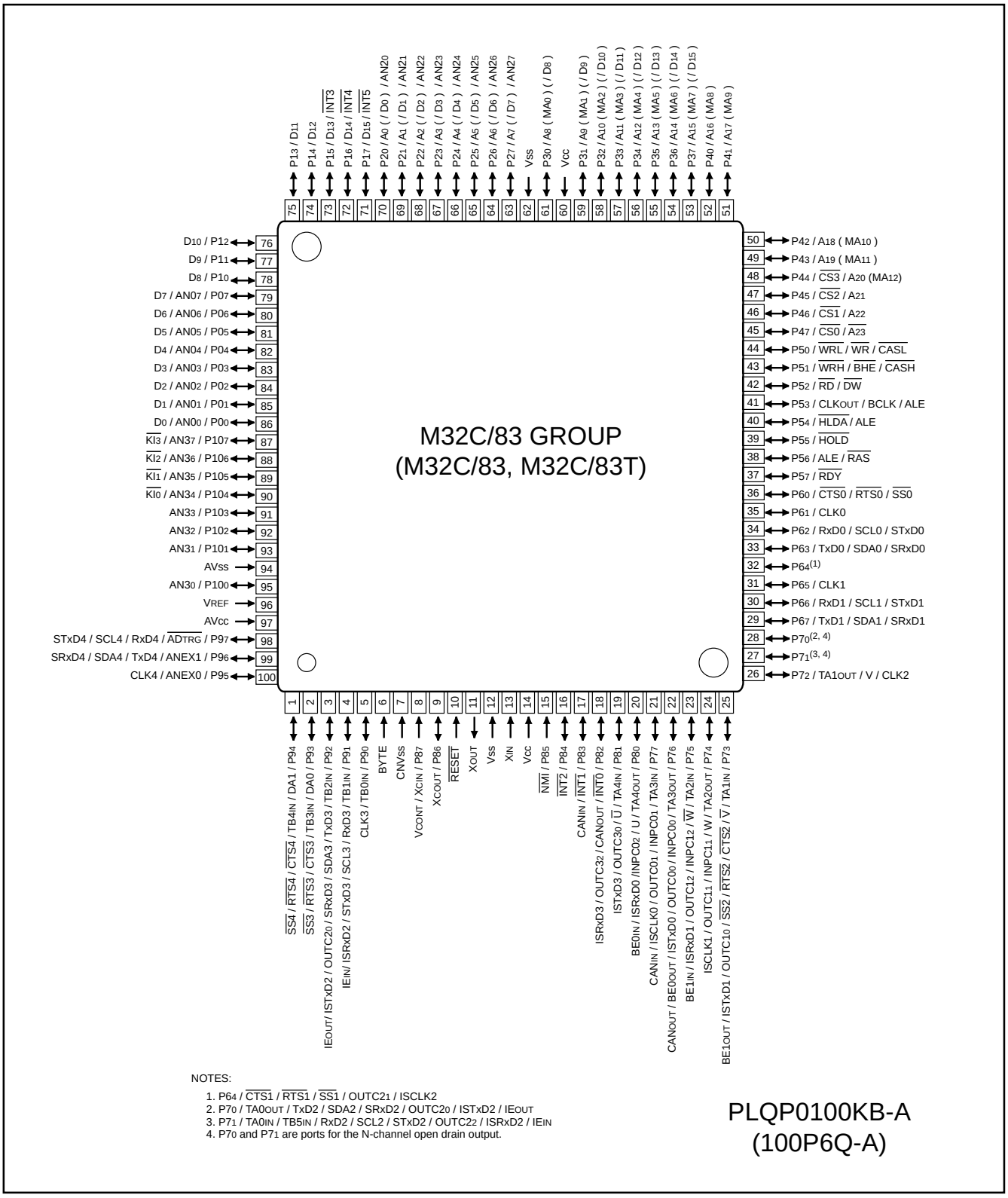


Figure 1.5 Pin Assignment for 100-Pin Package

Table 1.5 Pin Characteristics for 100-Pin Package

Package Pin No		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
FP	GP								
1	99		P9$_6$			TxD4/SDA4/SRxD4		ANEX1	
2	100		P9$_5$			CLK4		ANEX0	
3	1		P9$_4$		TB4$_{IN}$	$\overline{CTS4}$/$\overline{RTS4}$/$\overline{SS4}$		DA1	
4	2		P9$_3$		TB3$_{IN}$	$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$		DA0	
5	3		P9$_2$		TB2$_{IN}$	TxD3/SDA3/SRxD3	OUTC2$_0$/IE$_{OUT}$/ISTxD2		
6	4		P9$_1$		TB1$_{IN}$	RxD3/SCL3/STxD3	IE$_{IN}$/ISRxD2		
7	5		P9$_0$		TB0$_{IN}$	CLK3			
8	6	BYTE							
9	7	CNV$_{SS}$							
10	8	X$_{CIN}$/V$_{CONT}$	P8$_7$						
11	9	X$_{COUT}$	P8$_6$						
12	10	$\overline{RESET}$							
13	11	X$_{OUT}$							
14	12	V$_{SS}$							
15	13	X$_{IN}$							
16	14	V$_{CC}$							
17	15		P8$_5$	$\overline{NMI}$					
18	16		P8$_4$	$\overline{INT2}$					
19	17		P8$_3$	$\overline{INT1}$		CAN$_{IN}$			
20	18		P8$_2$	$\overline{INT0}$		CAN$_{OUT}$	OUTC3$_2$/ISRxD3		
21	19		P8$_1$		TA4$_{IN}$/$\overline{U}$		OUTC3$_0$/ISTxD3		
22	20		P8$_0$		TA4$_{OUT}$/U		INPC0$_2$/ISRxD0/BE0$_{IN}$		
23	21		P7$_7$		TA3$_{IN}$	CAN$_{IN}$	INPC0$_1$/OUTC0$_1$/ISCLK0		
24	22		P7$_6$		TA3$_{OUT}$	CAN$_{OUT}$	INPC0$_0$/OUTC0$_0$/ISTxD0/BE0$_{OUT}$		
25	23		P7$_5$		TA2$_{IN}$/$\overline{W}$		INPC1$_2$/OUTC1$_2$/ISRxD1/BE1$_{IN}$		
26	24		P7$_4$		TA2$_{OUT}$/W		INPC1$_1$/OUTC1$_1$/ISCLK1		
27	25		P7$_3$		TA1$_{IN}$/$\overline{V}$	$\overline{CTS2}$/$\overline{RTS2}$/$\overline{SS2}$	OUTC1$_0$/ISTxD1/BE1$_{OUT}$		
28	26		P7$_2$		TA1$_{OUT}$/V	CLK2			
29	27		P7$_1$		TB5$_{IN}$/TA0$_{IN}$	RxD2/SCL2/STxD2	OUTC2$_2$/ISRxD2/IE$_{IN}$		
30	28		P7$_0$		TA0$_{OUT}$	TxD2/SDA2/SRxD2	OUTC2$_0$/ISTxD2/IE$_{OUT}$		
31	29		P6$_7$			TxD1/SDA1/SRxD1			
32	30		P6$_6$			RxD1/SCL1/STxD1			
33	31		P6$_5$			CLK1			
34	32		P6$_4$			$\overline{CTS1}$/$\overline{RTS1}$/$\overline{SS1}$	OUTC2$_1$/ISCLK2		
35	33		P6$_3$			TxD0/SDA0/SRxD0			
36	34		P6$_2$			RxD0/SCL0/STxD0			
37	35		P6$_1$			CLK0			
38	36		P6$_0$			$\overline{CTS0}$/$\overline{RTS0}$/$\overline{SS0}$			
39	37		P5$_7$						$\overline{RDY}$
40	38		P5$_6$						ALE/$\overline{RAS}$
41	39		P5$_5$						$\overline{HOLD}$
42	40		P5$_4$						$\overline{HLDA}$/ALE
43	41		P5$_3$						CLK$_{OUT}$/BCLK/ALE
44	42		P5$_2$						$\overline{RD}$/$\overline{DW}$
45	43		P5$_1$						$\overline{WRH}$/$\overline{BHE}$/$\overline{CASH}$
46	44		P5$_0$						$\overline{WRL}$/$\overline{WR}$/$\overline{CASL}$
47	45		P4$_7$						$\overline{CS0}$/A$_{23}$
48	46		P4$_6$						$\overline{CS1}$/A$_{22}$
49	47		P4$_5$						$\overline{CS2}$/A$_{21}$
50	48		P4$_4$						$\overline{CS3}$/A$_{20}$(MA$_{12}$)

NOTES:

1. Bus control pins in M32C/83T cannot be used.

Table 1.5 Pin Characteristics for 100-Pin Package (Continued)

Package Pin No		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
FP	GP								
51	49		$P4_3$						$A_{19}(MA_{11})$
52	50		$P4_2$						$A_{18}(MA_{10})$
53	51		$P4_1$						$A_{17}(MA_9)$
54	52		$P4_0$						$A_{16}(MA_8)$
55	53		$P3_7$						$A_{15}(MA_7)(/D_{15})$
56	54		$P3_6$						$A_{14}(MA_6)(/D_{14})$
57	55		$P3_5$						$A_{13}(MA_5)(/D_{13})$
58	56		$P3_4$						$A_{12}(MA_4)(/D_{12})$
59	57		$P3_3$						$A_{11}(MA_3)(/D_{11})$
60	58		$P3_2$						$A_{10}(MA_2)(/D_{10})$
61	59		$P3_1$						$A_9(MA_1)(/D_9)$
62	60	V_{CC}							
63	61		$P3_0$						$A_8(MA_0)(/D_8)$
64	62	V_{SS}							
65	63		$P2_7$					$AN2_7$	$A_7(/D_7)$
66	64		$P2_6$					$AN2_6$	$A_6(/D_6)$
67	65		$P2_5$					$AN2_5$	$A_5(/D_5)$
68	66		$P2_4$					$AN2_4$	$A_4(/D_4)$
69	67		$P2_3$					$AN2_3$	$A_3(/D_3)$
70	68		$P2_2$					$AN2_2$	$A_2(/D_2)$
71	69		$P2_1$					$AN2_1$	$A_1(/D_1)$
72	70		$P2_0$					$AN2_0$	$A_0(/D_0)$
73	71		$P1_7$	$\overline{INT5}$					D_{15}
74	72		$P1_6$	$\overline{INT4}$					D_{14}
75	73		$P1_5$	$\overline{INT3}$					D_{13}
76	74		$P1_4$						D_{12}
77	75		$P1_3$						D_{11}
78	76		$P1_2$						D_{10}
79	77		$P1_1$						D_9
80	78		$P1_0$						D_8
81	79		$P0_7$					$AN0_7$	D_7
82	80		$P0_6$					$AN0_6$	D_6
83	81		$P0_5$					$AN0_5$	D_5
84	82		$P0_4$					$AN0_4$	D_4
85	83		$P0_3$					$AN0_3$	D_3
86	84		$P0_2$					$AN0_2$	D_2
87	85		$P0_1$					$AN0_1$	D_1
88	86		$P0_0$					$AN0_0$	D_0
89	87		$P10_7$	$\overline{KI_3}$				AN_7	
90	88		$P10_6$	$\overline{KI_2}$				AN_6	
91	89		$P10_5$	$\overline{KI_1}$				AN_5	
92	90		$P10_4$	$\overline{KI_0}$				AN_4	
93	91		$P10_3$					AN_3	
94	92		$P10_2$					AN_2	
95	93		$P10_1$					AN_1	
96	94	AV_{SS}							
97	95		$P10_0$					AN_0	
98	96	V_{REF}							
99	97	AV_{CC}							
100	98		$P9_7$			RxD4/SCL4/STxD4		$\overline{ADTRG}$	

NOTES:

1. Bus control pins in M32C/83T cannot be used.

1.6 Pin Description

Table 1.6 Pin Description (100-Pin and 144-Pin Packages)

Classsfication	Symbol	I/O Type	Function
Power Supply	VCC VSS	I	Apply 3.0 to 5.5V to both VCC pin. Apply 0V to the VSS pin. (1)
Analog Power Supply	AVCC AVSS	I	Supplies power to the A/D converter. Connect the AVCC pin to VCC and the AVSS pin to VSS
Reset Input	$\overline{\text{RESET}}$	I	The microcomputer is in a reset state when "L" is applied to the $\overline{\text{RESET}}$ pin
CNVSS	CNVSS	I	Switches processor mode. Connect the CNVSS pin to VSS to start up in single-chip mode or to VCC to start up in microprocessor mode
Input to Switch External Data Bus Width(2)	BYTE	I	Switches data bus width in external memory space 3. The data bus is 16 bits wide when the BYTE pin is held "L" and 8 bits wide when it is held "H". Set to either. Connect the BYTE pin to VSS to use the microcomputer in single-chip mode
Bus Control Pins(2)	D0 to D7	I/O	Inputs and outputs data (D0 to D7) while accessing an external memory space with separate bus
	D8 to D15	I/O	Inputs and outputs data (D8 to D15) while accessing an external memory space with 16-bit separate bus
	A0 to A22	O	Outputs address bits A0 to A22
	$\overline{\text{A23}}$	O	Outputs inversed address bit A23
	A0/D0 to A7/D7	I/O	Inputs and outputs data (D0 to D7) and outputs 8 low-order address bits (A0 to A7) by time-sharing while accessing an external memory space with multiplexed bus
	A8/D8 to A15/D15	I/O	Inputs and outputs data (D8 to D15) and outputs 8 middle-order address bits (A8 to A15) by time-sharing while accessing an external memory space with 16-bit multiplexed bus
	$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	O	Outputs $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ that are chip-select signals specifying an external space
	$\overline{\text{WRL}}$ / $\overline{\text{WR}}$ $\overline{\text{WRH}}$ / $\overline{\text{BHE}}$ $\overline{\text{RD}}$	O	Outputs $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, ($\overline{\text{WR}}$, $\overline{\text{BHE}}$) and $\overline{\text{RD}}$ signals. $\overline{\text{WRL}}$ and $\overline{\text{WRH}}$ can be switched with $\overline{\text{WR}}$ and $\overline{\text{BHE}}$ by program ■ $\overline{\text{WRL}}$, $\overline{\text{WRH}}$ and $\overline{\text{RD}}$ selected: If external data bus is 16 bits wide, data is written to an even address in external memory space when $\overline{\text{WRL}}$ is held "L". Data is written to an odd address when $\overline{\text{WRH}}$ is held "L". Data is read when $\overline{\text{RD}}$ is held "L". ■ $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ selected: Data is written to external memory space when $\overline{\text{WR}}$ is held "L". Data in an external memory space is read when $\overline{\text{RD}}$ is held "L". An odd address is accessed when $\overline{\text{BHE}}$ is held "L". Select $\overline{\text{WR}}$, $\overline{\text{BHE}}$ and $\overline{\text{RD}}$ for external 8-bit data bus.
	ALE	O	ALE is a signal latching the address
	$\overline{\text{HOLD}}$	I	The microcomputer is placed in a hold state while the $\overline{\text{HOLD}}$ pin is held "L"
	$\overline{\text{HLDA}}$	O	Outputs an "L" signal while the microcomputer is placed in a hold state
	$\overline{\text{RDY}}$	I	Bus is placed in a wait state while the $\overline{\text{RDY}}$ pin is held "L"
DRAM Bus Control Pin(2)	MA0 to MA12	O	When DRAM area is accessed, outputs column and row addresses by time-sharing.
	$\overline{\text{DW}}$ $\overline{\text{CASL}}$ $\overline{\text{CASH}}$ $\overline{\text{RAS}}$	O	The $\overline{\text{DW}}$ signal becomes "L" when data is written to the DRAM area. $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$ are signals indicating the timing to latch column addresses. The $\overline{\text{CASL}}$ signal becomes "L" when an even address is accessed. The $\overline{\text{CASH}}$ signal becomes "L" when an odd address is accessed. $\overline{\text{RAS}}$ is a signal latching row addresses.

I : Input O : Output I/O : Input and output

NOTES:

1. Apply 4.2 to 5.5V to the VCC pin when using M32C/83T.
2. Bus control pins in M32C/83T cannot be used.

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Classsfication	Symbol	I/O Type	Function
Main Clock Input	XIN	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open
Main Clock Output	XOUT	O	
Sub Clock Input	XCIN	I	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT. To apply external clock, apply it to XCIN and leave XCOUT open
Sub Clock Output	XCOUT	O	
Low-Pass Filter Connect Pin for PLL Frequency Synthesizer Pin	VCONT		Connects the low-pass filter to the VCONT pin when using the PLL frequency synthesizer. Connect P86 to VSS to stabilize the PLL frequency.
BCLK Output(1)	BCLK	O	Outputs BCLK signal
Clock Output	CLKOUT	O	Outputs the clock having the same frequency as fC, f8 or f32
$\overline{\text{INT}}$ Interrupt Input	$\overline{\text{INT0}}$ to $\overline{\text{INT5}}$	I	Input pins for the $\overline{\text{INT}}$ interrupt
$\overline{\text{NMI}}$ Interrupt Input	$\overline{\text{NMI}}$	I	Input pin for the $\overline{\text{NMI}}$ interrupt
Key Input Interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	I/O pins for the timer A0 to A4 (TA0OUT is a pin for the N-channel open drain output.)
	TA0IN to TA4IN	I	Input pins for the timer A0 to A4
Timer B	TB0IN to TB5IN	I	Input pins for the timer B0 to B5
Three-phase Motor Control Timer Output	U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$	O	Output pins for the three-phase motor control timer
Serial I/O	$\overline{\text{CTS0}}$ to $\overline{\text{CTS4}}$	I	Input pins for data transmission control
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS4}}$	O	Output pins for data reception control
	CLK0 to CLK4	I/O	Inputs and outputs the transfer clock
	RxD0 to RxD4	I	Inputs serial data
	TxD0 to TxD4	O	Outputs serial data (TxD2 is a pin for the N-channel open drain output.)
I^2C Mode	SDA0 to SDA4	I/O	Inputs and outputs serial data (SDA2 is a pin for the N-channel open drain output.)
	SCL0 to SCL4		Inputs and outputs the transfer clock (SCL2 is a pin for the N-channel open drain output.)

I : Input O : Output I/O : Input and output

NOTE:

1. Bus control pins in M32C/83T cannot be used.

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Classsfication	Symbol	I/O Type	Function
Serial I/O Special Function	STxD0 to STxD4	O	Outputs serial data when slave mode is selected
	SRxD0 to SRxD4	I	Inputs serial data when slave mode is selected
	$\overline{SS0}$ to $\overline{SS4}$	I	Input pins to control serial I/O special function
Reference Voltage Input	VREF	I	Applies reference voltage to the A/D converter and D/A converter
A/D Converter	AN0 to AN7 AN00 to AN07 AN20 to AN27	I	Analog input pins for the A/D converter
	AN150 to AN157		
	$\overline{ADTRG}$	I	Input pin for an external A/D trigger
	ANEX0	I/O	Extended analog input pin for the A/D converter and output pin in external op-amp connection mode
	ANEX1	I	Extended analog input pin for the A/D converter
D/A Converter	DA0, DA1	O	Output pin for the D/A converter
Intelligent I/O	INPC00 to INPC02	I	Input pins for the time measurement function
	INPC03 to INPC07(1)		
	INPC11 to INPC12		
	INPC16 to INPC17(1)		
	OUTC00 to OUTC02	O	Output pins for the waveform generating function (OUTC20 and OUTC22 assigned to P70 and P71 are pins for the N-channel open drain output.)
	OUTC04 to OUTC05(1)		
	OUTC10 to OUTC12		
	OUTC13 to OUTC17(1)		
	OUTC20 to OUTC22		
	OUTC23 to OUTC27(1)		
	OUTC30 to OUTC32		
	OUTC31, OUTC33 to OUTC37(1)		
	ISCLK0 to ISCLK2	I/O	Inputs and outputs the clock for the intelligent I/O communication function
	ISCLK3(1)		
	ISRXD0 to ISRXD3	I	Inputs data for the intelligent I/O communication function
	ISTXD0 to ISTXD3	O	Outputs data for the intelligent I/O communication function
	BE0IN, BE1IN	I	Inputs data for the intelligent I/O communication function
	BE0OUT, BE1OUT	O	Outputs data for the intelligent I/O communication function
	IEIN	I	Inputs data for the intelligent I/O communication function
	IEOUT	O	Outputs data for the intelligent I/O communication function
CAN	CANIN	I	Input pin for the CAN communication function
	CANOUT	O	Output pin for the CAN communication function

I : Input O : Output I/O : Input and output

NOTE:

1. Available in the 144-pin package only.

Table 1.6 Pin Description (144-Pin Package only) (Continued)

Classsfication	Symbol	I/O Type	Function
I/O Ports	$P0_0$ to $P0_7$ $P1_0$ to $P1_7$ $P2_0$ to $P2_7$ $P3_0$ to $P3_7$ $P4_0$ to $P4_7$ $P5_0$ to $P5_7$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P9_0$ to $P9_7$ $P10_0$ to $P10_7$	I/O	8-bit I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units ($P7_0$ and $P7_1$ are ports for the N-channel open drain output.)
	$P11_0$ to $P11_4$ $P12_0$ to $P12_7$ $P13_0$ to $P13_7$ $P14_0$ to $P14_6$ $P15_0$ to $P15_7$ (1)	I/O	I/O ports having equivalent functions to P0
	$P8_0$ to $P8_4$ $P8_6$, $P8_7$	I/O	I/O ports having equivalent functions to P0
Input Port	$P8_5$	I	Shares a pin with $\overline{NMI}$. $\overline{NMI}$ input state can be got by reading $P8_5$

I : Input O : Output I/O : Input and output

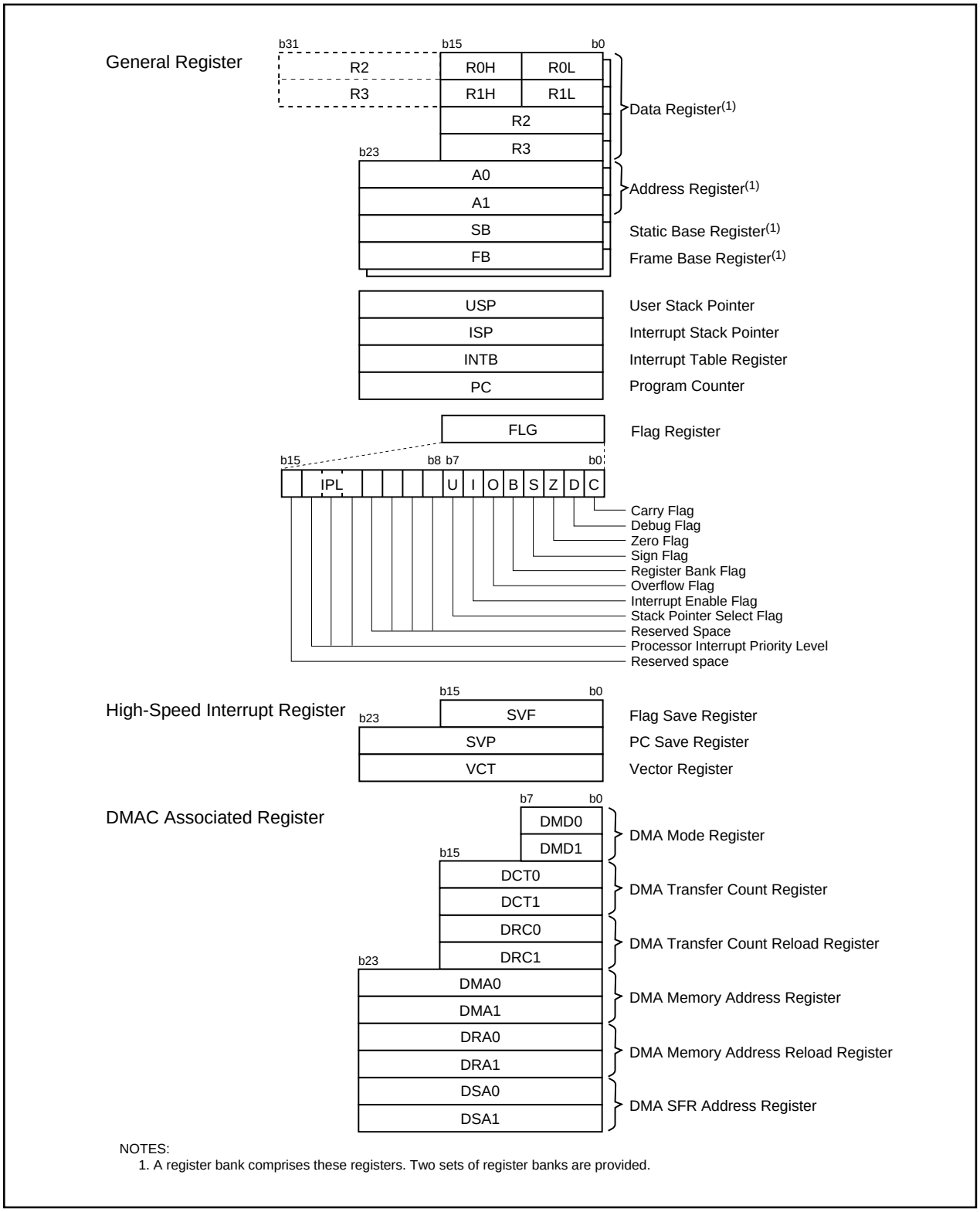
NOTE:

1. Available in the 144-pin package only.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

A register bank comprises 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.



NOTES:
1. A register bank comprises these registers. Two sets of register banks are provided.

Figure 2.1 CPU Register

2.1 General Registers

2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R3.

2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

2.1.3 Static Base Register (SB)

SB is a 24-bit register for SB-relative addressing.

2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

2.1.5 Program Counter (PC)

PC, 24 bits wide, indicates the address of an instruction to be executed.

2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating the starting address of an interrupt vector table.

2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are 24 bits wide each. The U flag is used to switch between USP and ISP. Refer to "2.1.8 Flag Register (FLG)" for details on the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating a CPU state.

2.1.8.1 Carry Flag (C)

The C flag indicates whether carry or borrow has occurred after executing an instruction.

2.1.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.1.8.3 Zero Flag (Z)

The Z flag is set to "1" when the value of zero is obtained from an arithmetic calculation; otherwise "0".

2.1.8.4 Sign Flag (S)

The S flag is set to "1" when a negative value is obtained from an arithmetic calculation; otherwise "0".

2.1.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

2.1.8.6 Overflow Flag (O)

The O flag is set to "1" when the result of an arithmetic operation overflows; otherwise "0".

2.1.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.
An interrupt is disabled when the I flag is set to "0" and enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".
The U flag is set to "0" when a hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.1.8.10 Reserved Space

When writing to a reserved space, set to "0". When read, its content is indeterminate.

2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows. Refer to **10.4 High-Speed Interrupt** for details.

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-Associated Registers

Registers associated with DMAC are as follows. Refer to **12. DMAC** for details.

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

3. Memory

Figure 3.1 shows a memory map of the M32C/83 group (M32C/83, M32C/83T).

M32C/83 group (M32C/83, M32C/83T) provides 16-Mbyte address space from addresses 000000$_{16}$ to FFFFFF$_{16}$.

The internal ROM is allocated lower addresses beginning with address FFFFFF$_{16}$. For example, a 64-Kbyte internal ROM is allocated addresses FF0000$_{16}$ to FFFFFF$_{16}$.

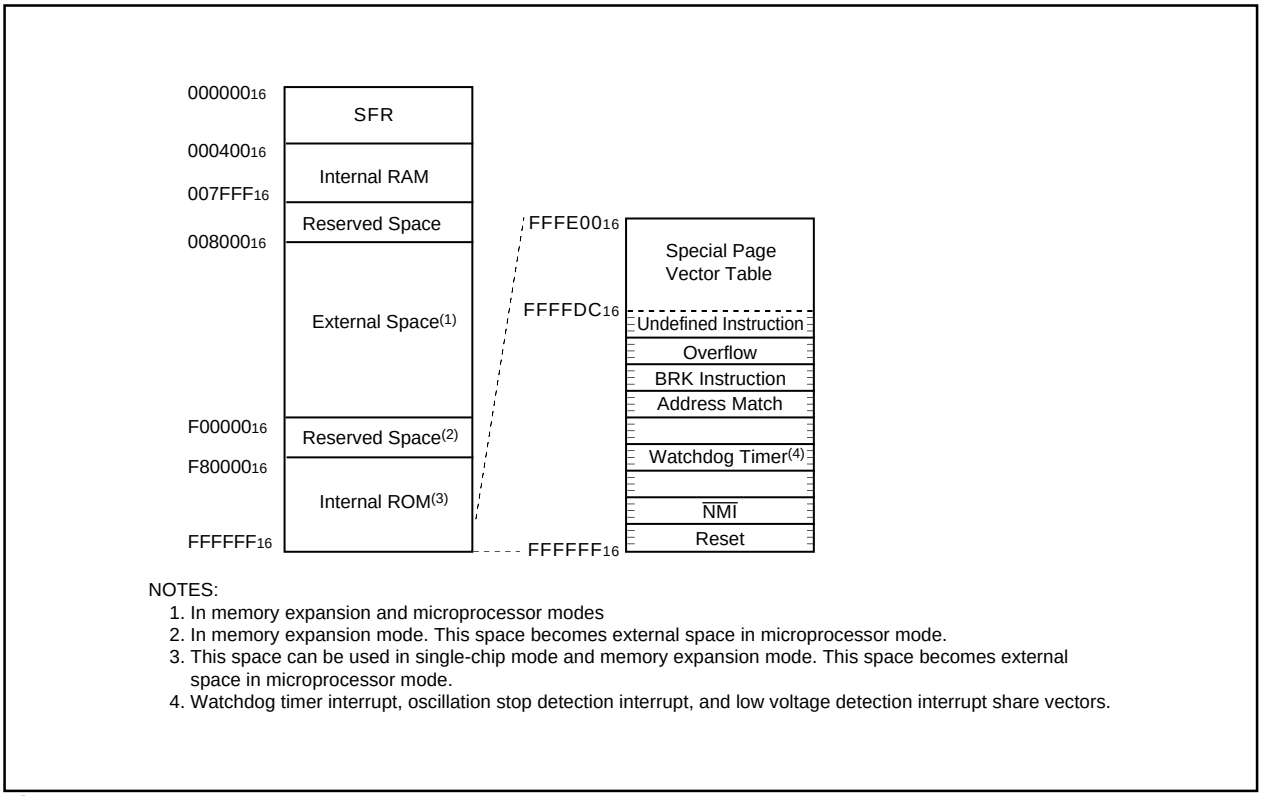
The fixed interrupt vectors are allocated addresses FFFFDC$_{16}$ to FFFFFF$_{16}$. It stores the starting address of each interrupt routine. Refer to **10. Interrupts** for details.

The internal RAM is allocated higher addresses beginning with address 000400$_{16}$. For example, a 10-Kbyte internal RAM is allocated addresses 000400$_{16}$ to 002BFF$_{16}$. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFR, consisting of control registers for peripheral functions such as I/O port, A/D conversion, serial I/O, and timers, is allocated addresses 000000$_{16}$ to 0003FF$_{16}$. All addresses, which have nothing allocated within SFR, are reserved space and cannot be accessed by users.

The special page vectors are allocated addresses FFFE00$_{16}$ to FFFFDB$_{16}$. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **Software Manual** for details.

In memory expansion mode and microprocessor mode, some space are reserved and cannot be accessed by users.



NOTES:
1. In memory expansion and microprocessor modes
2. In memory expansion mode. This space becomes external space in microprocessor mode.
3. This space can be used in single-chip mode and memory expansion mode. This space becomes external space in microprocessor mode.
4. Watchdog timer interrupt, oscillation stop detection interrupt, and low voltage detection interrupt share vectors.

Figure 3.1 Memory Map

4. Special Function Registers (SFR)

Address	Register	Symbol	Value after RESET
000016			
000116			
000216			
000316			
000416	Processor Mode Register 0(1)	PM0	1000 00002 (CNVss pin ="L") 0000 00112 (CNVss pin ="H")
000516	Processor Mode Register 1	PM1	0X00 00002
000616	System Clock Control Register 0	CM0	0000 X0002
000716	System Clock Control Register 1	CM1	0010 00002
000816	Wait Control Register(2)	WCR	1111 11112
000916	Address Match Interrupt Enable Register	AIER	XXXX 00002
000A16	Protect Register	PRCR	XXXX 00002
000B16	External Data Bus Width Control Register(2)	DS	XXXX 10002 (BYTE pin ="L") XXXX 00002 (BYTE pin ="H")
000C16	Main Clock Division Register	MCD	XXX0 10002
000D16	Oscillation Stop Detection Register	CM2	0016
000E16	Watchdog Timer Start Register	WDTS	XX16
000F16	Watchdog Timer Control Register	WDC	000X XXXX2
001016 001116 001216	Address Match Interrupt Register 0	RMAD0	00 00 0016
001316			
001416 001516 001616	Address Match Interrupt Register 1	RMAD1	00 00 0016
001716	VDC Control Register for PLL	PLV	XXXX XX012
001816 001916 001A16	Address Match Interrupt Register 2	RMAD2	00 00 0016
001B16	VDC Control Register 0	VDC0	0016
001C16 001D16 001E16	Address Match Interrupt Register 3	RMAD3	00 00 0016
001F16			
002016			
002116			
002216			
002316			
002416			
002516			
002616			
002716			
002816			
002916			
002A16			
002B16			
002C16			
002D16			
002E16			
002F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The PM00 and PM01 bits in the PM1 register maintain values set before reset even if software reset or watchdog timer reset is performed.
2. These registers in M32C/83T cannot be used.

Address	Register	Symbol	Value after RESET
0030₁₆			
0031₁₆			
0032₁₆			
0033₁₆			
0034₁₆			
0035₁₆			
0036₁₆			
0037₁₆			
0038₁₆			
0039₁₆			
003A₁₆			
003B₁₆			
003C₁₆			
003D₁₆			
003E₁₆			
003F₁₆			
0040₁₆	DRAM Control Register (1)	DRAMCONT	XX₁₆
0041₁₆	DRAM Refresh Interval Set Register (1)	REFCNT	XX₁₆
0042₁₆			
0043₁₆			
0044₁₆			
0045₁₆			
0046₁₆			
0047₁₆			
0048₁₆			
0049₁₆			
004A₁₆			
004B₁₆			
004C₁₆			
004D₁₆			
004E₁₆			
004F₁₆			
0050₁₆			
0051₁₆			
0052₁₆			
0053₁₆			
0054₁₆			
0055₁₆			
0056₁₆			
0057₁₆	Flash Memory Control Register 0	FMR0	XX00 0001₂
0058₁₆			
0059₁₆			
005A₁₆			
005B₁₆			
005C₁₆			
005D₁₆			
005E₁₆			
005F₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. These registers in M32C/83T cannot be used.

Address	Register	Symbol	Value after RESET
006016			
006116			
006216			
006316			
006416			
006516			
006616			
006716			
006816	DMA0 Interrupt Control Register	DM0IC	XXXX X0002
006916	Timer B5 Interrupt Control Register	TB5IC	XXXX X0002
006A16	DMA2 Interrupt Control Register	DM2IC	XXXX X0002
006B16	UART2 Receive /ACK Interrupt Control Register	S2RIC	XXXX X0002
006C16	Timer A0 Interrupt Control Register	TA0IC	XXXX X0002
006D16	UART3 Receive /ACK Interrupt Control Register	S3RIC	XXXX X0002
006E16	Timer A2 Interrupt Control Register	TA2IC	XXXX X0002
006F16	UART4 Receive /ACK Interrupt Control Register	S4RIC	XXXX X0002
007016	Timer A4 Interrupt Control Register	TA4IC	XXXX X0002
007116	UART0/UART3 Bus Conflict Detect Interrupt Control Register	BCN0IC/BCN3IC	XXXX X0002
007216	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X0002
007316	A/D0 Conversion Interrupt Control Register	AD0IC	XXXX X0002
007416	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X0002
007516	Intelligent I/O Interrupt Control Register 0	IIO0IC	XXXX X0002
007616	Timer B1 Interrupt Control Register	TB1IC	XXXX X0002
007716	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X0002
007816	Timer B3 Interrupt Control Register	TB3IC	XXXX X0002
007916	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X0002
007A16	INT5 Interrupt Control Register	INT5IC	XX00 X0002
007B16	Intelligent I/O Interrupt Control Register 6	IIO6IC	XXXX X0002
007C16	INT3 Interrupt Control Register	INT3IC	XX00 X0002
007D16	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X0002
007E16	INT1 Interrupt Control Register	INT1IC	XX00 X0002
007F16	Intelligent I/O Interrupt Control Register 10/ CAN Interrupt 1 Control Register	IIO10IC CAN1IC	XXXX X0002
008016			
008116	Intelligent I/O Interrupt Control Register 11/ CAN Interrupt 2 Control Register	IIO11IC CAN2IC	XXXX X0002
008216			
008316			
008416			
008516			
008616	A/D1 Conversion Interrupt Control Register	AD1IC	XXXX X0002
008716			
008816	DMA1 Interrupt Control Register	DM1IC	XXXX X0002
008916	UART2 Transmit /NACK Interrupt Control Register	S2TIC	XXXX X0002
008A16	DMA3 Interrupt Control Register	DM3IC	XXXX X0002
008B16	UART3 Transmit /NACK Interrupt Control Register	S3TIC	XXXX X0002
008C16	Timer A1 Interrupt Control Register	TA1IC	XXXX X0002
008D16	UART4 Transmit /NACK Interrupt Control Register	S4TIC	XXXX X0002
008E16	Timer A3 Interrupt Control Register	TA3IC	XXXX X0002
008F16	UART2 Bus Conflict Detect Interrupt Control Register	BCN2IC	XXXX X0002

X: Indeterminate

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Address	Register	Symbol	Value after RESET
009016	UART0 Transmit /NACK Interrupt Control Register	S0TIC	XXXX X0002
009116	UART1/UART4 Bus Conflict Detect Interrupt Control Register	BCN1IC/BCN4IC	XXXX X0002
009216	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X0002
009316	Key Input Interrupt Control Register	KUPIC	XXXX X0002
009416	Timer B0 Interrupt Control Register	TB0IC	XXXX X0002
009516	Intelligent I/O Interrupt Control Register 1	IIO1IC	XXXX X0002
009616	Timer B2 Interrupt Control Register	TB2IC	XXXX X0002
009716	Intelligent I/O Interrupt Control Register 3	IIO3IC	XXXX X0002
009816	Timer B4 Interrupt Control Register	TB4IC	XXXX X0002
009916	Intelligent I/O Interrupt Control Register 5	IIO5IC	XXXX X0002
009A16	INT4 Interrupt Control Register	INT4IC	XX00 X0002
009B16	Intelligent I/O Interrupt Control Register 7	IIO7IC	XXXX X0002
009C16	INT2 Interrupt Control Register	INT2IC	XX00 X0002
009D16	Intelligent I/O Interrupt Control Register 9/ CAN Interrupt 0 Control Register	IIO9IC CAN0IC	XXXX X0002
009E16	INT0 Interrupt Control Register	INT0IC	XX00 X0002
009F16	Exit Priority Control Register	RLVL	XXXX 00002
00A016	Interrupt Request Register 0	IIO0IR	0000 000X2
00A116	Interrupt Request Register 1	IIO1IR	0000 000X2
00A216	Interrupt Request Register 2	IIO2IR	0000 000X2
00A316	Interrupt Request Register 3	IIO3IR	0000 000X2
00A416	Interrupt Request Register 4	IIO4IR	0000 000X2
00A516	Interrupt Request Register 5	IIO5IR	0000 000X2
00A616	Interrupt Request Register 6	IIO6IR	0000 000X2
00A716	Interrupt Request Register 7	IIO7IR	0000 000X2
00A816	Interrupt Request Register 8	IIO8IR	0000 000X2
00A916	Interrupt Request Register 9	IIO9IR	0000 000X2
00AA16	Interrupt Request Register 10	IIO10IR	0000 000X2
00AB16	Interrupt Request Register 11	IIO11IR	0000 000X2
00AC16			
00AD16			
00AE16			
00AF16			
00B016	Interrupt Enable Register 0	IIO0IE	0016
00B116	Interrupt Enable Register 1	IIO1IE	0016
00B216	Interrupt Enable Register 2	IIO2IE	0016
00B316	Interrupt Enable Register 3	IIO3IE	0016
00B416	Interrupt Enable Register 4	IIO4IE	0016
00B516	Interrupt Enable Register 5	IIO5IE	0016
00B616	Interrupt Enable Register 6	IIO6IE	0016
00B716	Interrupt Enable Register 7	IIO7IE	0016
00B816	Interrupt Enable Register 8	IIO8IE	0016
00B916	Interrupt Enable Register 9	IIO9IE	0016
00BA16	Interrupt Enable Register 10	IIO10IE	0016
00BB16	Interrupt Enable Register 11	IIO11IE	0016
00BC16			
00BD16			
00BE16			
00BF16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00C0₁₆	Group 0 Time Measurement/Waveform Generating Register 0	G0TM0/G0PO0	XX₁₆
00C1₁₆			XX₁₆
00C2₁₆	Group 0 Time Measurement/Waveform Generating Register 1	G0TM1/G0PO1	XX₁₆
00C3₁₆			XX₁₆
00C4₁₆	Group 0 Time Measurement/Waveform Generating Register 2	G0TM2/G0PO2	XX₁₆
00C5₁₆			XX₁₆
00C6₁₆	Group 0 Time Measurement/Waveform Generating Register 3	G0TM3/G0PO3	XX₁₆
00C7₁₆			XX₁₆
00C8₁₆	Group 0 Time Measurement/Waveform Generating Register 4	G0TM4/G0PO4	XX₁₆
00C9₁₆			XX₁₆
00CA₁₆	Group 0 Time Measurement/Waveform Generating Register 5	G0TM5/G0PO5	XX₁₆
00CB₁₆			XX₁₆
00CC₁₆	Group 0 Time Measurement/Waveform Generating Register 6	G0TM6/G0PO6	XX₁₆
00CD₁₆			XX₁₆
00CE₁₆	Group 0 Time Measurement/Waveform Generating Register 7	G0TM7/G0PO7	XX₁₆
00CF₁₆			XX₁₆
00D0₁₆	Group 0 Waveform Generating Control Register 0	G0POCR0	0X00 X000₂
00D1₁₆	Group 0 Waveform Generating Control Register 1	G0POCR1	0X00 X000₂
00D2₁₆	Group 0 Waveform Generating Control Register 2	G0POCR2	0X00 X000₂
00D3₁₆	Group 0 Waveform Generating Control Register 3	G0POCR3	0X00 X000₂
00D4₁₆	Group 0 Waveform Generating Control Register 4	G0POCR4	0X00 X000₂
00D5₁₆	Group 0 Waveform Generating Control Register 5	G0POCR5	0X00 X000₂
00D6₁₆	Group 0 Waveform Generating Control Register 6	G0POCR6	0X00 X000₂
00D7₁₆	Group 0 Waveform Generating Control Register 7	G0POCR7	0X00 X000₂
00D8₁₆	Group 0 Time Measurement Control Register 0	G0TMCR0	00₁₆
00D9₁₆	Group 0 Time Measurement Control Register 1	G0TMCR1	00₁₆
00DA₁₆	Group 0 Time Measurement Control Register 2	G0TMCR2	00₁₆
00DB₁₆	Group 0 Time Measurement Control Register 3	G0TMCR3	00₁₆
00DC₁₆	Group 0 Time Measurement Control Register 4	G0TMCR4	00₁₆
00DD₁₆	Group 0 Time Measurement Control Register 5	G0TMCR5	00₁₆
00DE₁₆	Group 0 Time Measurement Control Register 6	G0TMCR6	00₁₆
00DF₁₆	Group 0 Time Measurement Control Register 7	G0TMCR7	00₁₆
00E0₁₆	Group 0 Base Timer Register	G0BT	XX₁₆
00E1₁₆			XX₁₆
00E2₁₆	Group 0 Base Timer Control Register 0	G0BCR0	00₁₆
00E3₁₆	Group 0 Base Timer Control Register 1	G0BCR1	00₁₆
00E4₁₆	Group 0 Time Measurement Prescaler Register 6	G0TPR6	00₁₆
00E5₁₆	Group 0 Time Measurement Prescaler Register 7	G0TPR7	00₁₆
00E6₁₆	Group 0 Function Enable Register	G0FE	00₁₆
00E7₁₆	Group 0 Function Select Register	G0FS	00₁₆
00E8₁₆	Group 0 SI/O Receive Buffer Register	G0RB	XXXX XXXX₂
00E9₁₆			XX00 XXXX₂
00EA₁₆	Group 0 Transmit Buffer/Receive Data Register	G0TB/G0DR	XX₁₆
00EB₁₆			
00EC₁₆	Group 0 Receive Input Register	G0RI	XX₁₆
00ED₁₆	Group 0 SI/O Communication Mode Register	G0MR	00₁₆
00EE₁₆	Group 0 Transmit Output Register	G0TO	XX₁₆
00EF₁₆	Group 0 SI/O Communication Control Register	G0CR	0000 X000₂

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Address	Register	Symbol	Value after RESET
00F016	Group 0 Data Compare Register 0	G0CMP0	XX16
00F116	Group 0 Data Compare Register 1	G0CMP1	XX16
00F216	Group 0 Data Compare Register 2	G0CMP2	XX16
00F316	Group 0 Data Compare Register 3	G0CMP3	XX16
00F416	Group 0 Data Mask Register 0	G0MSK0	XX16
00F516	Group 0 Data Mask Register 1	G0MSK1	XX16
00F616			
00F716			
00F816 00F916	Group 0 Receive CRC Code Register	G0RCRC	XX16 XX16
00FA16 00FB16	Group 0 Transmit CRC Code Register	G0TCRC	0016 0016
00FC16	Group 0 SI/O Extended Mode Register	G0EMR	0016
00FD16	Group 0 SI/O Extended Receive Control Register	G0ERC	0016
00FE16	Group 0 SI/O Special Communication Interrupt Detect Register	G0IRF	0000 00XX2
00FF16	Group 0 SI/O Extended Transmit Control Register	G0ETC	0000 0XXX2
010016 010116	Group 1 Time Measurement/Waveform Generating Register 0	G1TM0/G1PO0	XX16 XX16
010216 010316	Group 1 Time Measurement/Waveform Generating Register 1	G1TM1/G1PO1	XX16 XX16
010416 010516	Group 1 Time Measurement/Waveform Generating Register 2	G1TM2/G1PO2	XX16 XX16
010616 010716	Group 1 Time Measurement/Waveform Generating Register 3	G1TM3/G1PO3	XX16 XX16
010816 010916	Group 1 Time Measurement/Waveform Generating Register 4	G1TM4/G1PO4	XX16 XX16
010A16 010B16	Group 1 Time Measurement/Waveform Generating Register 5	G1TM5/G1PO5	XX16 XX16
010C16 010D16	Group 1 Time Measurement/Waveform Generating Register 6	G1TM6/G1PO6	XX16 XX16
010E16 010F16	Group 1 Time Measurement/Waveform Generating Register 7	G1TM7/G1PO7	XX16 XX16
011016	Group 1 Waveform Generating Control Register 0	G1POCR0	0X00 X0002
011116	Group 1 Waveform Generating Control Register 1	G1POCR1	0X00 X0002
011216	Group 1 Waveform Generating Control Register 2	G1POCR2	0X00 X0002
011316	Group 1 Waveform Generating Control Register 3	G1POCR3	0X00 X0002
011416	Group 1 Waveform Generating Control Register 4	G1POCR4	0X00 X0002
011516	Group 1 Waveform Generating Control Register 5	G1POCR5	0X00 X0002
011616	Group 1 Waveform Generating Control Register 6	G1POCR6	0X00 X0002
011716	Group 1 Waveform Generating Control Register 7	G1POCR7	0X00 X0002
011816	Group 1 Time Measurement Control Register 0	G1TMCR0	0016
011916	Group 1 Time Measurement Control Register 1	G1TMCR1	0016
011A16	Group 1 Time Measurement Control Register 2	G1TMCR2	0016
011B16	Group 1 Time Measurement Control Register 3	G1TMCR3	0016
011C16	Group 1 Time Measurement Control Register 4	G1TMCR4	0016
011D16	Group 1 Time Measurement Control Register 5	G1TMCR5	0016
011E16	Group 1 Time Measurement Control Register 6	G1TMCR6	0016
011F16	Group 1 Time Measurement Control Register 7	G1TMCR7	0016

X: Indeterminate

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Address	Register	Symbol	Value after RESET
012016 012116	Group 1 Base Timer Register	G1BT	XX16 XX16
012216	Group 1 Base Timer Control Register 0	G1BCR0	0016
012316	Group 1 Base Timer Control Register 1	G1BCR1	0016
012416	Group 1 Time Measurement Prescaler Register 6	G1TPR6	0016
012516	Group 1 Time Measurement Prescaler Register 7	G1TPR7	0016
012616	Group 1 Function Enable Register	G1FE	0016
012716	Group 1 Function Select Register	G1FS	0016
012816 012916	Group 1 SI/O Receive Buffer Register	G1RB	XXXX XXXX2 XX00 XXXX2
012A16	Group 1 Transmit Buffer/Receive Data Register	G1TB/G1DR	XX16
012B16			
012C16	Group 1 Receive Input Register	G1RI	XX16
012D16	Group 1 SI/O Communication Mode Register	G1MR	0016
012E16	Group 1 Transmit Output Register	G1TO	XX16
012F16	Group 1 SI/O Communication Control Register	G1CR	0000 X0002
013016	Group 1 Data Compare Register 0	G1CMP0	XX16
013116	Group 1 Data Compare Register 1	G1CMP1	XX16
013216	Group 1 Data Compare Register 2	G1CMP2	XX16
013316	Group 1 Data Compare Register 3	G1CMP3	XX16
013416	Group 1 Data Mask Register 0	G1MSK0	XX16
013516	Group 1 Data Mask Register 1	G1MSK1	XX16
013616			
013716			
013816 013916	Group 1 Receive CRC Code Register	G1RCRC	XX16 XX16
013A16 013B16	Group 1 Transmit CRC Code Register	G1TCRC	0016 0016
013C16	Group 1 SI/O Extended Mode Register	G1EMR	0016
013D16	Group 1 SI/O Extended Receive Control Register	G1ERC	0016
013E16	Group 1 SI/O Special Communication Interrupt Detect Register	G1IRF	0000 00XX2
013F16	Group 1 SI/O Extended Transmit Control Register	G1ETC	0000 0XXX2
014016 014116	Group 2 Waveform Generating Register 0	G2PO0	XX16 XX16
014216 014316	Group 2 Waveform Generating Register 1	G2PO1	XX16 XX16
014416 014516	Group 2 Waveform Generating Register 2	G2PO2	XX16 XX16
014616 014716	Group 2 Waveform Generating Register 3	G2PO3	XX16 XX16
014816 014916	Group 2 Waveform Generating Register 4	G2PO4	XX16 XX16
014A16 014B16	Group 2 Waveform Generating Register 5	G2PO5	XX16 XX16
014C16 014D16	Group 2 Waveform Generating Register 6	G2PO6	XX16 XX16
014E16 014F16	Group 2 Waveform Generating Register 7	G2PO7	XX16 XX16

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Address	Register	Symbol	Value after RESET
0150₁₆	Group 2 Waveform Generating Control Register 0	G2POCR0	00₁₆
0151₁₆	Group 2 Waveform Generating Control Register 1	G2POCR1	00₁₆
0152₁₆	Group 2 Waveform Generating Control Register 2	G2POCR2	00₁₆
0153₁₆	Group 2 Waveform Generating Control Register 3	G2POCR3	00₁₆
0154₁₆	Group 2 Waveform Generating Control Register 4	G2POCR4	00₁₆
0155₁₆	Group 2 Waveform Generating Control Register 5	G2POCR5	00₁₆
0156₁₆	Group 2 Waveform Generating Control Register 6	G2POCR6	00₁₆
0157₁₆	Group 2 Waveform Generating Control Register 7	G2POCR7	00₁₆
0158₁₆			
0159₁₆			
015A₁₆			
015B₁₆			
015C₁₆			
015D₁₆			
015E₁₆			
015F₁₆			
0160₁₆ 0161₁₆	Group 2 Base Timer Register	G2BT	XX₁₆ XX₁₆
0162₁₆	Group 2 Base Timer Control Register 0	G2BCR0	00₁₆
0163₁₆	Group 2 Base Timer Control Register 1	G2BCR1	00₁₆
0164₁₆	Base Timer Start Register	BTSR	XXXX 0000₂
0165₁₆			
0166₁₆	Group 2 Function Enable Register	G2FE	00₁₆
0167₁₆	Group 2 RTP Output Buffer Register	G2RTP	00₁₆
0168₁₆			
0169₁₆			
016A₁₆	Group 2 SI/O Communication Mode Register	G2MR	00XX X000₂
016B₁₆	Group 2 SI/O Communication Control Register	G2CR	0000 X000₂
016C₁₆ 016D₁₆	Group 2 SI/O Transmit Buffer Register	G2TB	XX₁₆ XX₁₆
016E₁₆ 016F₁₆	Group 2 SI/O Receive Buffer Register	G2RB	XX₁₆ XX₁₆
0170₁₆ 0171₁₆	Group 2 IEBus Address Register	IEAR	XX₁₆ XX₁₆
0172₁₆	Group 2 IEBus Control Register	IECR	00XX X000₂
0173₁₆	Group 2 IEBus Transmit Interrupt Cause Detect Register	IETIF	XXX0 0000₂
0174₁₆	Group 2 IEBus Receive Interrupt Cause Detect Register	IERIF	XXX0 0000₂
0175₁₆			
0176₁₆			
0177₁₆			
0178₁₆	Input Function Select Register	IPS	00₁₆
0179₁₆			
017A₁₆	Group 3 SI/O Communication Mode Register	G3MR	00XX 0000₂
017B₁₆	Group 3 SI/O Communication Control Register	G3CR	0000 X000₂
017C₁₆ 017D₁₆	Group 3 SI/O Transmit Buffer Register	G3TB	XX₁₆ XX₁₆
017E₁₆ 017F₁₆	Group 3 SI/O Receive Buffer Register	G3RB	XX₁₆ XX₁₆

X: Indeterminate

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Address	Register	Symbol	Value after RESET
018016 018116	Group 3 Waveform Generating Register 0	G3PO0	XX16 XX16
018216 018316	Group 3 Waveform Generating Register 1	G3PO1	XX16 XX16
018416 018516	Group 3 Waveform Generating Register 2	G3PO2	XX16 XX16
018616 018716	Group 3 Waveform Generating Register 3	G3PO3	XX16 XX16
018816 018916	Group 3 Waveform Generating Register 4	G3PO4	XX16 XX16
018A16 018B16	Group 3 Waveform Generating Register 5	G3PO5	XX16 XX16
018C16 018D16	Group 3 Waveform Generating Register 6	G3PO6	XX16 XX16
018E16 018F16	Group 3 Waveform Generating Register 7	G3PO7	XX16 XX16
019016	Group 3 Waveform Generating Control Register 0	G3POCR0	0016
019116	Group 3 Waveform Generating Control Register 1	G3POCR1	0016
019216	Group 3 Waveform Generating Control Register 2	G3POCR2	0016
019316	Group 3 Waveform Generating Control Register 3	G3POCR3	0016
019416	Group 3 Waveform Generating Control Register 4	G3POCR4	0016
019516	Group 3 Waveform Generating Control Register 5	G3POCR5	0016
019616	Group 3 Waveform Generating Control Register 6	G3POCR6	0016
019716	Group 3 Waveform Generating Control Register 7	G3POCR7	0016
019816 019916	Group 3 Waveform Generating Mask Register 4	G3MK4	XX16 XX16
019A16 019B16	Group 3 Waveform Generating Mask Register 5	G3MK5	XX16 XX16
019C16 019D16	Group 3 Waveform Generating Mask Register 6	G3MK6	XX16 XX16
019E16 019F16	Group 3 Waveform Generating Mask Register 7	G3MK7	XX16 XX16
01A016 01A116	Group 3 Base Timer Register	G3BT	XX16 XX16
01A216	Group 3 Base Timer Control Register 0	G3BCR0	0016
01A316	Group 3 Base Timer Control Register 1	G3BCR1	0016
01A416			
01A516			
01A616	Group 3 Function Enable Register	G3FE	0016
01A716	Group 3 RTP Output Buffer Register	G3RTP	0016
01A816			
01A916			
01AA16			
01AB16			
01AC16			
01AD16	Group 3 SI/O Communication Flag Register	G3FLG	XXXX XXX02
01AE16			
01AF16			

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Address	Register	Symbol	Value after RESET
01B0₁₆			
01B1₁₆			
01B2₁₆			
01B3₁₆			
01B4₁₆			
01B5₁₆			
01B6₁₆			
01B7₁₆			
01B8₁₆			
01B9₁₆			
01BA₁₆			
01BB₁₆			
01BC₁₆			
01BD₁₆			
01BE₁₆			
01BF₁₆			
01C0₁₆ 01C1₁₆	A/D1 Register 0	AD10	XX₁₆ XX₁₆
01C2₁₆ 01C3₁₆	A/D1 Register 1	AD11	XX₁₆ XX₁₆
01C4₁₆ 01C5₁₆	A/D1 Register 2	AD12	XX₁₆ XX₁₆
01C6₁₆ 01C7₁₆	A/D1 Register 3	AD13	XX₁₆ XX₁₆
01C8₁₆ 01C9₁₆	A/D1 Register 4	AD14	XX₁₆ XX₁₆
01CA₁₆ 01CB₁₆	A/D1 Register 5	AD15	XX₁₆ XX₁₆
01CC₁₆ 01CD₁₆	A/D1 Register 6	AD16	XX₁₆ XX₁₆
01CE₁₆ 01CF₁₆	A/D1 Register 7	AD17	XX₁₆ XX₁₆
01D0₁₆			
01D1₁₆			
01D2₁₆			
01D3₁₆			
01D4₁₆	A/D1 Control Register 2	AD1CON2	X00X X000₂
01D5₁₆			
01D6₁₆	A/D1 Control Register 0	AD1CON0	00₁₆
01D7₁₆	A/D1 Control Register 1	AD1CON1	XX00 0000₂
01D8₁₆			
01D9₁₆			
01DA₁₆			
01DB₁₆			
01DC₁₆			
01DD₁₆			
01DE₁₆			
01DF₁₆			

X: Indeterminate

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Address	Register	Symbol	Value after RESET
01E016	CAN0 Message Slot Buffer 0 Standard ID0	C0SLOT0_0	XX16
01E116	CAN0 Message Slot Buffer 0 Standard ID1	C0SLOT0_1	XX16
01E216	CAN0 Message Slot Buffer 0 Extended ID0	C0SLOT0_2	XX16
01E316	CAN0 Message Slot Buffer 0 Extended ID1	C0SLOT0_3	XX16
01E416	CAN0 Message Slot Buffer 0 Extended ID2	C0SLOT0_4	XX16
01E516	CAN0 Message Slot Buffer 0 Data Length Code	C0SLOT0_5	XX16
01E616	CAN0 Message Slot Buffer 0 Data 0	C0SLOT0_6	XX16
01E716	CAN0 Message Slot Buffer 0 Data 1	C0SLOT0_7	XX16
01E816	CAN0 Message Slot Buffer 0 Data 2	C0SLOT0_8	XX16
01E916	CAN0 Message Slot Buffer 0 Data 3	C0SLOT0_9	XX16
01EA16	CAN0 Message Slot Buffer 0 Data 4	C0SLOT0_10	XX16
01EB16	CAN0 Message Slot Buffer 0 Data 5	C0SLOT0_11	XX16
01EC16	CAN0 Message Slot Buffer 0 Data 6	C0SLOT0_12	XX16
01ED16	CAN0 Message Slot Buffer 0 Data 7	C0SLOT0_13	XX16
01EE16	CAN0 Message Slot Buffer 0 Time Stamp High-Order	C0SLOT0_14	XX16
01EF16	CAN0 Message Slot Buffer 0 Time Stamp Low-Order	C0SLOT0_15	XX16
01F016	CAN0 Message Slot Buffer 1 Standard ID0	C0SLOT1_0	XX16
01F116	CAN0 Message Slot Buffer 1 Standard ID1	C0SLOT1_1	XX16
01F216	CAN0 Message Slot Buffer 1 Extended ID0	C0SLOT1_2	XX16
01F316	CAN0 Message Slot Buffer 1 Extended ID1	C0SLOT1_3	XX16
01F416	CAN0 Message Slot Buffer 1 Extended ID2	C0SLOT1_4	XX16
01F516	CAN0 Message Slot Buffer 1 Data Length Code	C0SLOT1_5	XX16
01F616	CAN0 Message Slot Buffer 1 Data 0	C0SLOT1_6	XX16
01F716	CAN0 Message Slot Buffer 1 Data 1	C0SLOT1_7	XX16
01F816	CAN0 Message Slot Buffer 1 Data 2	C0SLOT1_8	XX16
01F916	CAN0 Message Slot Buffer 1 Data 3	C0SLOT1_9	XX16
01FA16	CAN0 Message Slot Buffer 1 Data 4	C0SLOT1_10	XX16
01FB16	CAN0 Message Slot Buffer 1 Data 5	C0SLOT1_11	XX16
01FC16	CAN0 Message Slot Buffer 1 Data 6	C0SLOT1_12	XX16
01FD16	CAN0 Message Slot Buffer 1 Data 7	C0SLOT1_13	XX16
01FE16	CAN0 Message Slot Buffer 1 Time Stamp High-Order	C0SLOT1_14	XX16
01FF16	CAN0 Message Slot Buffer 1 Time Stamp Low-Order	C0SLOT1_15	XX16
020016 020116	CAN0 Control Register 0	C0CTLR0	XX01 0X012(1) XXXX 00002(1)
020216 020316	CAN0 Status Register	C0STR	0000 00002(1) X000 0X012(1)
020416 020516	CAN0 Extended ID Register	C0IDR	0016(1) 0016(1)
020616 020716	CAN0 Configuration Register	C0CONR	0000 XXXX2(1) 0000 00002(1)
020816 020916	CAN0 Time Stamp Register	C0TSR	0016(1) 0016(1)
020A16	CAN0 Transmit Error Count Register	C0TEC	0016(1)
020B16	CAN0 Receive Error Count Register	C0REC	0016(1)
020C16 020D16	CAN0 Slot Interrupt Status Register	C0SISTR	0016(1) 0016(1)
020E16			
020F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
0210$_{16}$ 0211$_{16}$	CAN0 Slot Interrupt Mask Register	C0SIMKR	00$_{16}$(2) 00$_{16}$(2)
0212$_{16}$			
0213$_{16}$			
0214$_{16}$	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X000$_2$(2)
0215$_{16}$	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X000$_2$(2)
0216$_{16}$			
0217$_{16}$	CAN0 Baud Rate Prescaler	C0BRP	0000 0001$_2$(2)
0218$_{16}$			
0219$_{16}$			
021A$_{16}$			
021B$_{16}$			
021C$_{16}$			
021D$_{16}$			
021E$_{16}$			
021F$_{16}$			
0220$_{16}$			
0221$_{16}$			
0222$_{16}$			
0223$_{16}$			
0224$_{16}$			
0225$_{16}$			
0226$_{16}$			
0227$_{16}$			
0228$_{16}$	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 0000$_2$(2)
0229$_{16}$	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 0000$_2$(2)
022A$_{16}$	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 0000$_2$(2)
022B$_{16}$	CAN0 Global Mask Register Extended ID1	C0GMR3	00$_{16}$(2)
022C$_{16}$	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 0000$_2$(2)
022D$_{16}$			
022E$_{16}$			
022F$_{16}$			
0230$_{16}$	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0/ C0LMAR0	0000 0000$_2$(2) XXX0 0000$_2$(2)
0231$_{16}$	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1/ C0LMAR1	0000 0000$_2$(2) XX00 0000$_2$(2)
0232$_{16}$	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2/ C0LMAR2	0000 0000$_2$(2) XXXX 0000$_2$(2)
0233$_{16}$	CAN0 Message Slot 3 Control Register / CAN0 Local Mask Register A Extended ID1	C0MCTL3/ C0LMAR3	00$_{16}$(2) 00$_{16}$(2)
0234$_{16}$	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4/ C0LMAR4	0000 0000$_2$(2) XX00 0000$_2$(2)
0235$_{16}$	CAN0 Message Slot 5 Control Register	C0MCTL5	00$_{16}$(2)
0236$_{16}$	CAN0 Message Slot 6 Control Register	C0MCTL6	00$_{16}$(2)
0237$_{16}$	CAN0 Message Slot 7 Control Register	C0MCTL7	00$_{16}$(2)
0238$_{16}$	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8/ C0LMBR0	0000 0000$_2$(2) XXX0 0000$_2$(2)

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220$_{16}$ to 023F$_{16}$.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
023916	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9/ C0LMBR1	0000 00002(2) XX00 00002(2)
023A16	CAN0 Message Slot 10 Control Register / CAN0 Local Mask Register B Extended ID0	C0MCTL10/ C0LMBR2	0000 00002(2) XXXX 00002(2)
023B16	CAN0 Message Slot 11 Control Register / CAN0 Local Mask Register B Extended ID1	C0MCTL11/ C0LMBR3	0016(2) 0016(2)
023C16	CAN0 Message Slot 12 Control Register / CAN0 Local Mask Register B Extended ID2	C0MCTL12/ C0LMBR4	0000 00002(2) XX00 00002(2)
023D16	CAN0 Message Slot 13 Control Register	C0MCTL13	0016(2)
023E16	CAN0 Message Slot 14 Control Register	C0MCTL14	0016(2)
023F16	CAN0 Message Slot 15 Control Register	C0MCTL15	0016(2)
024016	CAN0 Slot Buffer Select Register	C0SBS	0016(2)
024116	CAN0 Control Register 1	C0CTLR1	XX00 00XX2(2)
024216	CAN0 Sleep Control Register	C0SLPR	XXXX XXX02
024316			
024416	CAN0 Acceptance Filter Support Register	C0AFS	0016(2)
024516			0116(2)
024616			
024716			
024816			
024916			
024A16			
024B16			
024C16			
024D16			
024E16			
024F16			
025016			
025116			
025216			
025316			
025416			
025516			
025616			
025716			
025816			
025916			
025A16			
025B16			
025C16			
025D16			
025E16			
025F16			
026016			
026116 to 02BF16			

(Note 1)

X: Indeterminate

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NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 022016 to 023F16.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
02C0₁₆ 02C1₁₆	X0 Register Y0 Register	X0R,Y0R	XX₁₆ XX₁₆
02C2₁₆ 02C3₁₆	X1 Register Y1 Register	X1R,Y1R	XX₁₆ XX₁₆
02C4₁₆ 02C5₁₆	X2 Register Y2 Register	X2R,Y2R	XX₁₆ XX₁₆
02C6₁₆ 02C7₁₆	X3 Register Y3 Register	X3R,Y3R	XX₁₆ XX₁₆
02C8₁₆ 02C9₁₆	X4 Register Y4 Register	X4R,Y4R	XX₁₆ XX₁₆
02CA₁₆ 02CB₁₆	X5 Register Y5 Register	X5R,Y5R	XX₁₆ XX₁₆
02CC₁₆ 02CD₁₆	X6 Register Y6 Register	X6R,Y6R	XX₁₆ XX₁₆
02CE₁₆ 02CF₁₆	X7 Register Y7 Register	X7R,Y7R	XX₁₆ XX₁₆
02D0₁₆ 02D1₁₆	X8 Register Y8 Register	X8R,Y8R	XX₁₆ XX₁₆
02D2₁₆ 02D3₁₆	X9 Register Y9 Register	X9R,Y9R	XX₁₆ XX₁₆
02D4₁₆ 02D5₁₆	X10 Register Y10 Register	X10R,Y10R	XX₁₆ XX₁₆
02D6₁₆ 02D7₁₆	X11 Register Y11 Register	X11R,Y11R	XX₁₆ XX₁₆
02D8₁₆ 02D9₁₆	X12 Register Y12 Register	X12R,Y12R	XX₁₆ XX₁₆
02DA₁₆ 02DB₁₆	X13 Register Y13 Register	X13R,Y13R	XX₁₆ XX₁₆
02DC₁₆ 02DD₁₆	X14 Register Y14 Register	X14R,Y14R	XX₁₆ XX₁₆
02DE₁₆ 02DF₁₆	X15 Register Y15 Register	X15R,Y15R	XX₁₆ XX₁₆
02E0₁₆	XY Control Register	XYC	XXXX XX00₂
02E1₁₆			
02E2₁₆			
02E3₁₆			
02E4₁₆	UART1 Special Mode Register 4	U1SMR4	00₁₆
02E5₁₆	UART1 Special Mode Register 3	U1SMR3	00₁₆
02E6₁₆	UART1 Special Mode Register 2	U1SMR2	00₁₆
02E7₁₆	UART1 Special Mode Register	U1SMR	00₁₆
02E8₁₆	UART1 Transmit/Receive Mode Register	U1MR	00₁₆
02E9₁₆	UART1 Baud Rate Register	U1BRG	XX₁₆
02EA₁₆ 02EB₁₆	UART1 Transmit Buffer Register	U1TB	XX₁₆ XX₁₆
02EC₁₆	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000₂
02ED₁₆	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010₂
02EE₁₆ 02EF₁₆	UART1 Receive Buffer Register	U1RB	XX₁₆ XX₁₆

X: Indeterminate

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Address	Register	Symbol	Value after RESET
02F0₁₆			
02F1₁₆			
02F2₁₆			
02F3₁₆			
02F4₁₆	UART4 Special Mode Register 4	U4SMR4	00₁₆
02F5₁₆	UART4 Special Mode Register 3	U4SMR3	00₁₆
02F6₁₆	UART4 Special Mode Register 2	U4SMR2	00₁₆
02F7₁₆	UART4 Special Mode Register	U4SMR	00₁₆
02F8₁₆	UART4 Transmit/Receive Mode Register	U4MR	00₁₆
02F9₁₆	UART4 Baud Rate Register	U4BRG	XX₁₆
02FA₁₆ 02FB₁₆	UART4 Transmit Buffer Register	U4TB	XX₁₆ XX₁₆
02FC₁₆	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000₂
02FD₁₆	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010₂
02FE₁₆ 02FF₁₆	UART4 Receive Buffer Register	U4RB	XX₁₆ XX₁₆
0300₁₆	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX₂
0301₁₆			
0302₁₆ 0303₁₆	Timer A1-1 Register	TA11	XX₁₆ XX₁₆
0304₁₆ 0305₁₆	Timer A2-1 Register	TA21	XX₁₆ XX₁₆
0306₁₆ 0307₁₆	Timer A4-1 Register	TA41	XX₁₆ XX₁₆
0308₁₆	Three-Phase PWM Control Register 0	INVC0	00₁₆
0309₁₆	Three-Phase PWM Control Register 1	INVC1	00₁₆
030A₁₆	Three-Phase output Buffer Register 0	IDB0	XX11 1111₂
030B₁₆	Three-Phase output Buffer Register 1	IDB1	XX11 1111₂
030C₁₆	Dead Time Timer	DTT	XX₁₆
030D₁₆	Timer B2 Interrupt Generating Frequency Set Counter	ICTB2	XX₁₆
030E₁₆			
030F₁₆			
0310₁₆ 0311₁₆	Timer B3 Register	TB3	XX₁₆ XX₁₆
0312₁₆ 0313₁₆	Timer B4 Register	TB4	XX₁₆ XX₁₆
0314₁₆ 0315₁₆	Timer B5 Register	TB5	XX₁₆ XX₁₆
0316₁₆			
0317₁₆			
0318₁₆			
0319₁₆			
031A₁₆			
031B₁₆	Timer B3 Mode Register	TB3MR	00XX 0000₂
031C₁₆	Timer B4 Mode Register	TB4MR	00XX 0000₂
031D₁₆	Timer B5 Mode Register	TB5MR	00XX 0000₂
031E₁₆			
031F₁₆	External Interrupt Cause Select Register	IFSR	00₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
032016			
032116			
032216			
032316			
032416	UART3 Special Mode Register 4	U3SMR4	0016
032516	UART3 Special Mode Register 3	U3SMR3	0016
032616	UART3 Special Mode Register 2	U3SMR2	0016
032716	UART3 Special Mode Register	U3SMR	0016
032816	UART3 Transmit/Receive Mode Register	U3MR	0016
032916	UART3 Baud Rate Register	U3BRG	XX16
032A16 032B16	UART3 Transmit Buffer Register	U3TB	XX16 XX16
032C16	UART3 Transmit/Receive Control Register 0	U3C0	0000 10002
032D16	UART3 Transmit/Receive Control Register 1	U3C1	0000 00102
032E16 032F16	UART3 Receive Buffer Register	U3RB	XX16 XX16
033016			
033116			
033216			
033316			
033416	UART2 Special Mode Register 4	U2SMR4	0016
033516	UART2 Special Mode Register 3	U2SMR3	0016
033616	UART2 Special Mode Register 2	U2SMR2	0016
033716	UART2 Special Mode Register	U2SMR	0016
033816	UART2 Transmit/Receive Mode Register	U2MR	0016
033916	UART2 Baud Rate Register	U2BRG	XX16
033A16 033B16	UART2 Transmit Buffer Register	U2TB	XX16 XX16
033C16	UART2 Transmit/Receive Control Register 0	U2C0	0000 10002
033D16	UART2 Transmit/Receive Control Register 1	U2C1	0000 00102
033E16 033F16	UART2 Receive Buffer Register	U2RB	XX16 XX16
034016	Count Start Flag	TABSR	0016
034116	Clock Prescaler Reset Flag	CPSRF	0XXX XXXX2
034216	One-Shot Start Flag	ONSF	0016
034316	Trigger Select Register	TRGSR	0016
034416	Up-Down Flag	UDF	0016
034516			
034616 034716	Timer A0 Register	TA0	XX16 XX16
034816 034916	Timer A1 Register	TA1	XX16 XX16
034A16 034B16	Timer A2 Register	TA2	XX16 XX16
034C16 034D16	Timer A3 Register	TA3	XX16 XX16
034E16 034F16	Timer A4 Register	TA4	XX16 XX16

X: Indeterminate

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Address	Register	Symbol	Value after RESET
035016	Timer B0 Register	TB0	XX16
035116			XX16
035216	Timer B1 Register	TB1	XX16
035316			XX16
035416	Timer B2 Register	TB2	XX16
035516			XX16
035616	Timer A0 Mode Register	TA0MR	0000 0X002
035716	Timer A1 Mode Register	TA1MR	0000 0X002
035816	Timer A2 Mode Register	TA2MR	0000 0X002
035916	Timer A3 Mode Register	TA3MR	0000 0X002
035A16	Timer A4 Mode Register	TA4MR	0000 0X002
035B16	Timer B0 Mode Register	TB0MR	00XX 00002
035C16	Timer B1 Mode register	TB1MR	00XX 00002
035D16	Timer B2 Mode Register	TB2MR	00XX 00002
035E16	Timer B2 Special Mode Register	TB2SC	XXXX XXX02
035F16	Count Source Prescaler Register(1)	TCSPR	0XXX 00002
036016			
036116			
036216			
036316			
036416	UART0 Special Mode Register 4	U0SMR4	0016
036516	UART0 Special Mode Register 3	U0SMR3	0016
036616	UART0 Special Mode Register 2	U0SMR2	0016
036716	UART0 Special Mode Register	U0SMR	0016
036816	UART0 Transmit/Receive Mode Register	U0MR	0016
036916	UART0 Baud Rate Register	U0BRG	XX16
036A16	UART0 Transmit Buffer Register	U0TB	XX16
036B16			XX16
036C16	UART0 Transmit/Receive Control Register 0	U0C0	0000 10002
036D16	UART0 Transmit/Receive Control Register 1	U0C1	0000 00102
036E16	UART0 Receive Buffer Register	U0RB	XX16
036F16			XX16
037016			
037116			
037216			
037316			
037416			
037516			
037616	PLL Control Register 0	PLC0	0011 X1002
037716	PLL Control Register 1	PLC1	XXXX 00002
037816	DMA0 Cause Select Register	DM0SL	0X00 00002
037916	DMA1 Cause Select Register	DM1SL	0X00 00002
037A16	DMA2 Cause Select Register	DM2SL	0X00 00002
037B16	DMA3 Cause Select Register	DM3SL	0X00 00002
037C16	CRC Data Register	CRCD	XX16
037D16			XX16
037E16	CRC Input Register	CRCIN	XX16
037F16			

X: Indeterminate

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NOTES:

1. The TCSPR register maintains the values set before reset even if software reset or watchdog timer reset is performed.

Address	Register	Symbol	Value after RESET
038016 038116	A/D0 Register 0	AD00	XX16 XX16
038216 038316	A/D0 Register 1	AD01	XX16 XX16
038416 038516	A/D0 Register 2	AD02	XX16 XX16
038616 038716	A/D0 Register 3	AD03	XX16 XX16
038816 038916	A/D0 Register 4	AD04	XX16 XX16
038A16 038B16	A/D0 Register 5	AD05	XX16 XX16
038C16 038D16	A/D0 Register 6	AD06	XX16 XX16
038E16 038F16	A/D0 Register 7	AD07	XX16 XX16
039016			
039116			
039216			
039316			
039416	A/D0 Control Register 2	AD0CON2	X000 00002
039516			
039616	A/D0 Control Register 0	AD0CON0	0016
039716	A/D0 Control Register 1	AD0CON1	0016
039816	D/A Register 0	DA0	XX16
039916			
039A16	D/A Register 1	DA1	XX16
039B16			
039C16	D/A Control Register	DACON	XXXX XX002
039D16			
039E16			
039F16			

X: Indeterminate

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<144-pin package>

Address	Register	Symbol	Value after RESET
03A0₁₆	Function Select Register A8	PS8	X000 0000₂
03A1₁₆	Function Select Register A9	PS9	00₁₆
03A2₁₆			
03A3₁₆			
03A4₁₆			
03A5₁₆			
03A6₁₆			
03A7₁₆			
03A8₁₆			
03A9₁₆			
03AA₁₆			
03AB₁₆			
03AC₁₆			
03AD₁₆			
03AE₁₆			
03AF₁₆	Function Select Register C	PSC	00X0 0000₂
03B0₁₆	Function Select Register A0	PS0	00₁₆
03B1₁₆	Function Select Register A1	PS1	00₁₆
03B2₁₆	Function Select Register B0	PSL0	00₁₆
03B3₁₆	Function Select Register B1	PSL1	00₁₆
03B4₁₆	Function Select Register A2	PS2	00X0 0000₂
03B5₁₆	Function Select Register A3	PS3	00₁₆
03B6₁₆	Function Select Register B2	PSL2	00X0 0000₂
03B7₁₆	Function Select Register B3	PSL3	00₁₆
03B8₁₆			
03B9₁₆	Function Select Register A5	PS5	XXX0 0000₂
03BA₁₆			
03BB₁₆			
03BC₁₆	Function Select Register A6	PS6	00₁₆
03BD₁₆	Function Select Register A7	PS7	00₁₆
03BE₁₆			
03BF₁₆			
03C0₁₆	Port P6 Register	P6	XX₁₆
03C1₁₆	Port P7 Register	P7	XX₁₆
03C2₁₆	Port P6 Direction Register	PD6	00₁₆
03C3₁₆	Port P7 Direction Register	PD7	00₁₆
03C4₁₆	Port P8 Register	P8	XX₁₆
03C5₁₆	Port P9 Register	P9	XX₁₆
03C6₁₆	Port P8 Direction Register	PD8	00X0 0000₂
03C7₁₆	Port P9 Direction Register	PD9	00₁₆
03C8₁₆	Port P10 Register	P10	XX₁₆
03C9₁₆	Port P11 Register	P11	XX₁₆
03CA₁₆	Port P10 Direction Register	PD10	00₁₆
03CB₁₆	Port P11 Direction Register	PD11	XXX0 0000₂
03CC₁₆	Port P12 Register	P12	XX₁₆
03CD₁₆	Port P13 Register	P13	XX₁₆
03CE₁₆	Port P12 Direction Register	PD12	00₁₆
03CF₁₆	Port P13 Direction Register	PD13	00₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<144-pin package>

Address	Register	Symbol	Value after RESET
03D0$_{16}$	Port P14 Register	P14	XX$_{16}$
03D1$_{16}$	Port P15 Register	P15	XX$_{16}$
03D2$_{16}$	Port P14 Direction Register	PD14	X000 0000$_2$
03D3$_{16}$	Port P15 Direction Register	PD15	00$_{16}$
03D4$_{16}$			
03D5$_{16}$			
03D6$_{16}$			
03D7$_{16}$			
03D8$_{16}$			
03D9$_{16}$			
03DA$_{16}$	Pull-Up Control Register 2	PUR2	00$_{16}$
03DB$_{16}$	Pull-Up Control Register 3	PUR3	00$_{16}$
03DC$_{16}$	Pull-Up Control Register 4	PUR4	XXXX 0000$_2$
03DD$_{16}$			
03DE$_{16}$			
03DF$_{16}$			
03E0$_{16}$	Port P0 Register	P0	XX$_{16}$
03E1$_{16}$	Port P1 Register	P1	XX$_{16}$
03E2$_{16}$	Port P0 Direction Register	PD0	00$_{16}$
03E3$_{16}$	Port P1 Direction Register	PD1	00$_{16}$
03E4$_{16}$	Port P2 Register	P2	XX$_{16}$
03E5$_{16}$	Port P3 Register	P3	XX$_{16}$
03E6$_{16}$	Port P2 Direction Register	PD2	00$_{16}$
03E7$_{16}$	Port P3 Direction Register	PD3	00$_{16}$
03E8$_{16}$	Port P4 Register	P4	XX$_{16}$
03E9$_{16}$	Port P5 Register	P5	XX$_{16}$
03EA$_{16}$	Port P4 Direction Register	PD4	00$_{16}$
03EB$_{16}$	Port P5 Direction Register	PD5	00$_{16}$
03EC$_{16}$			
03ED$_{16}$			
03EE$_{16}$			
03EF$_{16}$			
03F0$_{16}$	Pull-Up Control Register 0	PUR0	00$_{16}$
03F1$_{16}$	Pull-Up Control Register 1	PUR1	XXXX 0000$_2$
03F2$_{16}$			
03F3$_{16}$			
03F4$_{16}$			
03F5$_{16}$			
03F6$_{16}$			
03F7$_{16}$			
03F8$_{16}$			
03F9$_{16}$			
03FA$_{16}$			
03FB$_{16}$			
03FC$_{16}$			
03FD$_{16}$			
03FE$_{16}$			
03FF$_{16}$	Port Control Register	PCR	XXXX XXX0$_2$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<100-pin package>

Address	Register	Symbol	Value after RESET	
03A016				(Note 2)
03A116				
03A216				
03A316				
03A416				
03A516				
03A616				
03A716				
03A816				
03A916				
03AA16				
03AB16				
03AC16				
03AD16				
03AE16				
03AF16	Function Select Register C	PSC	0X00 00002	
03B016	Function Select Register A0	PS0	0016	
03B116	Function Select Register A1	PS1	0016	
03B216	Function Select Register B0	PSL0	0016	
03B316	Function Select Register B1	PSL1	0016	
03B416	Function Select Register A2	PS2	00X0 00002	
03B516	Function Select Register A3	PS3	0016	
03B616	Function Select Register B2	PSL2	00X0 00002	
03B716	Function Select Register B3	PSL3	0016	
03B816				
03B916				(Note 2)
03BA16				
03BB16				
03BC16				(Note 2)
03BD16				
03BE16				
03BF16				
03C016	Port P6 Register	P6	XX16	
03C116	Port P7 Register	P7	XX16	
03C216	Port P6 Direction Register	PD6	0016	
03C316	Port P7 Direction Register	PD7	0016	
03C416	Port P8 Register	P8	XX16	
03C516	Port P9 Register	P9	XX16	
03C616	Port P8 Direction Register	PD8	00X0 00002	
03C716	Port P9 Direction Register	PD9	0016	
03C816	Port P10 Register	P10	XX16	
03C916				(Note 2)
03CA16	Port P10 Direction Register	PD10	0016	
03CB16				(Note 1)
03CC16				(Note 2)
03CD16				
03CE16				(Note 1)
03CF16				

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Set address spaces 03CB16, 03CE16 and 03CF16 to "FF16" in the 100-pin package.
2. Address spaces 03A016, 03A116, 03B916, 03BC16, 03BD16, 03C916, 03CC16 and 03CD16 are not provided in the 100-pin package.

<100-pin package>

Address	Register	Symbol	Value after RESET	
03D016				(Note 3)
03D116				
03D216				(Note 1)
03D316				
03D416				
03D516				
03D616				
03D716				
03D816				
03D916				
03DA16	Pull-up Control Register 2	PUR2	0016	
03DB16	Pull-up Control Register 3	PUR3	0016	
03DC16				(Note 2)
03DD16				
03DE16				
03DF16				
03E016	Port P0 Register	P0	XX16	
03E116	Port P1 Register	P1	XX16	
03E216	Port P0 Direction Register	PD0	0016	
03E316	Port P1 Direction Register	PD1	0016	
03E416	Port P2 Register	P2	XX16	
03E516	Port P3 Register	P3	XX16	
03E616	Port P2 Direction Register	PD2	0016	
03E716	Port P3 Direction Register	PD3	0016	
03E816	Port P4 Register	P4	XX16	
03E916	Port P5 Register	P5	XX16	
03EA16	Port P4 Direction Register	PD4	0016	
03EB16	Port P5 Direction Register	PD5	0016	
03EC16				
03ED16				
03EE16				
03EF16				
03F016	Pull-Up Control Register 0	PUR0	0016	
03F116	Pull-Up Control Register 1	PUR1	XXXX 00002	
03F216				
03F316				
03F416				
03F516				
03F616				
03F716				
03F816				
03F916				
03FA16				
03FB16				
03FC16				
03FD16				
03FE16				
03FF16	Port Control Register	PCR	XXXX XXX02	

X: Indeterminate
Blank spaces are reserved. No access is allowed.

NOTES:

1. Set address spaces 03D216 and 03D316 to "FF16" in the 100-pin package.
2. Set address spaces 03DC16 to "0016" in the 100-pin package.
3. Address spaces 03D016 and 03D116 are not provided in the 100-pin package.

5. Electrical Characteristics

5.1 Electrical Characteristics (M32C/83)

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
V_{CC}	Supply Voltage		V_{CC}=AV_{CC}	-0.3 to 6.0	V
AV_{CC}	Analog Supply Voltage		V_{CC}=AV_{CC}	-0.3 to 6.0	V
V_I	Input Voltage	$\overline{RESET}$, CNV_{SS}, BYTE, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), V_{REF}, X_{IN}		-0.3 to V_{CC}+0.3	V
		$P7_0$, $P7_1$		-0.3 to 6.0	V
V_O	Output Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{OUT}		-0.3 to V_{CC}+0.3	V
Pd	Power Dissipation		Topr=25° C	500	mW
Topr	Operating Ambient Temperature			-20 to 85	° C
Tstg	Storage Temperature			-65 to 150	° C

NOTES:
1. P11 to P15 are provided in the 144-pin package.

Table 5.2 Recommended Operating Conditions (V_{CC} = 3.0V to 5.5V at Topr = – 20 to 85°C)

Symbol	Parameter			Standard			Unit
				Min	Typ	Max	
V_{CC}	Supply Voltage (Through VDC)			3.0	5.0	5.5	V
	Supply Voltage (Not through VDC)			3.0	3.3	3.6	V
AV_{CC}	Analog Supply Voltage				V_{CC}		V
V_{SS}	Supply Voltage				0		V
AV_{SS}	Analog Supply Voltage				0		V
V_{IH}	Input High ("H") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE		0.8V_{CC}		V_{CC}	V
		$P7_0$, $P7_1$		0.8V_{CC}		6.0	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in single-chip mode)		0.8V_{CC}		V_{CC}	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in memory expansion mode and microprocesor mode)		0.5V_{CC}		V_{CC}	V
V_{IL}	Input Low ("L") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE		0		0.2V_{CC}	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in single-chip mode)		0		0.2V_{CC}	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in memory expansion mode and microprocesor mode)		0		0.16V_{CC}	V
$I_{OH(peak)}$	Peak Output High ("H") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)				-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)				-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)				10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)				5.0	mA
$f(X_{IN})$	Main Clock Input Frequency	Through VDC	V_{CC}=4.2 to 5.5V	0		32	MHz
			V_{CC}=3.0 to 4.3V	0		20	MHz
		Not through VDC	V_{CC}=3.0 to 3.6	0		20	MHz
$f(X_{CIN})$	Sub Clock Oscillation Frequency				32.768	50	kHz

NOTES:

1. Typical values when average output current is 100ms.
2. Total $I_{OL(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be 80mA or less.
   Total $I_{OH(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be -80mA or less.
   Total $I_{OL(peak)}$ for P3, P4, P5, P6, P7, $P8_0$ to $P8_4$, P12 and P13 must be 80mA or less.
   Total $I_{OH(peak)}$ for P3, P4, P5, P6, $P7_2$ to $P7_7$, $P8_0$ to $P8_4$, P12 and P13 must be -80mA or less.
3. V_{IH} and V_{IL} reference for $P8_7$ applies when $P8_7$ is used as a programmable input port.
   It does not apply to $P8_7$ used as X_{CIN}.
4. P11 to P15 are provided in the 144-pin package only.

V_{CC}=5V

Table 5.3 Electrical Characteristics (V_{CC}=4.2 to 5.5V, V_{SS}=0V at Topr= –20 to 85°C, f(X_{IN})=32MHz unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit
				Min	Typ	Max	
V_{OH}	Output High ("H") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OH}=-5mA	Vcc - 2.0			V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OH}=-200µA	Vcc - 0.3			V
		X_{OUT}	I_{OH}=-1mA	3.0			V
		X_{COUT}	No load applied		3.3		V
V_{OL}	Output Low ("L") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=5mA			2.0	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=200µA			0.45	V
		X_{OUT}	I_{OL}=1mA			2.0	V
		X_{COUT}	No load applied		0		V
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$-$TA4_{IN}$, $TB0_{IN}$-$TB5_{IN}$, $\overline{INT0}$-$\overline{INT5}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, $TA0_{OUT}$-$TA4_{OUT}$, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		$\overline{RESET}$		0.2		1.8	V
I_{IH}	Input High ("H") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=5V			5.0	µA
I_{IL}	Input Low ("L") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=0V			-5.0	µA
R_{PULLUP}	Pull-up Resistance	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	V_I=0V	30	50	167	kΩ
Rf_{XIN}	Feedback Resistance	X_{IN}			1.5		MΩ
Rf_{XCIN}	Feedback Resistance	X_{CIN}			10		MΩ
V_{RAM}	RAM Standby Voltage	Through VDC		2.5			V
I_{CC}	Power Supply Current	Measurement conditions: In single-chip mode, output pins are left open and other pins are connected to V_{SS}.	f(X_{IN})=32 MHz, square wave, no division		40	54	mA
			f(X_{CIN})=32 kHz, with a wait state, Topr=25° C		470		µA
			Topr=25° C when the clock stops		0.4	20	µA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

VCC=5V

Table 5.4 A/D Conversion Characteristics (VCC = AVCC = VREF = 4.2 to 5.5V, Vss = AVSS = 0V at Topr = –20 to 85°C, f(XIN) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min	Typ	Max	
-	Resolution	VREF=VCC				10	Bits
INL	Integral Nonlinearity Error	VREF=VCC=5V	AN0 to AN7 ANEX0, ANEX1			±3	LSB LSB
			External op-amp connection mode			±7	LSB LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
RLADDER	Resistor Ladder	VREF=VCC		8		40	kΩ
tCONV	10-bit Conversion Time			2.1			µs
tCONV	8-bit Conversion Time			1.8			µs
tSAMP	Sample Time			0.2			µs
VREF	Reference Voltage			2		VCC	V
VIA	Analog Input Voltage			0		VREF	V

NOTES:
1. Divide f(XIN), if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.

Table 5.5 D/A Conversion Characteristics (VCC = VREF = 4.2 to 5.5V, VSS = AVSS = 0V at Topr = –20 to 85°C, f(XIN) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
tSU	Setup Time				3	µs
RO	Output Resistance		4	10	20	kΩ
IVREF	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:
1. Measurement results when using one D/A converter. The DAi register (i=0, 1) of the D/A converter not being used is set to "00$_{16}$". The resistor ladder in the A/D converter is exclued. IVREF flows even if the VCUT bit in the ADiCON1 register is set to "0" (no VREF connection).

Table 5.6 Flash Memory Version Electrical Characteristics

Parameter	Standard			Unit
	Min	Typ	Max	
Program Time (per page)		8	120	ms
Block Erase Time (per block)		50	600	ms

NOTES:
1. VCC= 4.2 to 5.5V (through VDC), 3.0 to 3.6V (not through VDC) at Topr= 0 to 60° C, unless otherwise specified

VCC=5V

Timing Requirements (VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.7 External Clock Input

Symbol	Parameter	Standard		Unit
		Min	Max	
tc	External Clock Input Cycle Time	33		ns
tw(H)	External Clock Input High ("H") Pulse Width	13		ns
tw(L)	External Clock Input Low ("L") Pulse Width	13		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

Table 5.8 Memory Expansion and Microprocessor Modes

Symbol	Parameter	Standard		Unit
		Min	Max	
tac1(RD-DB)	Data Input Access Time (RD standard, with no wait state)		(Note 1)	ns
tac1(AD-DB)	Data Input Access Time (AD standard, CS standard, with no wait state)		(Note 1)	ns
tac2(RD-DB)	Data Input Access Time (RD standard, with a wait state)		(Note 1)	ns
tac2(AD-DB)	Data Input Access Time (AD standard, CS standard, with a wait state)		(Note 1)	ns
tac3(RD-DB)	Data Input Access Time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tac3(AD-DB)	Data Input Access Time (AD standard, CS standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tac4(RAS-DB)	Data Input Access Time (RAS standard, when accessing a DRAM space)		(Note 1)	ns
tac4(CAS-DB)	Data Input Access Time (CAS standard, when accessing a DRAM space)		(Note 1)	ns
tac4(CAD-DB)	Data Input Access Time (CAD standard, when accessing a DRAM space)		(Note 1)	ns
tsu(DB-BCLK)	Data Input Setup Time	26		ns
tsu(RDY-BCLK)	$\overline{RDY}$ Input Setup Time	26		ns
tsu(HOLD-BCLK)	$\overline{HOLD}$ Input Setup Time	30		ns
th(RD-DB)	Data Input Hold Time	0		ns
th(CAS-DB)	Data Input Hold Time	0		ns
th(BCLK-RDY)	$\overline{RDY}$ Input Hold Time	0		ns
th(BCLK-HOLD)	$\overline{HOLD}$ Input Hold Time	0		ns
td(BCLK-HLDA)	$\overline{HLDA}$ Output Delay Time		25	ns

NOTES:
1. Values can be obtained from the following equations, according to BCLK frequecncy. Insert a wait state or lower the operation frequency, f(BCLK), if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9}{f(BCLK) \times 2} - 35 \quad [ns]$$

$$t_{ac1(AD-DB)} = \frac{10^9}{f(BCLK)} - 35 \quad [ns]$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns] \text{ (m=3 with 1 wait state, m=5 with 2 wait states and m=7 with 3 wait states)}$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times n}{f(BCLK)} - 35 \quad [ns] \text{ (n=2 with 1 wait state, n=3 with 2 wait states and n=4 with 3 wait states)}$$

$$t_{ac3(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns] \text{ (m=3 with 2 wait states and m=5 with 3 wait states)}$$

$$t_{ac3(AD-DB)} = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns] \text{ (n=5 with 2 wait states and n=7 with 3 wait states)}$$

$$t_{ac4(RAS-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns] \text{ (m=3 with 1 wait state and m=5 with 2 wait states)}$$

$$t_{ac4(CAS-DB)} = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns] \text{ (n=1 with 1 wait state and n=3 when 2 wait states)}$$

$$t_{ac4(CAD-DB)} = \frac{10^9 \times l}{f(BCLK)} - 35 \quad [ns] \text{ (l=1 with 1 wait state and l=2 with 2 wait states)}$$

VCC=5V

Timing Requirements

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.9 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	100		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	40		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	40		ns

Table 5.10 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	400		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	200		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	200		ns

Table 5.11 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	200		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	100		ns

Table 5.12 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	100		ns

Table 5.13 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(UP)}$	TAi_{OUT} Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} Input High ("H") Pulse Width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} Input Low ("L") Pulse Width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} Input Hold Time	400		ns

VCC=5V

Timing Requirements

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.14 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Pulse Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Pulse Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Pulse Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Pulse Width (counted on both edges)	80		ns

Table 5.15 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Pulse Width	200		ns

Table 5.16 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Pulse Width	200		ns

Table 5.17 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(AD)}$	$\overline{AD_{TRG}}$ Input Cycle Time (required for re-trigger)	1000		ns
$t_{w(ADL)}$	$\overline{AD_{TRG}}$ Input Low ("L") Pulse Width	125		ns

Table 5.18 Serial I/O

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Pulse Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Pulse Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Set Up Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 5.19 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Pulse Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Pulse Width	250		ns

VCC=5V

Switching Characteristics

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.20 Memory Expansion Mode and Microprocessor Mode (with No Wait State)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.1		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-select Signal Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-CS)}$	Chip-select Signal Output Hold Time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE Signal Output Delay Time			18	ns
$t_{h(BCLK-ALE)}$	ALE Signal Output Hold Time		-2		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-5		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		-3		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 1)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 1)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [ns]$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{w(WR)} = \frac{10^9}{f_{(BCLK)} \times 2} - 15 \quad [ns]$$

VCC=5V

Switching Characteristics

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.21 Memory Expansion Mode and Microprocessor Mode (With a Wait State, Accessing an External Memory)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.1		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-select Signal Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-CS)}$	Chip-select Signal Output Hold Time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE Signal Output Delay Time			18	ns
$t_{h(BCLK-ALE)}$	ALE Signal Output Hold Time		-2		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-5		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		-3		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 1)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{W(WR)}$	WR Output Width		(Note 1)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9 \times n}{f(BCLK)} - 20 \quad [ns]$$ (n=1 with 1 wait state, n=2 with 2 wait states and n=3 with 3 wait states)

$$t_{h(WR-DB)} = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$t_{W(WR)} = \frac{10^9 \times n}{f(BCLK) \times 2} - 15 \quad [ns]$$ (n=1 with 1 wait state, n=3 with 2 wait states and n=5 with 3 wait states)

VCC=5V

Switching Characteristics

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.22 Memory Expansion Mode and Microprocessor Mode (With a Wait State, Accessing an External Memory and Selecting a Space with the Multiplexed Bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address Output Delay Time	See Figure 5.1		18	ns
th(BCLK-AD)	Address Output Hold Time (BCLK standard)		-3		ns
th(RD-AD)	Address Output Hold Time (RD standard)		(Note 1)		ns
th(WR-AD)	Address Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select Signal Output Delay Time			18	ns
th(BCLK-CS)	Chip-select Signal Output Hold Time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select Signal Output Hold Time (RD standard)		(Note 1)		ns
th(WR-CS)	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-RD)	RD Signal Output Delay Time			18	ns
th(BCLK-AD)	RD Signal Output Hold Time		-5		ns
td(BCLK-WR)	WR Signal Output Delay Time			18	ns
th(BCLK-WR)	WR Signal Output Hold Time		-3		ns
td(DB-WR)	Data Output Delay Time (WR standard)		(Note 1)		ns
th(WR-DB)	Data Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE Signal Output Delay Time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE Signal Output Hold Time (BCLK standard)		-2		ns
td(AD-ALE)	ALE Signal Output Delay Time (address standard)		(Note 1)		ns
th(ALE-AD)	ALE Signal Output Hold Time (address standard)		(Note 1)		ns
tdz(RD-AD)	Address Output High-Impedance Time			8	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$th(RD-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(RD-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$td(DB-WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \quad [ns] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$th(WR-DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$td(AD-ALE) = \frac{10^9}{f(BCLK) \times 2} - 20 \quad [ns]$$

$$th(ALE-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

VCC=5V

Switching Characteristics

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.23 Memory Expansion Mode and Microprocessor Mode

(With a Wait State, Accessing an External Memory and Selecting the DRAM Space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
$t_{d(BCLK-RAD)}$	Row Address Output Delay Time	See Figure 5.1		18	ns
$t_{h(BCLK-RAD)}$	Row Address Output Hold Time (BCLK standard)		-3		ns
$t_{d(BCLK-CAD)}$	Column Address Output Delay Time			18	ns
$t_{h(BCLK-CAD)}$	Column Address Output Hold Time (BCLK standard)		-3		ns
$t_{h(RAS-RAD)}$	Row Address Output Hold Time after RAS Output		(Note 1)		ns
$t_{d(BCLK-RAS)}$	RAS Output Delay Time (BCLK standard)			18	ns
$t_{h(BCLK-RAS)}$	RAS Output Hold Time (BCLK standard)		-3		ns
t_{RP}	RAS High ("H") Hold Time		(Note 1)		ns
$t_{d(BCLK-CAS)}$	CAS Output Delay Time (BCLK standard)			18	ns
$t_{h(BCLK-CAS)}$	CAS Output Hold Time (BCLK standard)		-3		ns
$t_{d(BCLK-DW)}$	DW Output Delay Time (BCLK standard)			18	ns
$t_{h(BCLK-DW)}$	DW Output Hold Time (BCLK standard)		-5		ns
$t_{su(DB-CAS)}$	CAS Output Setup Time after DB Output		(Note 1)		ns
$t_{h(BCLK-DB)}$	DB Signal Output Hold Time (BCLK standard)		-7		ns
$t_{su(CAS-RAS)}$	CAS Output Setup Time before RAS Output (refresh)		(Note 1)		ns

NOTES:

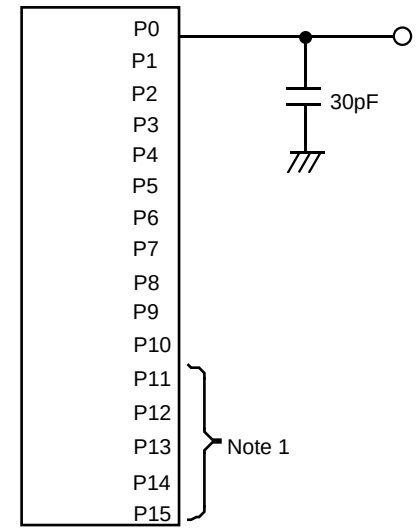
1. Values can be obtained from the following equation, according to BCLK frequency.

$$t_{h(RAS-RAD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [ns]$$

$$t_{RP} = \frac{10^9 \times 3}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

$$t_{su(DB-CAS)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [ns]$$

$$t_{su(CAS-RAS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [ns]$$



NOTES:

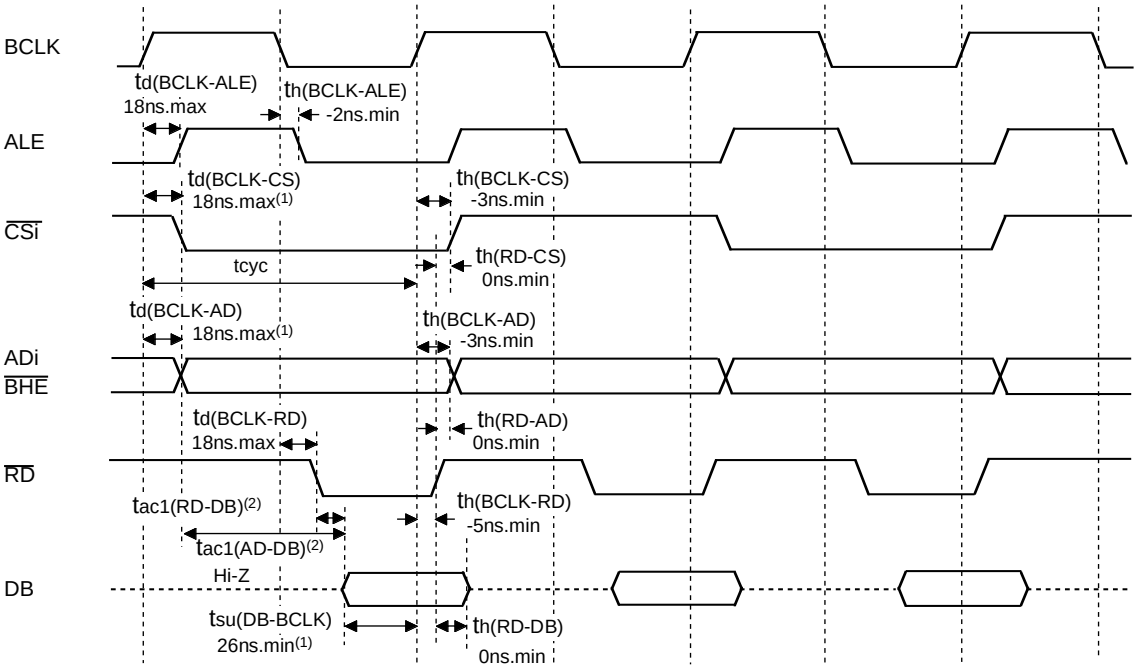
1. P11 to P15 are provided in the 144-pin package only.

Figure 5.1 P0 to P15 Measurement Circuit

Vcc=5V

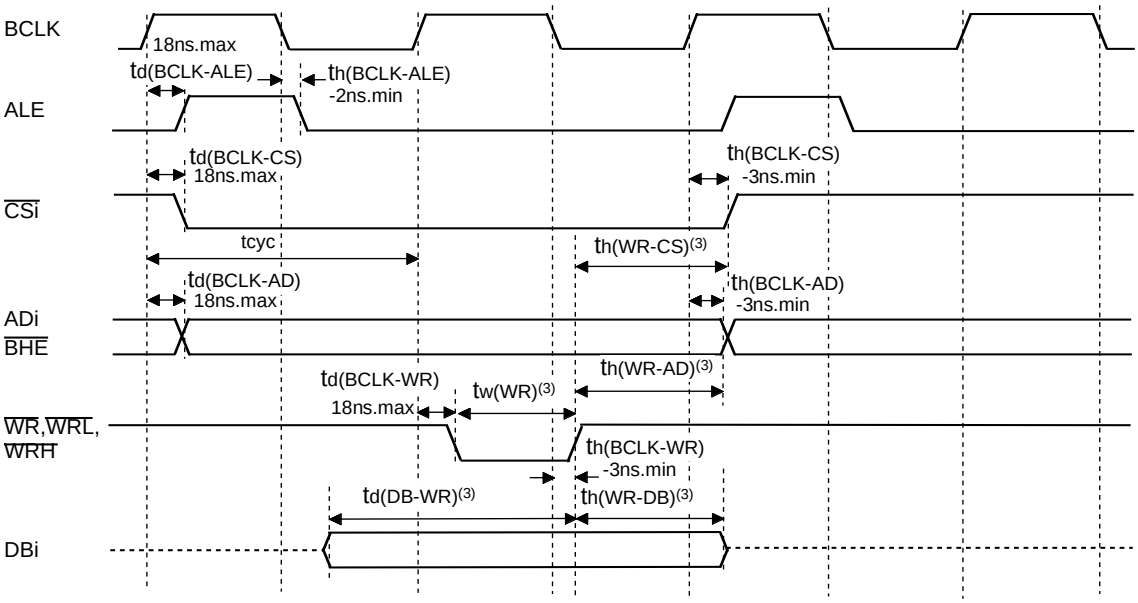
Memory Expansion Mode and Microprocessor Mode (with no wait state)

Read Timing



NOTES:
1. Values guaranteed only when the microcomputer is used independently.
   A maximum of 35ns is guaranteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
2. Varies with operation frequency:
   $t_{ac1(RD-DB)}$=(tcyc/2-35)ns.max
   $t_{ac1(AD-DB)}$=(tcyc-35)ns.max

Write Timing (written in 2 cycles with no wait state)



NOTES:
3. Varies with operation frequency:
   $t_{d(DB-WR)}$=(tcyc-20)ns.min
   $t_{h(WR-DB)}$=(tcyc/2-10)ns.min
   $t_{h(WR-AD)}$=(tcyc/2-10)ns.min
   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min
   $t_{w(WR)}$=(tcyc/2-15)ns.min

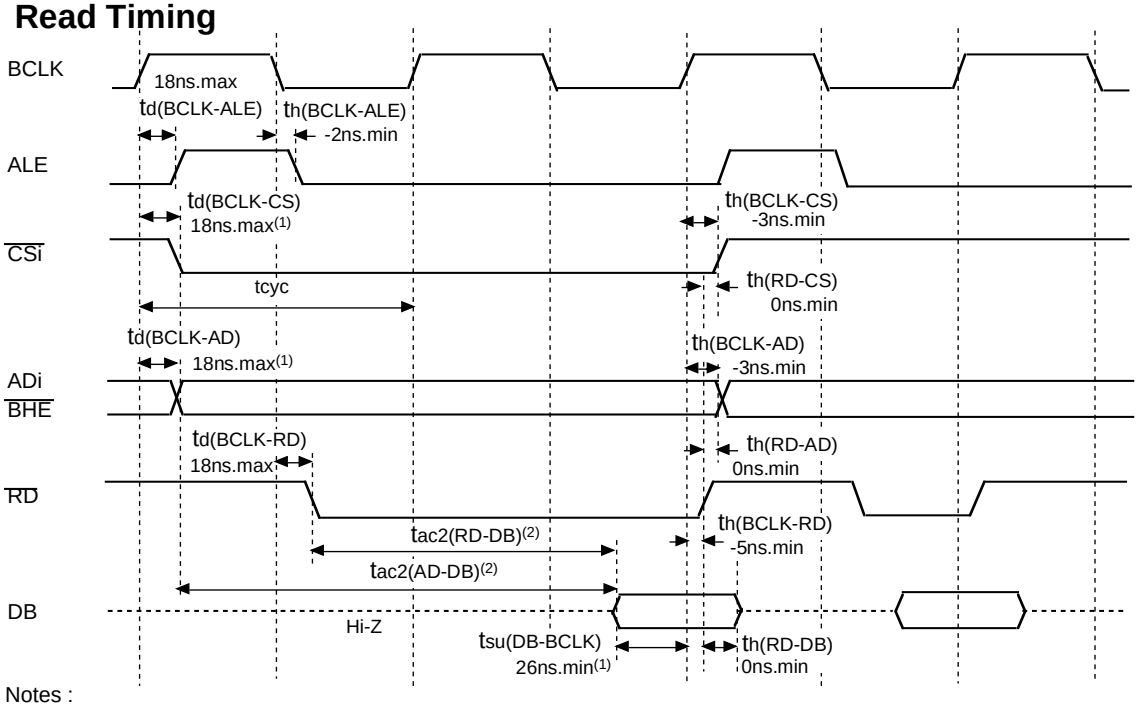
Measurement Conditions:
- V_{CC}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

Figure 5.2 Vcc=5V Timing Diagram (1)

Vcc=5V

Memory Expansion Mode and Microprocessor Mode (with a wait state)

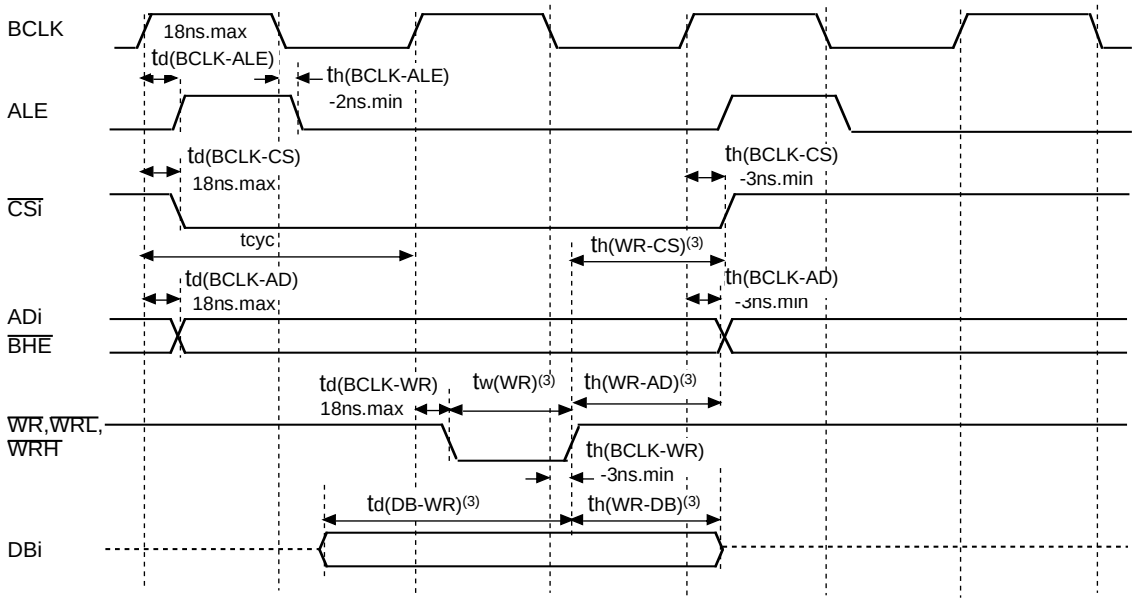
Read Timing



Notes :

1. Value guaranteed only when the microcomputer is used independently.
   A maximum of 35ns is guaranteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
2. Varies with operation frequency:
   $t_{ac2(RD-DB)}$=(tcyc/2 x m-35)ns.max (m=3 with 1 wait state, m=5 with 2 wait states and m=7 with 3 wait states.)
   $t_{ac2(AD-DB)}$=(tcyc x n-35)ns.max (n=2 with 1 wait state, n=3 with 2 wait states and n=4 with 3 wait states.)

Write Timing (written in 2 cycles with no wait state)



NOTES:

3. Varies with operation frequency:
   $t_{d(DB-WR)}$=(tcyc x n-20)ns.min
   (n=1 with 1 wait state, n=2 with 2 wait states and n=3 with 3 wait states)
   $t_{h(WR-DB)}$=(tcyc/2-10)ns.min
   $t_{h(WR-AD)}$=(tcyc/2-10)ns.min
   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min
   $t_{w(WR)}$=(tcyc/2 x n-15)ns.min
   (n=1 with 1 wait state, n=3 with 2 wait states and n=5 with 3 wait states)

Measurement conditions

- V_{CC}=4.2 to 5.5V
- Input high and low voltage:
  V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage:
  V_{OH}=2.0V, V_{OL}=0.8V

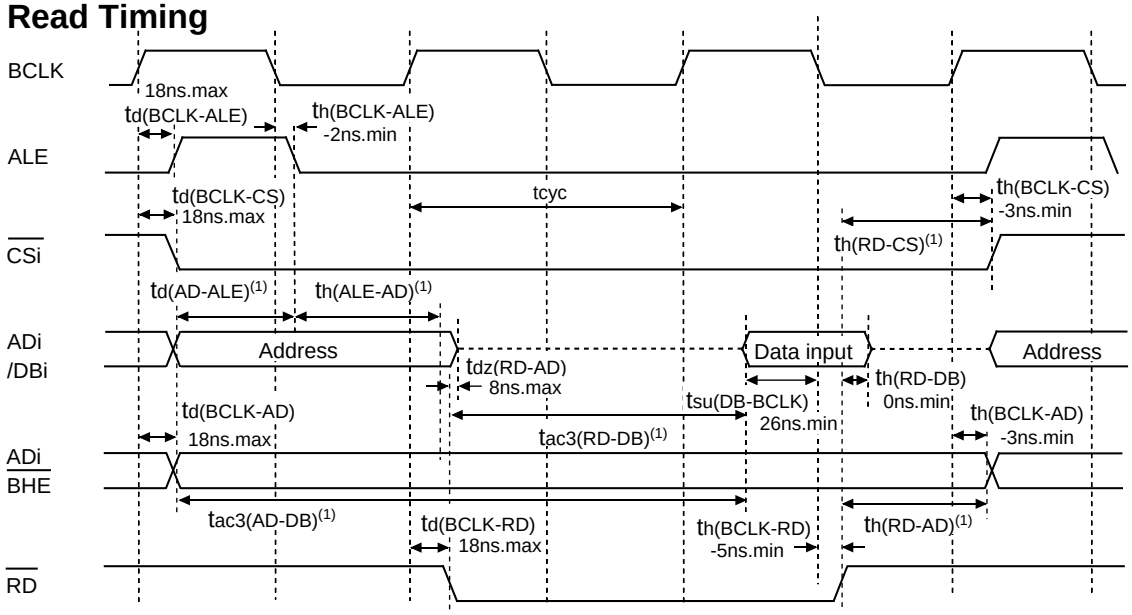
Figure 5.3 Vcc=5V Timing Diagram (2)

Vcc=5V

Memory Expansion Mode and Microprocessor Mode

(with a wait state, when accessing an external memory and using the multiplexed bus)

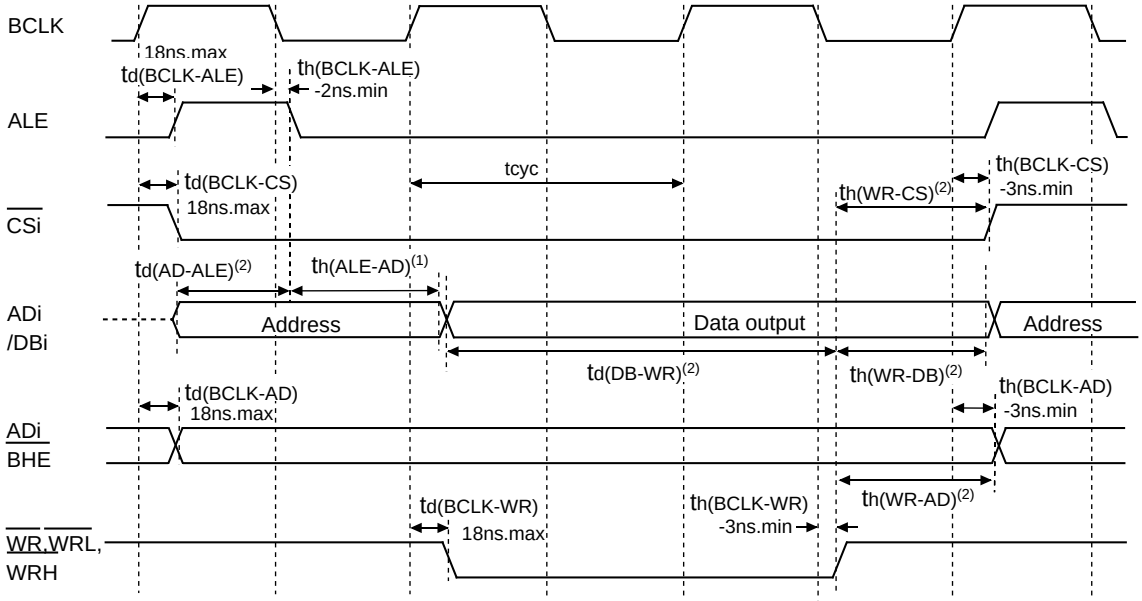
Read Timing



NOTES:

1. Varies with operation frequency:
   $t_{d(AD-ALE)}$=(tcyc/2-20)ns.min
   $t_{h(ALE-AD)}$=(tcyc/2-10)ns.min, $t_{h(RD-AD)}$=(tcyc/2-10)ns.min, $t_{h(RD-CS)}$=(tcyc/2-10)ns.min
   $t_{ac3(RD-DB)}$=(tcyc/2 x m-35)ns.max (m=3 with 2 wait states and m=5 with 3 wait states)
   $t_{ac3(AD-DB)}$=(tcyc/2 x n-35)ns.max (n=5 with 2 wait states and n=7 with 3 wait states)

Write Timing (written in 2 cycles with no wait state)



NOTES:

2. Varies with operation frequency:
   $t_{d(AD-ALE)}$=(tcyc/2-20)ns.min
   $t_{h(ALE-AD)}$=(tcyc/2-10)ns.min, $t_{h(WR-AD)}$=(tcyc/2-10)ns.min
   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min, $t_{h(WR-DB)}$=(tcyc/2-10)ns.min
   $t_{d(DB-WR)}$=(tcyc/2 x m-25)ns.min

Measurement Conditions:

- V_{CC}=4.2 to 5.5V
- Input high and low voltage:
  V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage:
  V_{OH}=2.0V. V_{OL}=0.8V

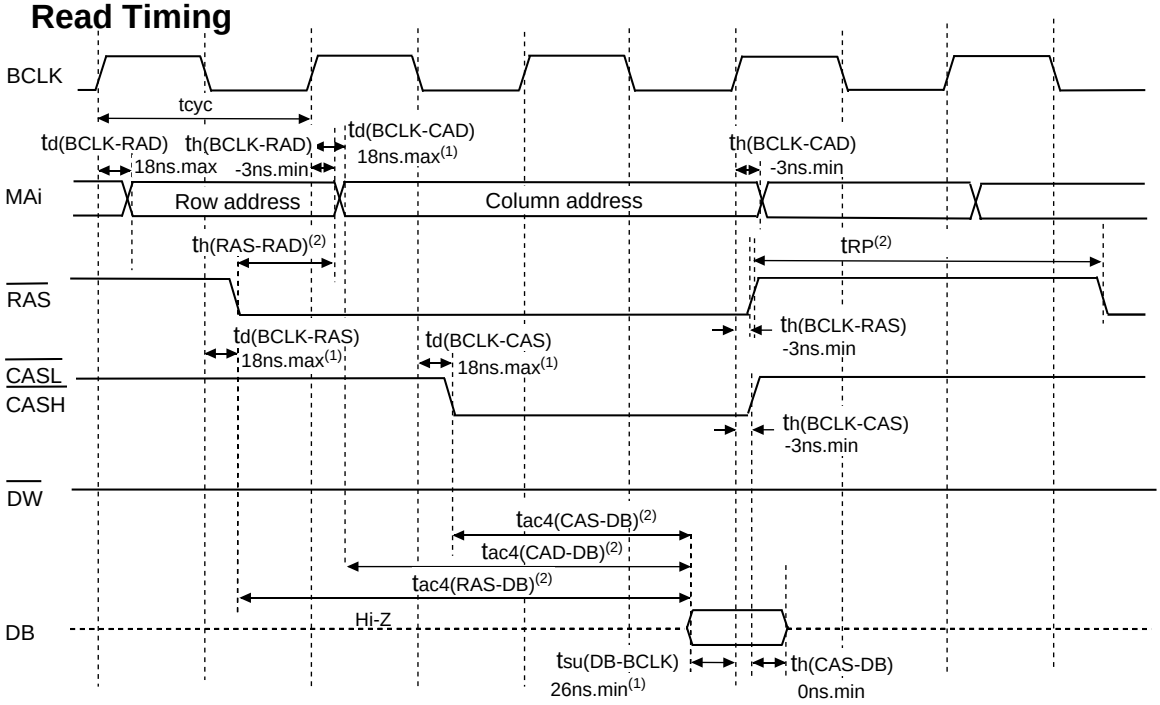
Figure 5.4 Vcc=5V Timing Diagram (3)

Vcc=5V

Memory Expansion Mode and Microprocessor Mode

(When accessing the DRAM area)

Read Timing



NOTES:

1. Values guaranteed only when the microcomputer is used independently.
   A maximum of 35ns is guaranteed for the following combinations.
   - $t_{d(BCLK-RAS)} + t_{su(DB-BCLK)}$
   - $t_{d(BCLK-CAS)} + t_{su(DB-BCLK)}$
   - $t_{d(BCLK-CAD)} + t_{su(DB-BCLK)}$
2. Varies with operation frequency:
   - $t_{ac4(RAS-DB)}$=(tcyc/2 x m-35)ns.max (m=3 with 1 wait state and m=5 with 2 wait states)
   - $t_{ac4(CAS-DB)}$=(tcyc/2 x n-35)ns.max (n=1 with 1 wait state and n=3 with 2 wait states)
   - $t_{ac4(CAD-DB)}$=(tcyc x l-35)ns.max (l=1 with 1 wait state and l=2 with 2 wait states)
   - $t_{h(RAS-RAD)}$=(tcyc/2-13)ns.min
   - t_{RP}=(tcyc/2 x 3-20)ns.min

Measurement Conditions:

- V_{CC}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

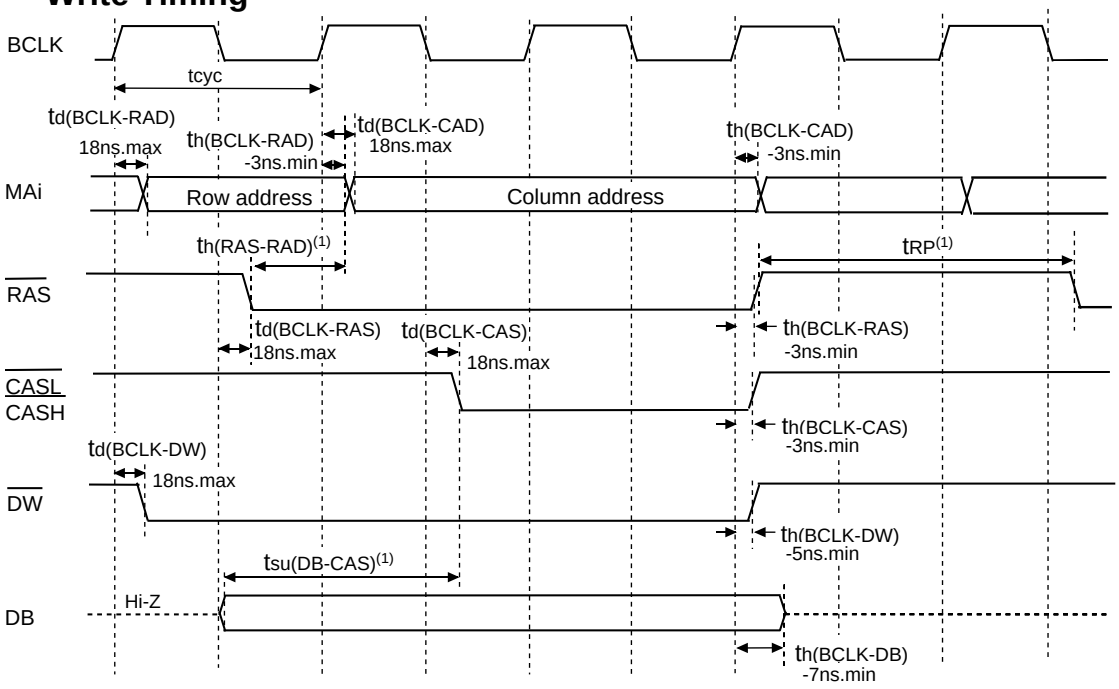
Figure 5.5 Vcc=5V Timing Diagram (4)

Memory Expansion Mode and Microprocessor Mode

Vcc=5V

(When accessing the DRAM area)

Write Timing



NOTES:

1. Varies with operation frequency:
   $t_{h(RAS-RAD)}$=(tcyc/2-13)ns.min
   t_{RP}=(tcyc/2 x 3-20)ns.min
   $t_{su(DB-CAS)}$=(tcyc-20)ns.min

Measurement Conditions:

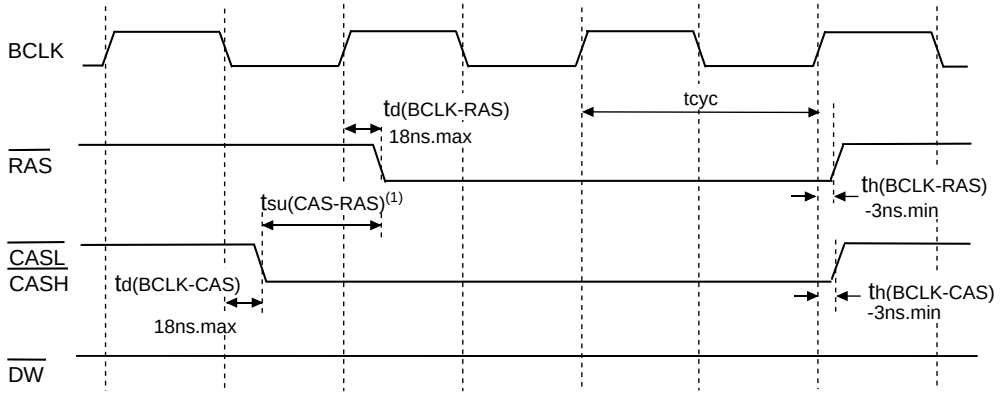
- V_{CC}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

Figure 5.6 Vcc=5V Timing Diagram (5)

Memory Expansion Mode and Microprocessor Mode

Vcc=5V

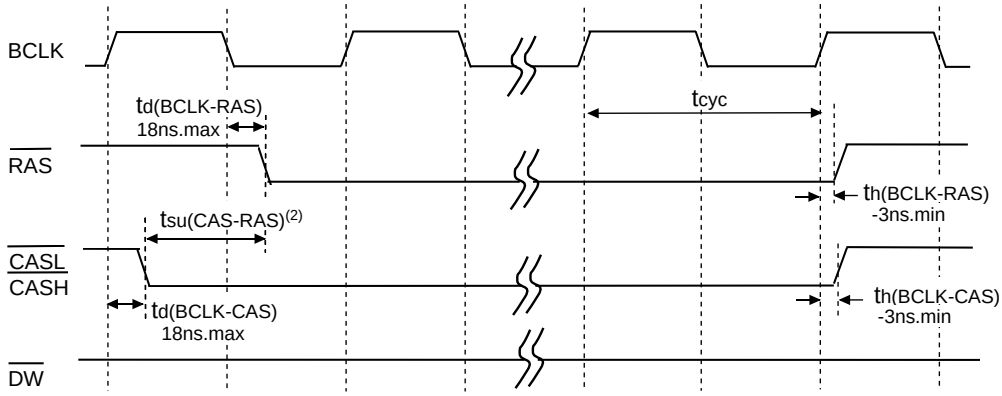
Refresh Timing (CAS-before-RAS refresh)



NOTES :

1. Varies with operation frequency:
   $t_{su(CAS-RAS)}$=(tcyc/2-13)ns.min

Refresh Timing (Self-refresh)



NOTES:

2. Varies with operation frequency:
   $t_{su(CAS-RAS)}$=(tcyc/2-13)ns.min

Measurement Conditions:

- V_{CC}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

Figure 5.7 Vcc=5V Timing Diagram (6)

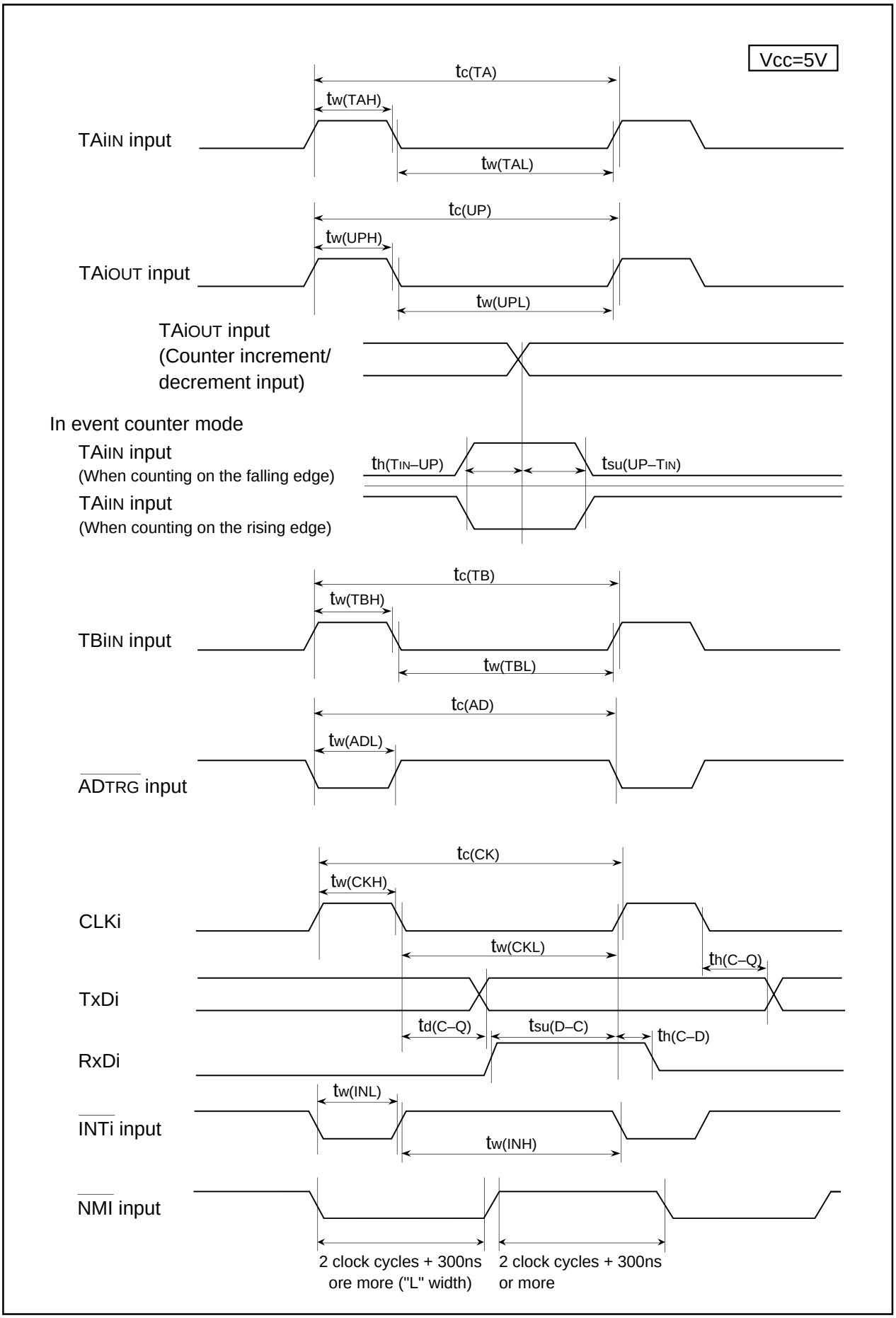
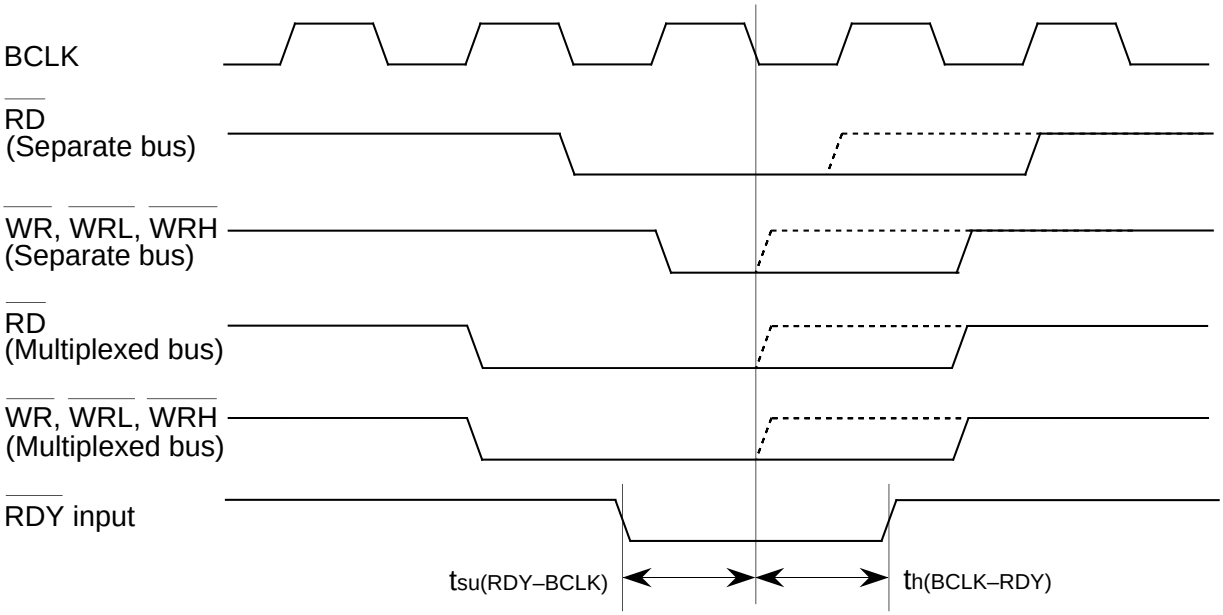


Figure 5.8 Vcc=5V Timing Diagram (7)

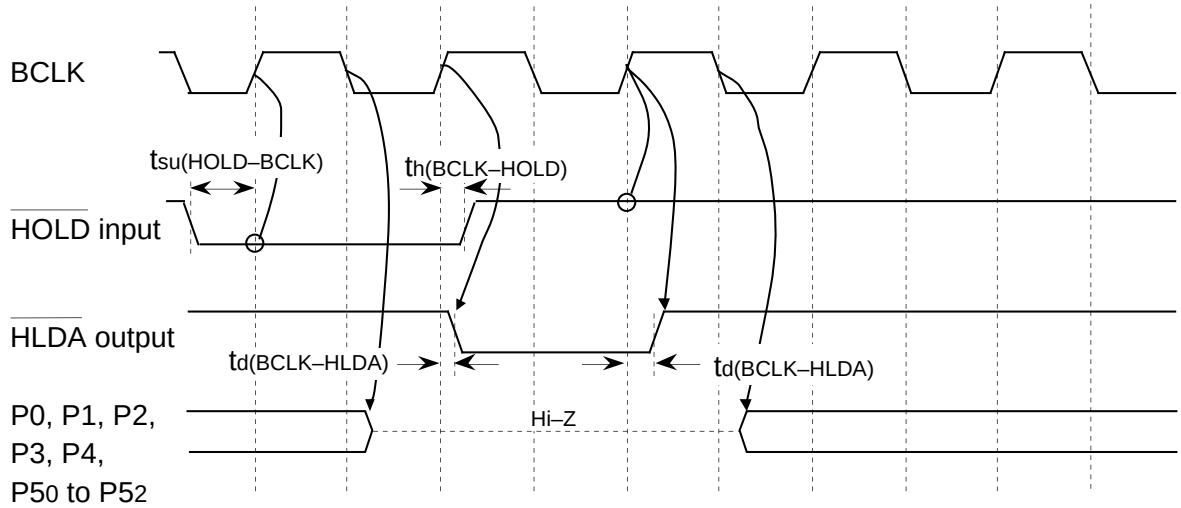
Vcc=5V

Memory Expansion Mode and Microprocessor Mode

(Valid only with a wait state)



(Valid with a wait state or with no wait state)



Measurement Conditions:

- VCC=4.2 to 5.5V
- Input high and low voltage: VIH=4.0V, VIL=1.0V
- Output high and low voltage: VOH=2.5V, VOL=2.5V

Figure 5.9 Vcc=5V Timing Diagram (8)

VCC=3.3V

Table 5.24 Electrical Characteristics (VCC=3.0 to 3.6V, VSS=0V at Topr = –20 to 85°C, f(XIN)=20MHz unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit
				Min	Typ	Max	
VOH	Output High ("H") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(1)	IOH=-1mA	Vcc-0.6			V
		XOUT	IOH=-0.1mA	2.7			V
		XCOUT	No load applied		3.3		V
VOL	Output Low ("L") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(1)	IOL=1mA			0.5	V
		XOUT	IOL=0.1mA			0.5	V
		XCOUT	No load applied		0		V
VT+-VT-	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN-TA4IN, TB0IN-TB5IN, $\overline{INT0}$-$\overline{INT5}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, TA0OUT-TA4OUT, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		RESET		0.2		1.8	V
IIH	Input High ("H") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(1), XIN, $\overline{RESET}$, CNVSS, BYTE	VI=3V			4.0	µA
IIL	Input Low ("L") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(1), XIN, $\overline{RESET}$, CNVSS, BYTE	VI=0V			-4.0	µA
RPULLUP	Pull-up Resistance	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(1)	VI=0V	66	120	500	kΩ
RfXIN	Feedback Resistance	XIN			3.0		MΩ
RfXCIN	Feedback Resistance	XCIN			20.0		MΩ
VRAM	RAM Standby Voltage	Through VDC		2.5			V
		Not through VDC		2.0			V
ICC	Power Supply Current	Measurement condition: In single-chip mode, output pins are left open and other pins are connected to VSS.	f(XIN)=20 MHz, square wave, no division		26	38	mA
			f(XCIN)=32 kHz, with a wait state, not through VDC, Topr=25° C		5.0		µA
			f(XCIN)=32 kHz, with a wait state, through VDC, Topr=25° C		340		µA
			Topr=25° C when the clock stops		0.4	20	µA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

VCC=3.3V

Table 5.25 A/D Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 3.0 to 3.6V, V_{SS} = AV_{SS} = 0V at Topr = –20 to 85°C, f(X_{IN}) = 20MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min	Typ	Max	
-	Resolution		V_{REF}=V_{CC}			10	Bits
INL	Integral Nonlinearity Error	No S&H function (8-bit)	V_{CC}=V_{REF}=3.3V			±2	LSB
DNL	Differential Nonlinearity Error	No S&H function (8-bit)				±1	LSB
-	Offset Error	No S&H function (8-bit)				±2	LSB
-	Gain Error	No S&H function (8-bit)				±2	LSB
R_{LADDER}	Resistor Ladder		V_{REF}=V_{CC}	8		40	kΩ
t_{CONV}	8-bit Conversion Time			4.9			µs
V_{REF}	Reference Voltage			3.0		V_{CC}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

S&H: Sample and hold

NOTES:
1. Divide f(X_{IN}), if exceeding 10 MHz, to keep ϕAD frequency at 10 MHz or less.

Table 5.26 D/A Conversion Characteristics (V_{CC} = V_{REF} = 3.0 to 3.6V, V_{SS} = AV_{SS} = 0V at Topr = –20 to 85°C, f(X_{IN}) = 20MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.0	mA

NOTES:
1. Measurement results when using one D/A converter. The DAi register (i=0, 1) of the D/A converter not being used is set to "00_{16}". The resistor ladder in the A/D converter is exclued.
I_{VREF} flows even if the VCUT bit in the ADiCON1 register is set to "0" (no V_{REF} connection).

Table 5.27 Flash Memory Version Electrical Characteristics

Parameter	Standard			Unit
	Min	Typ	Max	
Program Time (per page)		8	120	ms
Block Erase Time (per block)		50	600	ms

NOTES:
1. V_{CC}= 4.2 to 5.5V (through VDC), 3.0 to 3.6V (not through VDC) at Topr= 0 to 60° C, unless otherwise specified

VCC=3.3V

Timing Requirements (Vcc = 3.0 to 3.6V, Vss = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.28 External Clock Input

Symbol	Parameter	Standard		Unit
		Min	Max	
tc	External Clock Input Cycle Time	50		ns
tw(H)	External Clock Input High ("H") Pulse Width	22		ns
tw(L)	External Clock Input Low ("L") Pulse Width	22		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

Table 5.29 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min	Max	
tac1(RD-DB)	Data Input Access Time (RD standard, with no wait state)		(Note 1)	ns
tac1(AD-DB)	Data Input Access Time (AD standard, CS standard, with no wait state)		(Note 1)	ns
tac2(RD-DB)	Data Input Access Time (RD standard, with a wait state)		(Note 1)	ns
tac2(AD-DB)	Data Input Access Time (AD standard, CS standard, with a wait state)		(Note 1)	ns
tac3(RD-DB)	Data Input Access Time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tac3(AD-DB)	Data Input Access Time (AD standard, CS standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tac4(RAS-DB)	Data Input Access Time (RAS standard, when accessing a DRAM space)		(Note 1)	ns
tac4(CAS-DB)	Data Input Access Time (CAS standard, when accessing a DRAM space)		(Note 1)	ns
tac4(CAD-DB)	Data Input Access Time (CAD standard, when accessing a DRAM space)		(Note 1)	ns
tsu(DB-BCLK)	Data Input Setup Time	30		ns
tsu(RDY-BCLK)	RDY Input Setup Time	40		ns
tsu(HOLD-BCLK)	HOLD Input Setup Time	60		ns
th(RD-DB)	Data Input Hold Time	0		ns
th(CAS-DB)	Data Input Hold Time	0		ns
th(BCLK-RDY)	RDY Input Hold Time	0		ns
th(BCLK-HOLD)	HOLD Input Hold Time	0		ns
td(BCLK-HLDA)	HLDA Output Delay Time		25	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency. Insert a wait state or lower operation frequency, f(BCLK), if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9}{f(BCLK) \times 2} - 35 \quad [ns]$$

$$t_{ac1(AD-DB)} = \frac{10^9}{f(BCLK)} - 35 \quad [ns]$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns]\ (m=3 \text{ with 1 wait state, } m=5 \text{ with 2 wait states and } m=7 \text{ with 3 wait states})$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times n}{f(BCLK)} - 35 \quad [ns]\ (n=2 \text{ with 1 wait state, } n=3 \text{ with 2 wait states and } n=4 \text{ with 3 wait states})$$

$$t_{ac3(RD-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns]\ (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$t_{ac3(AD-DB)} = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns]\ (n=5 \text{ with 2 wait states and } n=7 \text{ with 3 wait states})$$

$$t_{ac4(RAS-DB)} = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns]\ (m=3 \text{ with 1 wait state and } m=5 \text{ with 2 wait states})$$

$$t_{ac4(CAS-DB)} = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns]\ (n=1 \text{ with 1 wait state and } n=3 \text{ when 2 wait states})$$

$$t_{ac4(CAD-DB)} = \frac{10^9 \times l}{f(BCLK)} - 35 \quad [ns]\ (l=1 \text{ with 1 wait state and } l=2 \text{ with 2 wait states})$$

VCC=3.3V

Timing Requirements

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.30 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Pulse Width	40		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Pulse Width	40		ns

Table 5.31 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Pulse Width	200		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Pulse Width	200		ns

Table 5.32 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Pulse Width	100		ns

Table 5.33 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{w(TAH)}$	TAiIN Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Pulse Width	100		ns

Table 5.34 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAiOUT Input High ("H") Pulse Width	1000		ns
$t_{w(UPL)}$	TAiOUT Input Low ("L") Pulse Width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

VCC=3.3V

Timing Requirements

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.35 Timer B input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Pulse Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Pulse Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Pulse Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Pulse Width (counted on both edges)	80		ns

Table 5.36 Timer B input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Pulse Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Pulse Width	200		ns

Table 5.37 Timer B input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Pulse Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Pulse Width	200		ns

Table 5.38 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(AD)}$	$\overline{AD_{TRG}}$ Input High ("H") Pulse Width (required for re-trigger)	1000		ns
$t_{w(ADL)}$	$\overline{AD_{TRG}}$ Input Low ("L") Pulse Width	125		ns

Table 5.39 Serial I/O

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Pulse Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Pulse Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Set Up Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 5.40 External Interrupt $\overline{INTi}$ input

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{w(INH)}$	INTi Input High ("H") Pulse Width	250		ns
$t_{w(INL)}$	INTi Input Low ("L") Pulse Width	250		ns

VCC=3.3V

Switching Characteristics

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C, unless otherwise specified)

Table 5.41 Memory Expansion Mode and Microprocessor Mode (with No Wait State)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.1		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-select Signal Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-CS)}$	Chip-select Signal Output Hold Time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE Signal Output Delay Time			18	ns
$t_{h(BCLK-ALE)}$	ALE Signal Output Hold Time		-2		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-3		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 1)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 1)		ns

NOTES:

1. Values can be obtained from the following equations according to the BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [ns]$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{w(WR)} = \frac{10^9}{f_{(BCLK)} \times 2} - 15 \quad [ns]$$

VCC=3.3V

Switching Characteristics

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.42 Memory Expansion Mode and Microprocessor Mode (With a Wait State, Accessing an External Memory)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address Output Delay Time	See Figure 5.1		18	ns
th(BCLK-AD)	Address Output Hold Time (BCLK standard)		0		ns
th(RD-AD)	Address Output Hold Time (RD standard)		0		ns
th(WR-AD)	Address Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select Signal Output Delay Time			18	ns
th(BCLK-CS)	Chip-select Signal Output Hold Time (BCLK standard)		0		ns
th(RD-CS)	Chip-select Signal Output Hold Time (RD standard)		0		ns
th(WR-CS)	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE Signal Output Delay Time			18	ns
th(BCLK-ALE)	ALE Signal Output Hold Time		-2		ns
td(BCLK-RD)	RD Signal Output Delay Time			18	ns
th(BCLK-RD)	RD Signal Output Hold Time		-3		ns
td(BCLK-WR)	WR Signal Output Delay Time			18	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(DB-WR)	Data Output Delay Time (WR standard)		(Note 1)		ns
th(WR-DB)	Data Output Hold Time (WR standard)		(Note 1)		ns
tw(WR)	WR Output Width		(Note 1)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$td(DB-WR) = \frac{10^9 \times n}{f(BCLK)} - 20 \quad [ns]$$ (n=1 with 1 wait state, n=2 with 2 wait states and n=3 with 3 wait states)

$$th(WR-DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$tw(WR) = \frac{10^9 \times n}{f(BCLK) \times 2} - 15 \quad [ns]$$ (n=1 with 1 wait state, n=3 with 2 wait states and n=5 with 3 wait states)

VCC=3.3V

Switching Characteristics

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.43 Memory Expansion Mode and Microprocessor Mode (With a Wait State, Accessing an External Memory and Selecting a Space with the Multiplexed Bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.1		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		(Note 1)		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-select Signal Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-CS)}$	Chip-select Signal Output Hold Time (RD standard)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-AD)}$	RD Signal Output Hold Time		-3		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 1)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE Signal Output Delay Time (BCLK standard)			18	ns
$t_{h(BCLK-ALE)}$	ALE Signal Output Hold Time (BCLK standard)		-2		ns
$t_{d(AD-ALE)}$	ALE Signal Output Delay Time (address standard)		(Note 1)		ns
$t_{h(ALE-AD)}$	ALE Signal Output Hold Time (address standard)		(Note 1)		ns
$t_{dz(RD-AD)}$	Address Output High-Impedance Time			8	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(RD-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(RD-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 25 \quad [ns] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{d(AD-ALE)} = \frac{10^9}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

$$t_{h(ALE-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

VCC=3.3V

Switching Characteristics

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.44 Memory Expansion Mode and Microprocessor Mode (With a Wait State, Accessing an External Memory and Selecting the DRAM Area)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
$t_{d(BCLK-RAD)}$	Row Address Output Delay Time	See Figure 5.1		18	ns
$t_{h(BCLK-RAD)}$	Row Address Output Hold Time (BCLK standard)		0		ns
$t_{d(BCLK-CAD)}$	Column Address Output Delay Time			18	ns
$t_{h(BCLK-CAD)}$	Column Address Output Hold Time (BCLK standard)		0		ns
$t_{h(RAS-RAD)}$	Row Address Output Hold Time after RAS Output		(Note 1)		ns
$t_{d(BCLK-RAS)}$	RAS Output Delay Time (BCLK standard)			18	ns
$t_{h(BCLK-RAS)}$	RAS Output Hold Time (BCLK standard)		0		ns
t_{RP}	RAS High ("H") Hold Time		(Note 1)		ns
$t_{d(BCLK-CAS)}$	CAS Output Delay Time (BCLK standard)			18	ns
$t_{h(BCLK-CAS)}$	CAS Output Hold Time (BCLK standard)		0		ns
$t_{d(BCLK-DW)}$	DW Output Delay Time (BCLK standard)			18	ns
$t_{h(BCLK-DW)}$	DW Output Hold Time (BCLK standard)		-3		ns
$t_{su(DB-CAS)}$	CAS Output Setup Time after DB output		(Note 1)		ns
$t_{h(BCLK-DB)}$	DB Signal Output Hold Time (BCLK standard)		-7		ns
$t_{su(CAS-RAS)}$	CAS Output Setup Time before RAS Output (refresh)		(Note 1)		ns

NOTES:

1. Values can be obtained from the following equations, according to the BCLK frequency.

$$t_{h(RAS-RAD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [ns]$$

$$t_{RP} = \frac{10^9 \times 3}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

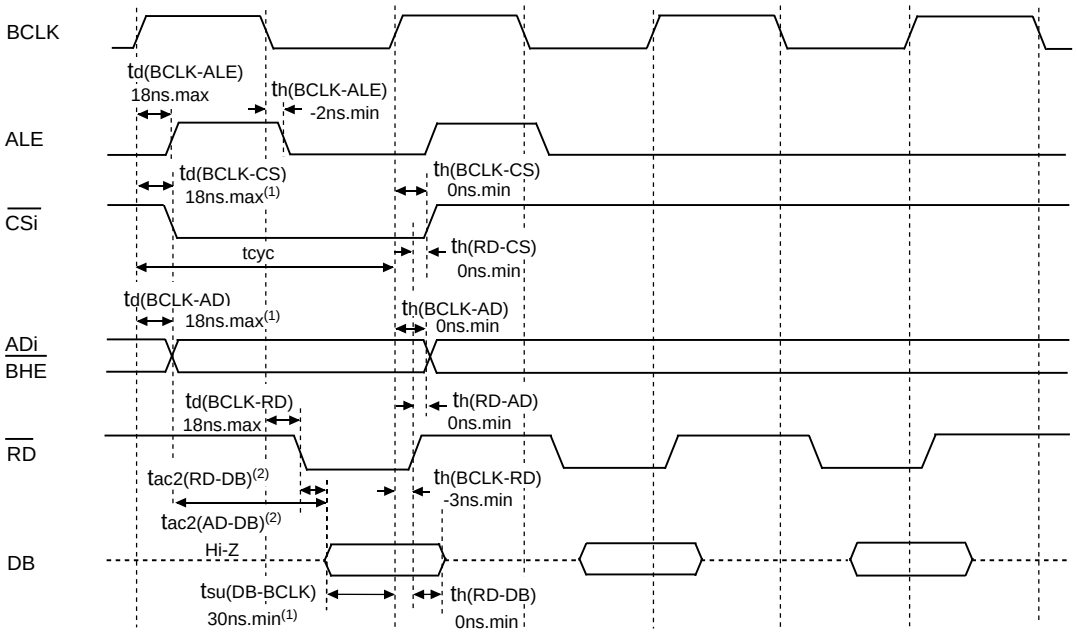
$$t_{su(DB-CAS)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [ns]$$

$$t_{su(CAS-RAS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [ns]$$

Vcc=3.3V

Memory Expansion Mode and Microprocessor Mode (with no wait state)

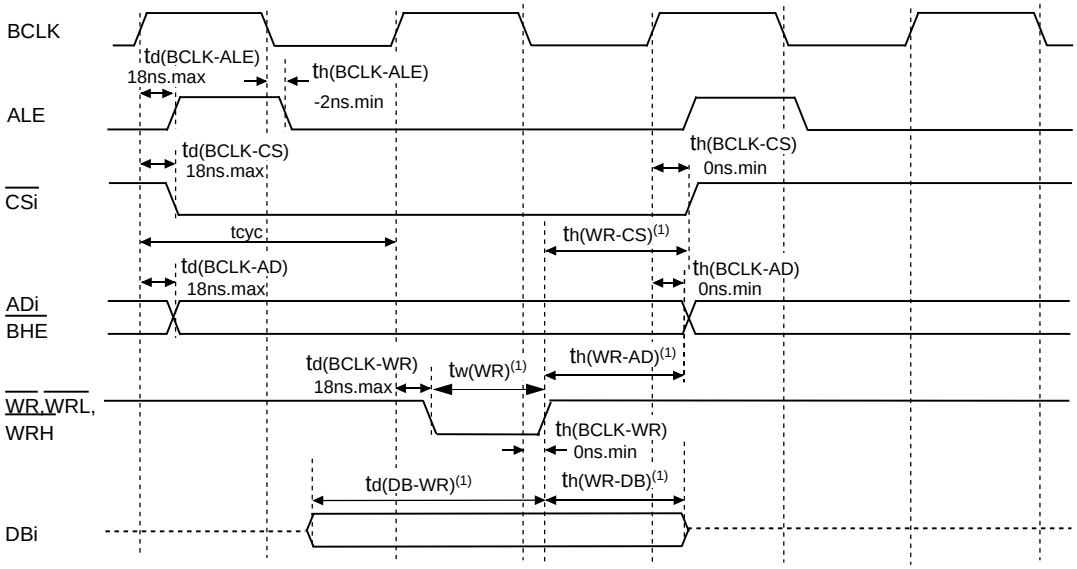
Read Timing



NOTES:

1. Values guaranteed only when the microcomputer is used independently.
   A maximum of 35ns is guaranteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
2. Varies with operation frequency:
   $t_{ac2(RD-DB)}$=(tcyc/2-35)ns.max
   $t_{ac2(AD-DB)}$=(tcyc-35)ns.max

Write Timing



NOTES:

1. Varies with operation frequency.
   $t_{d(DB-WR)}$=(tcyc-20)ns.min
   $t_{h(WR-DB)}$=(tcyc/2-10)ns.min
   $t_{h(WR-AD)}$=(tcyc/2-10)ns.min
   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min
   $t_{w(WR)}$=(tcyc/2-15)ns.min

Measurement Conditions:

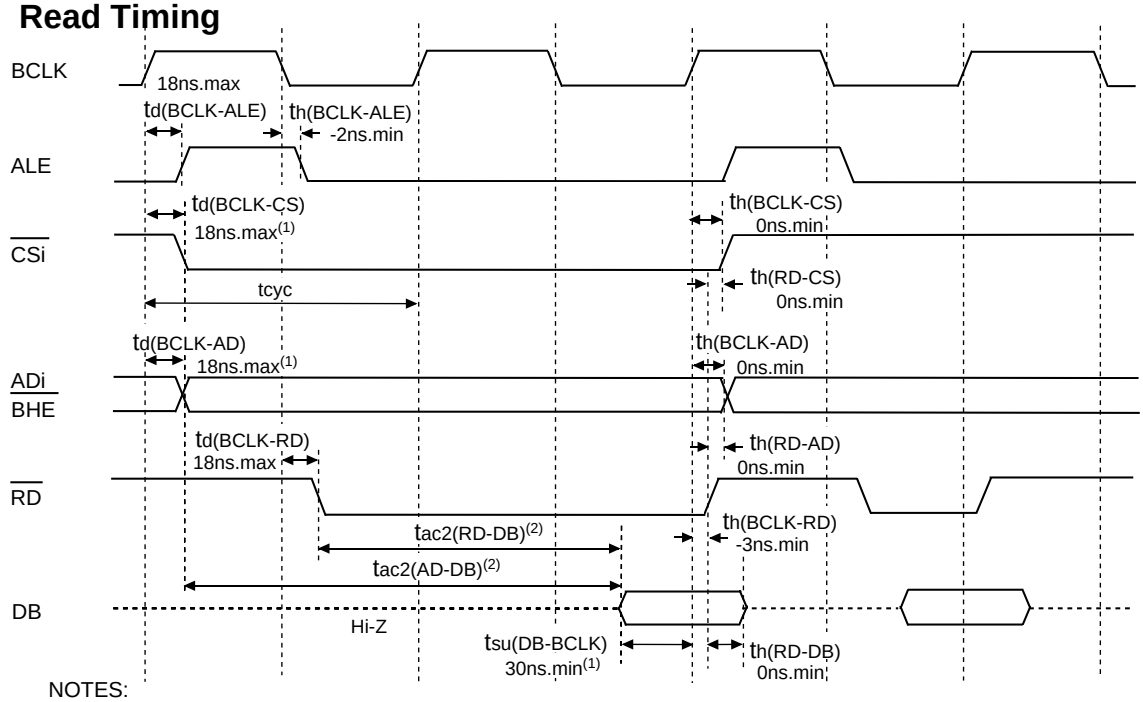
- V_{CC}=3.0 to 3.6V
- Input high and low voltage: V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage: V_{OH}=1.5V, V_{OL}=1.5V

Figure 5.10 V_{CC}=3.3V Timing Diagram (1)

Vcc=3.3V

Memory Expansion Mode and Microprocessor Mode (with a wait state)

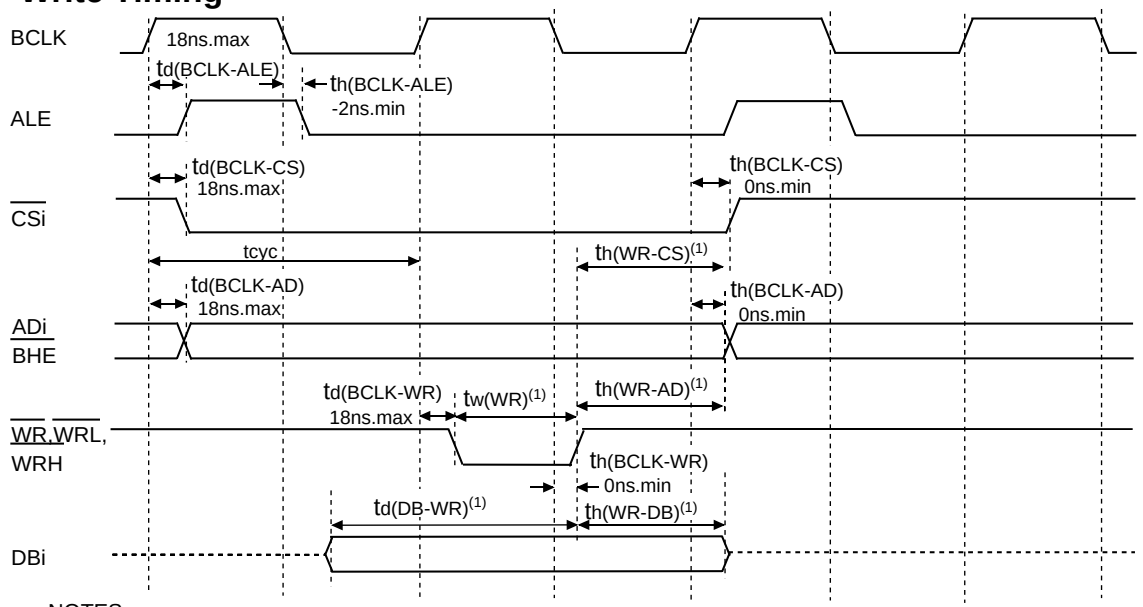
Read Timing



NOTES:

1. Values guaranteed only when the microcomputer is used independently. A maximum of 35ns is guaranteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
2. Varies with operation frequency.
   $t_{ac2(RD-DB)}$=(tcyc/2 x m-35)ns.max (m=3 with 1 wait state, m=5 with 2 wait states and m=7 with 3 wait states)
   $t_{ac2(AD-DB)}$=(tcyc x n-35)ns.max (n=2 with 1 wait state, n=3 with 2 wait states and n=4 with 3 wait states)

Write Timing



NOTES:

1. Varies with operation frequency.
   $t_{d(DB-WR)}$=(tcyc x n-20)ns.min
   (n=1 with 1 wait state, n=2 with 2 wait states and n=3 with 3 wait states)
   $t_{h(WR-DB)}$=(tcyc/2-10)ns.min
   $t_{h(WR-AD)}$=(tcyc/2-10)ns.min
   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min
   $t_{w(WR)}$=(tcyc/2 x n-15)ns.min
   (n=1 with 1 wait state, n=3 with 2 wait states and n=5 with 3 wait states)

Measurement Conditions:

- V_{CC}=3.0 to 3.6V
- Input high and low voltage:
  V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage:
  V_{OH}=1.5V, V_{OL}=1.5V

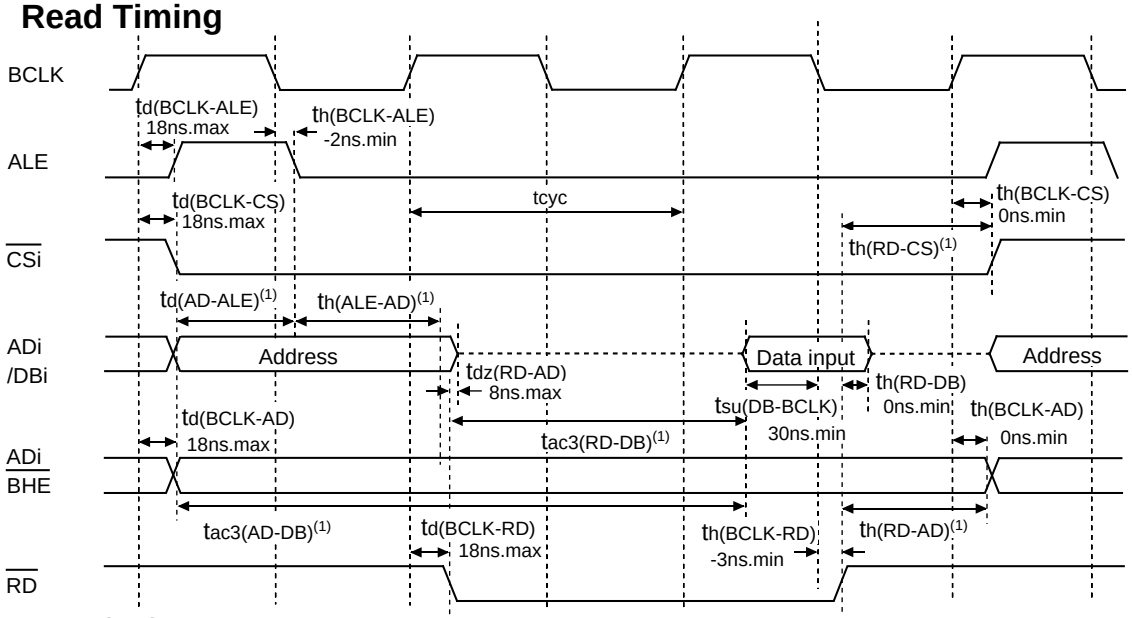
Figure 5.11 V_{CC}=3.3V Timing Diagram (2)

Vcc=3.3V

Memory Expansion Mode and Microprocessor Mode

(with a wait state, when accessing an external memory and using the multiplexed bus)

Read Timing



NOTES:

1. Varies with operation frequency.

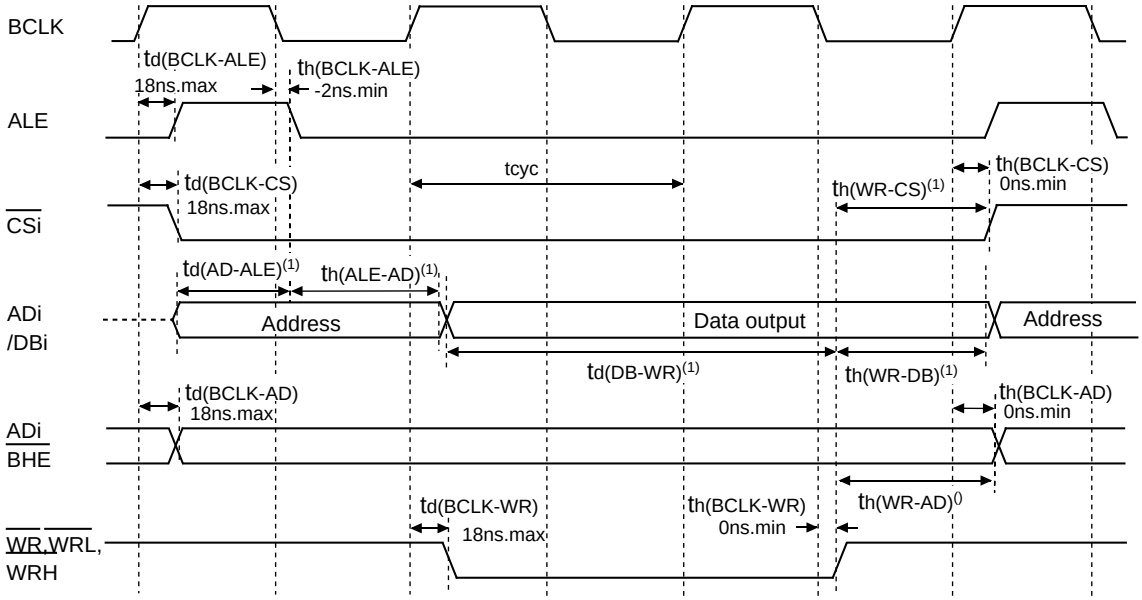
$t_{d(AD-ALE)}$=(tcyc/2-20)ns.min

$t_{h(ALE-AD)}$=(tcyc/2-10)ns.min, $t_{h(RD-AD)}$=(tcyc/2-10)ns.min, $t_{h(RD-CS)}$=(tcyc/2-10)ns.min

$t_{ac3(RD-DB)}$=(tcyc/2 x m-35)ns.max (m=3 with 2 wait states and m=5 with 3 wait states)

$t_{ac3(AD-DB)}$=(tcyc/2 x n-35)ns.max (n=5 with 2 wait states and n=7 with 3 wait states)

Write Timing



NOTES:

1. Varies with operation frequency.

$t_{d(AD-ALE)}$=(tcyc/2-20)ns.min

$t_{h(ALE-AD)}$=(tcyc/2-10)ns.min, $t_{h(WR-AD)}$=(tcyc/2-10)ns.min

$t_{h(WR-CS)}$=(tcyc/2-10)ns.min, $t_{h(WR-DB)}$=(tcyc/2-10)ns.min

$t_{d(DB-WR)}$=(tcyc/2 x m-25)ns.min

(m=3 with 2 wait states and m=5 with 3 wait states)

Measurement Conditions:

- V_{CC}=3.0 to 3.6V
- Input high and low voltage:
  V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage:
  V_{OH}=1.5V, V_{OL}=1.5V

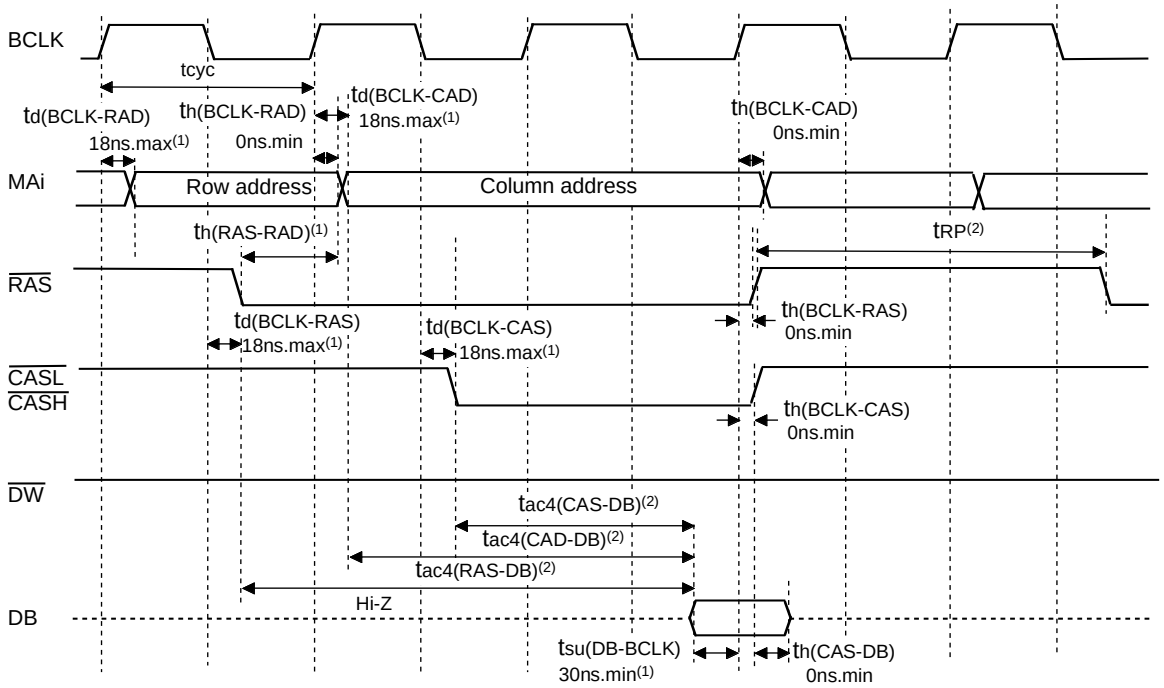
Figure 5.12 V_{CC}=3.3V Timing Diagram (3)

Vcc=3.3V

Memory Expansion Mode and Microprocessor Mode

(With 2 wait states, when accessing the DRAM area)

Read Timing



NOTES:

1. Values guaranteed only when the microcomputer is used independently. A maximum of 35ns is guaranteed for the followings:
   $t_{d(BCLK-RAS)} + t_{su(DB-BCLK)}$
   $t_{d(BCLK-CAS)} + t_{su(DB-BCLK)}$
   $t_{d(BCLK-CAD)} + t_{su(DB-BCLK)}$
2. It varies with the operation frequency.
   $t_{ac4(RAS-DB)}$=(tcyc/2 x m-35)ns.max (m=3 with 1 wait state and m=5 with 2 wait states)
   $t_{ac4(CAS-DB)}$=(tcyc/2 x n-35)ns.max (n=1 with 1 wait state and n=3 with 2 wait states)
   $t_{ac4(CAD-DB)}$=(tcyc x l-35)ns.max (l=1 with 1 wait state and l=2 with 2 wait states)
   $t_{h(RAS-RAD)}$=(tcyc/2-13)ns.min
   t_{RP}=(tcyc/2 x 3-20)ns.min

Measurement Conditions:

- V_{CC}=3.0 to 3.6V
- Input high and low voltage: V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage: V_{OH}=1.5V, V_{OL}=1.5V

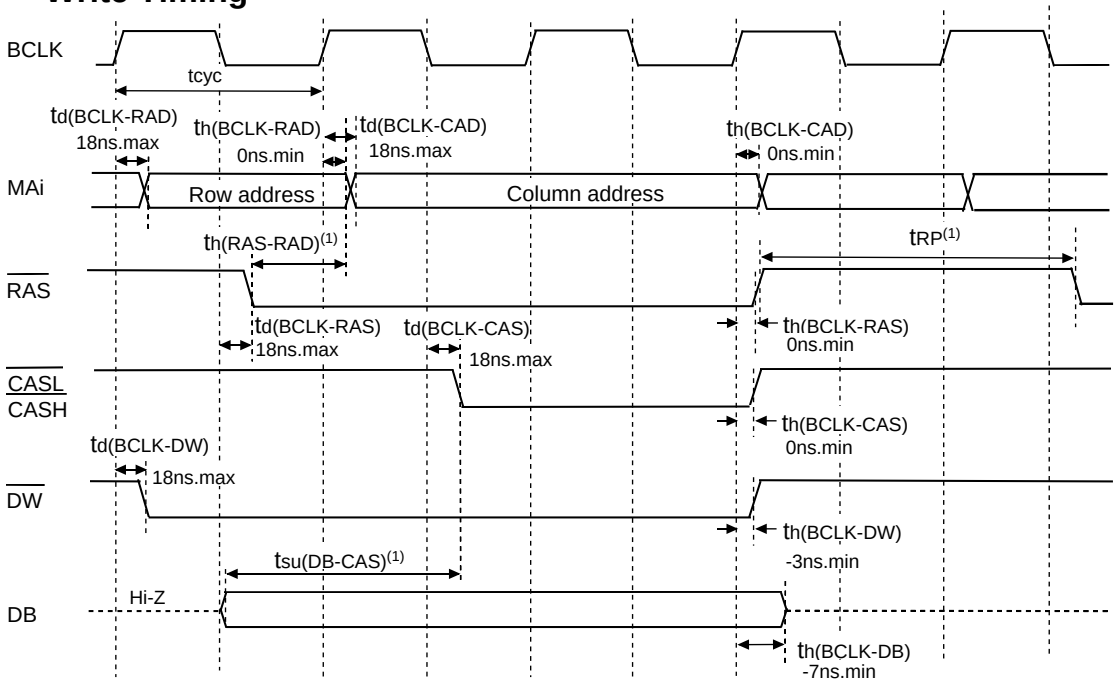
Figure 5.13 V_{CC}=3.3V Timing Diagram (4)

Vcc=3.3V

Memory Expansion Mode and Microprocessor Mode

(With 2 wait states, when accessing the DRAM area)

Write Timing



NOTES:

1. Varies with operation frequency.
   $t_{h(RAS-RAD)}$=(tcyc/2-13)ns.min
   t_{RP}=(tcyc/2 x 3-20)ns.min
   $t_{su(DB-CAS)}$=(tcyc-20)ns.min

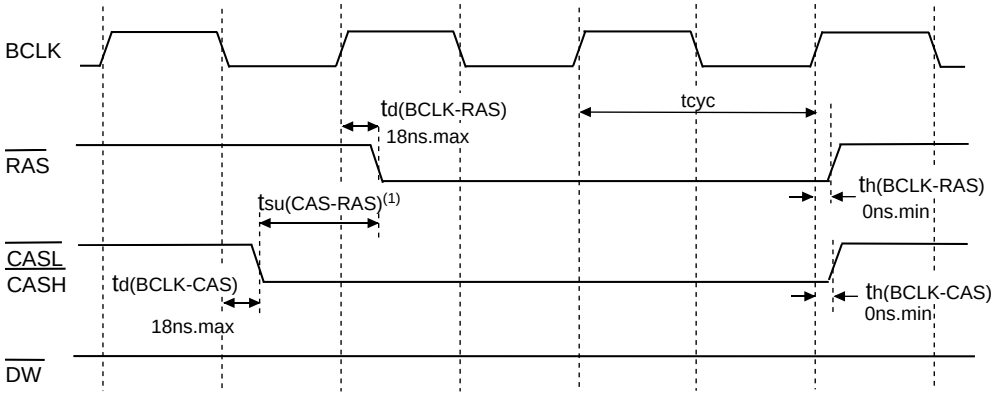
Measurement Conditions:

- V_{CC}=3.0 to 3.6V
- Input high and low voltage:
  V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage:
  V_{OH}=1.5V, V_{OL}=1.5V

Figure 5.14 V_{CC}=3.3V Timing Diagram (5)

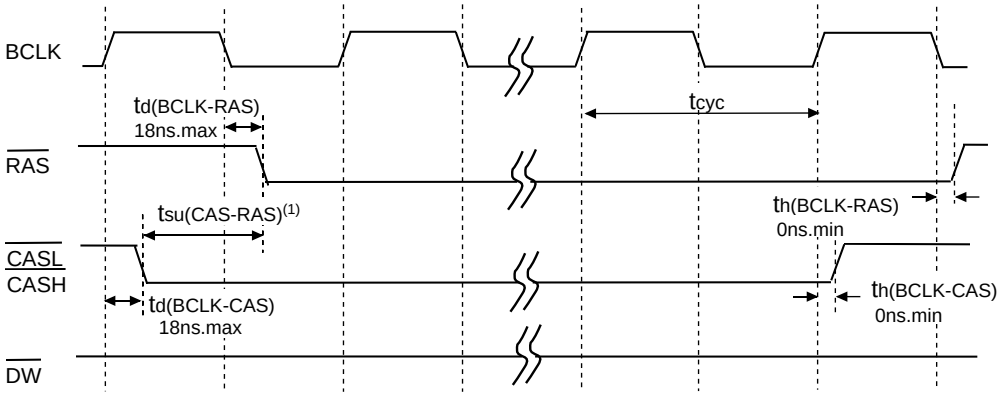
Vcc=3.3V

Memory Expansion Mode and Microprocessor Mode
Refresh Timing (CAS-before-RAS refresh)



NOTES:
1. Varies with operation frequency.
$t_{su(CAS-RAS)}$=(tcyc/2-13)ns.min

Refresh Timing (Self-refresh)



NOTES:
1. Varies with operation frequency.
$t_{su(CAS-RAS)}$=(tcyc/2-13)ns.min

Measurement Conditions:
- V_{CC}=3.0 to 3.6V
- Input high and low voltage: V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage: V_{OH}=1.5V, V_{OL}=1.5V

Figure 5.15 V_{CC}=3.3V Timing Diagram (6)

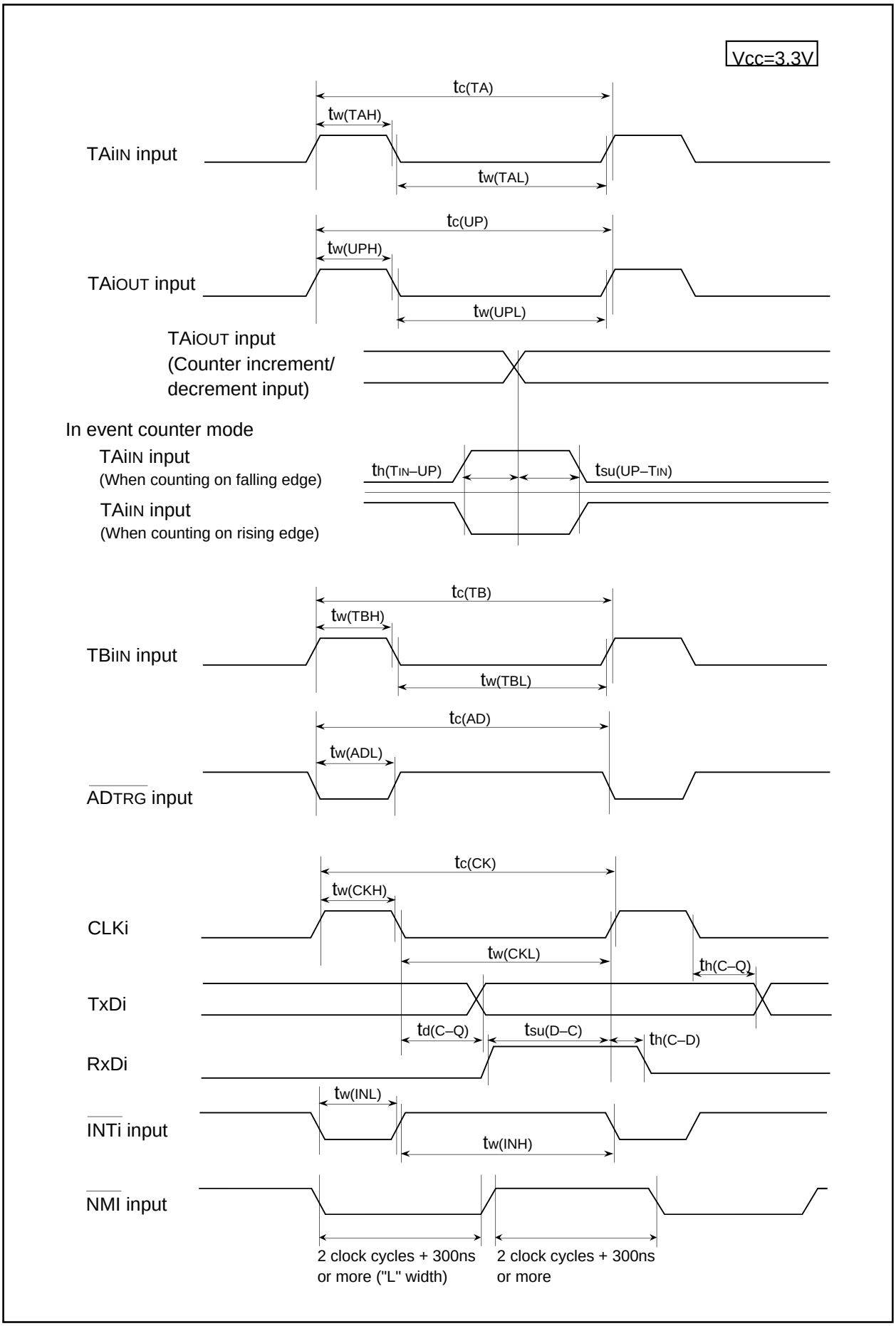
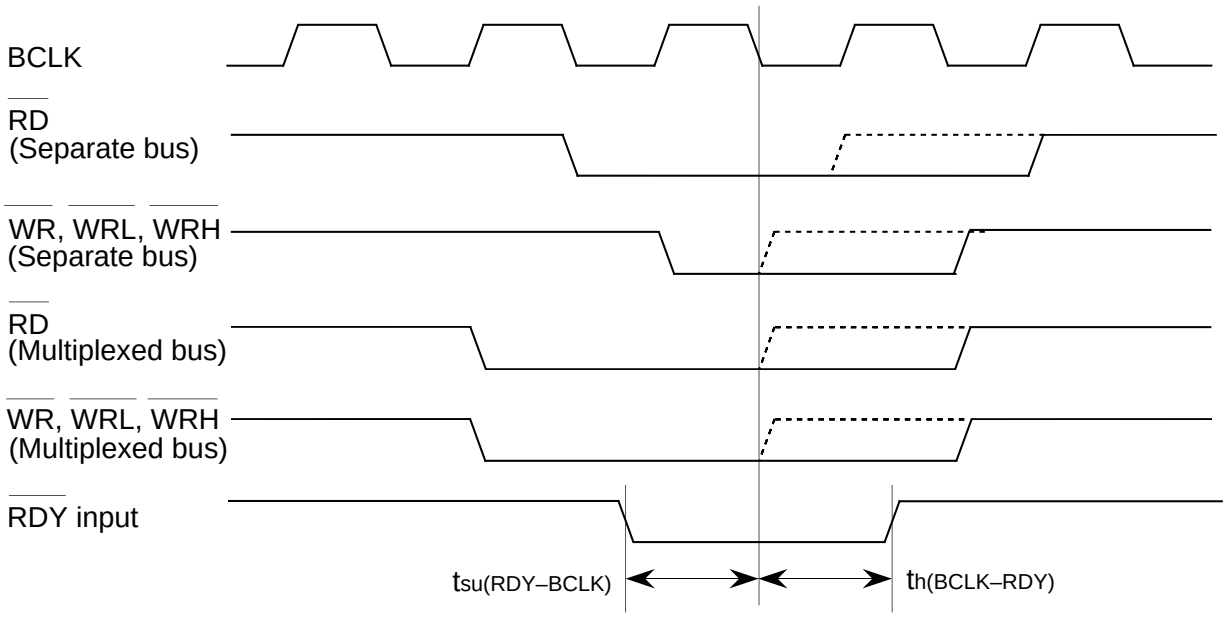


Figure 5.16 V_{CC}=3.3V Timing Diagram (7)

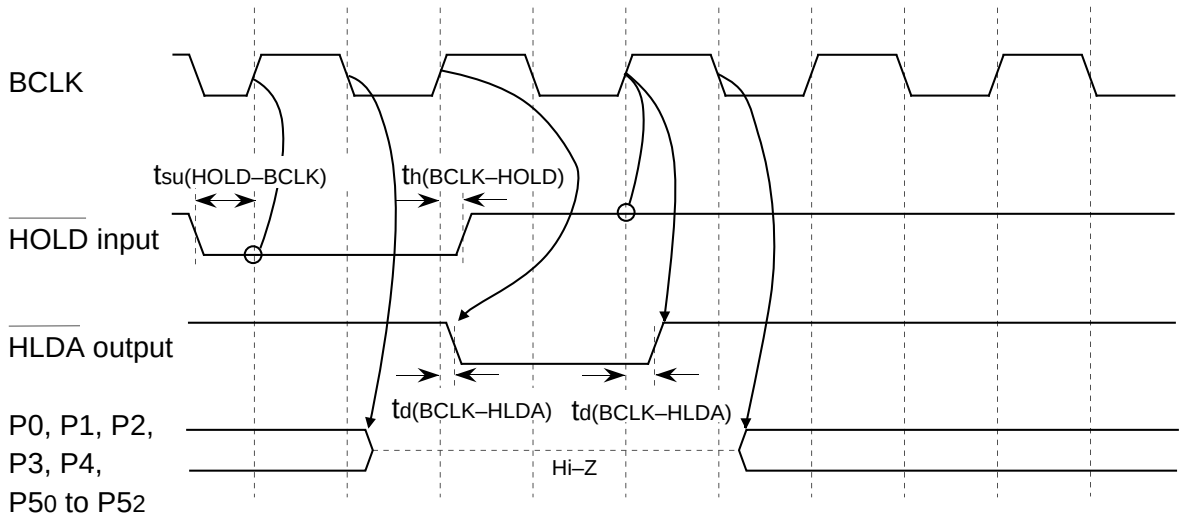
Vcc=3.3V

Memory Expansion Mode and Microprocessor Mode

(Valid only with a wait state)



(Valid with a wait state and no wait state)



Measurement Conditions:

- VCC=3.0 to 3.6V
- Input high and low voltage: V_{IH}=2.4V, V_{IL}=0.6V
- Output high and low voltage: V_{OH}=1.5V, V_{OL}=1.5V

Figure 5.17 V_{CC}=3.3V Timing Diagram (8)

5.2 Electrical Characteristics (M32C/83T)

Table 5.45 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
V_{CC}	Supply Voltage		V_{CC}=AV_{CC}	-0.3 to 6.0	V
AV_{CC}	Analog Supply Voltage		V_{CC}=AV_{CC}	-0.3 to 6.0	V
V_I	Input Voltage	$\overline{RESET}$, CNV_{SS}, BYTE, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), V_{REF}, X_{IN}		-0.3 to V_{CC}+0.3	V
		$P7_0$, $P7_1$		-0.3 to 6.0	V
V_O	Output Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{OUT}		-0.3 to V_{CC}+0.3	V
Pd	Power Dissipation		Topr=25° C	400	mW
Topr	Operating Ambient Temperature		T version	-40 to 85	° C
Tstg	Storage Temperature			-65 to 150	° C

NOTES:
1. P11 to P15 are provided in the 144-pin package.

Table 5.46 Recommended Operating Conditions

(Vcc=4.2 to 5.5V, Vss=0V at Topr = -40 to 85°C (T version) unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
Vcc	Supply Voltage		4.2	5.0	5.5	V
AVcc	Analog Supply Voltage			Vcc		V
Vss	Supply Voltage			0		V
AVss	Analog Supply Voltage			0		V
VIH	Input High ("H") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P87(3), P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(4), XIN, RESET, CNVss, BYTE	0.8Vcc		Vcc	V
		P70, P71	0.8Vcc		6.0	
VIL	Input Low ("L") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87(3), P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(4), XIN, RESET, CNVss, BYTE	0		0.2Vcc	V
IOH(peak)	Peak Output High ("H") Current(2)	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(4)			-10.0	mA
IOH(avg)	Average Output High ("H") Current(1)	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(4)			-5.0	mA
IOL(peak)	Peak Output Low ("L") Current(2)	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(4)			10.0	mA
IOL(avg)	Average Output Low ("L") Current(1)	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157(4)			5.0	mA
f(XIN)	Main Clock Input Frequency	Vcc=4.2 to 5.5V	0		32	MHz
f(XCIN)	Sub Clock Oscillation Frequency			32.768	50	kHz

NOTES:

1. Typical values when average output current is 100ms.
2. Total IOL(peak) for P0, P1, P2, P86, P87, P9, P10, P11, P14 and P15 must be 80mA or less.
   Total IOH(peak) for P0, P1, P2, P86, P87, P9, P10, P11, P14 and P15 must be -80mA or less.
   Total IOL(peak) for P3, P4, P5, P6, P7, P80 to P84, P12 and P13 must be 80mA or less.
   Total IOH(peak) for P3, P4, P5, P6, P72 to P77, P80 to P84, P12 and P13 must be -80mA or less.
3. VIH and VIL reference for P87 applies when P87 is used as a programmable input port.
   It does not apply when P87 is used as XCIN.
4. P11 to P15 are provided in the 144-pin package only.

VCC=5V

Table 5.47 Electrical Characteristics (V_{CC} = 4.2 to 5.5 V, V_{SS} = 0V at Topr = –40 to 85°C(T version), f(X_{IN})=32MHz unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit
				Min	Typ	Max	
V_{OH}	Output High ("H") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OH}=-5mA	V_{CC}-2.0			V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OH}=-200µA	V_{CC}-0.3			V
		X_{OUT}	I_{OH}=-1mA	3.0			V
		X_{COUT}	No load applied		3.3		V
V_{OL}	Output Low ("L") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=5mA			2.0	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=200µA			0.45	V
		X_{OUT}	I_{OL}=1mA			2.0	V
		X_{COUT}	No load applied		0		V
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$-$TA4_{IN}$, $TB0_{IN}$-$TB5_{IN}$, $\overline{INT0}$-$\overline{INT5}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, $TA0_{OUT}$-$TA4_{OUT}$, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		$\overline{RESET}$		0.2		1.8	V
I_{IH}	Input High ("H") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=5V			5.0	µA
I_{IL}	Input Low ("L") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=0V			-5.0	µA
R_{PULLUP}	Pull-up Resistance	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	V_I=0V	30	50	167	kΩ
Rf_{XIN}	Feedback Resistance	X_{IN}			1.5		MΩ
Rf_{XCIN}	Feedback Resistance	X_{CIN}			10		MΩ
V_{RAM}	RAM Standby Voltage			2.5			V
I_{CC}	Power Supply Current	Measurement conditions: In single-chip mode, output pins are left open and other pins are connected to V_{SS}	f(X_{IN})=32 MHz, square wave, no division		40	54	mA
			f(X_{CIN})=32 kHz, with a wait state, Topr=25° C		470		µA
			Topr=25° C when the clock stops		0.4	20	µA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

V_{CC}=5V

Table 5.48 A/D Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 4.2 to 5.5V, Vss = AV_{SS} = 0V at Topr = –40 to 85°C (T version), f(X_{IN}) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min	Typ	Max	
-	Resolution	V_{REF}=V_{CC}				10	Bits
INL	Integral Nonlinearity Error	V_{REF}=V_{CC}=5V	AN_0 to AN_7 $ANEX_0$, $ANEX_1$			±3	LSB
							LSB
			External op-amp connection mode			±7	LSB
							LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
R_{LADDER}	Resistor Ladder	V_{REF}=V_{CC}		8		40	kΩ
t_{CONV}	10-bit Conversion Time			2.1			µs
t_{CONV}	8-bit Conversion Time			1.8			µs
t_{SAMP}	Sample Time			0.2			µs
V_{REF}	Reference Voltage			2		V_{CC}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

NOTES:
1. Divide f(X_{IN}), if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.

Table 5.49 D/A Conversion Characteristics (V_{CC} = V_{REF} = 4.2 to 5.5V, V_{SS} = AV_{SS} = 0V at Topr = –40 to 85°C (T version), f(X_{IN}) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:
1. Measurement results when using one D/A converter. The DAi register (i=0, 1) of the D/A converter not being used is set to "00_{16}". The resistor ladder in the A/D converter is exclued. I_{VREF} flows even if the VCUT bit in the ADiCON1 register is set to "0" (no V_{REF} connection).

Table 5.50 Flash Memory Version Electrical Characteristics

Parameter	Standard			Unit
	Min	Typ	Max	
Program Time (per page)		8	120	ms
Block Erase Time (per block)		50	600	ms

NOTES:
1. V_{CC}= 4.2 to 5.5V at Topr= 0 to 60° C, unless otherwise specified

VCC=5V

Timing Requirements (VCC = 4.2 to 5.5V, VSS = 0V at Topr = –40 to 85°C (T version) unless otherwise specified)

Table 5.51 External Clock Input

Symbol	Parameter	Standard		Unit
		Min	Max	
tc	External Clock Input Cycle Time	33		ns
$t_{w(H)}$	External Clock Input High ("H") Pulse Width	13		ns
$t_{w(L)}$	External Clock Input Low ("L") Pulse Width	13		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

VCC=5V

Timing Requirements

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –40 to 85°C (T version) unless otherwise specified)

Table 5.52 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	100		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	40		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	40		ns

Table 5.53 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	400		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	200		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	200		ns

Table 5.54 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	200		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	100		ns

Table 5.55 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Pulse Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Pulse Width	100		ns

Table 5.56 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(UP)}$	TAi_{OUT} Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} Input High ("H") Pulse Width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} Input Low ("L") Pulse Width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} Input Hold Time	400		ns

VCC=5V

Timing Requirements

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = –40 to 85°C (T version) unless otherwise specified)

Table 5.57 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Pulse Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Pulse Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Pulse Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Pulse Width (counted on both edges)	80		ns

Table 5.58 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Pulse Width	200		ns

Table 5.59 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Pulse Width	200		ns

Table 5.60 A/D Trigger Input

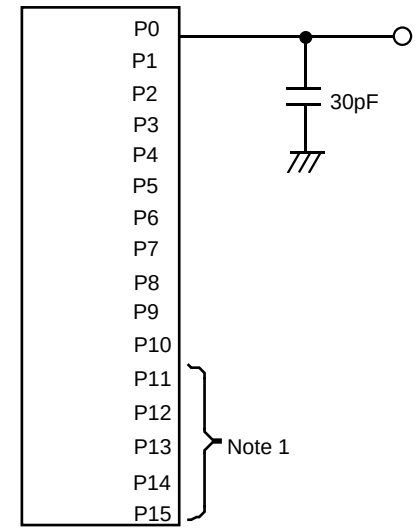
Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time (required for re-trigger)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ Input Low ("L") Pulse Width	125		ns

Table 5.61 Serial I/O

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Pulse Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Pulse Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Set Up Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 5.62 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min	Max	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Pulse Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Pulse Width	250		ns



NOTES:

1. P11 to P15 are provided in the 144-pin package only.

Figure 5.18 P0 to P15 Measurement Circuit

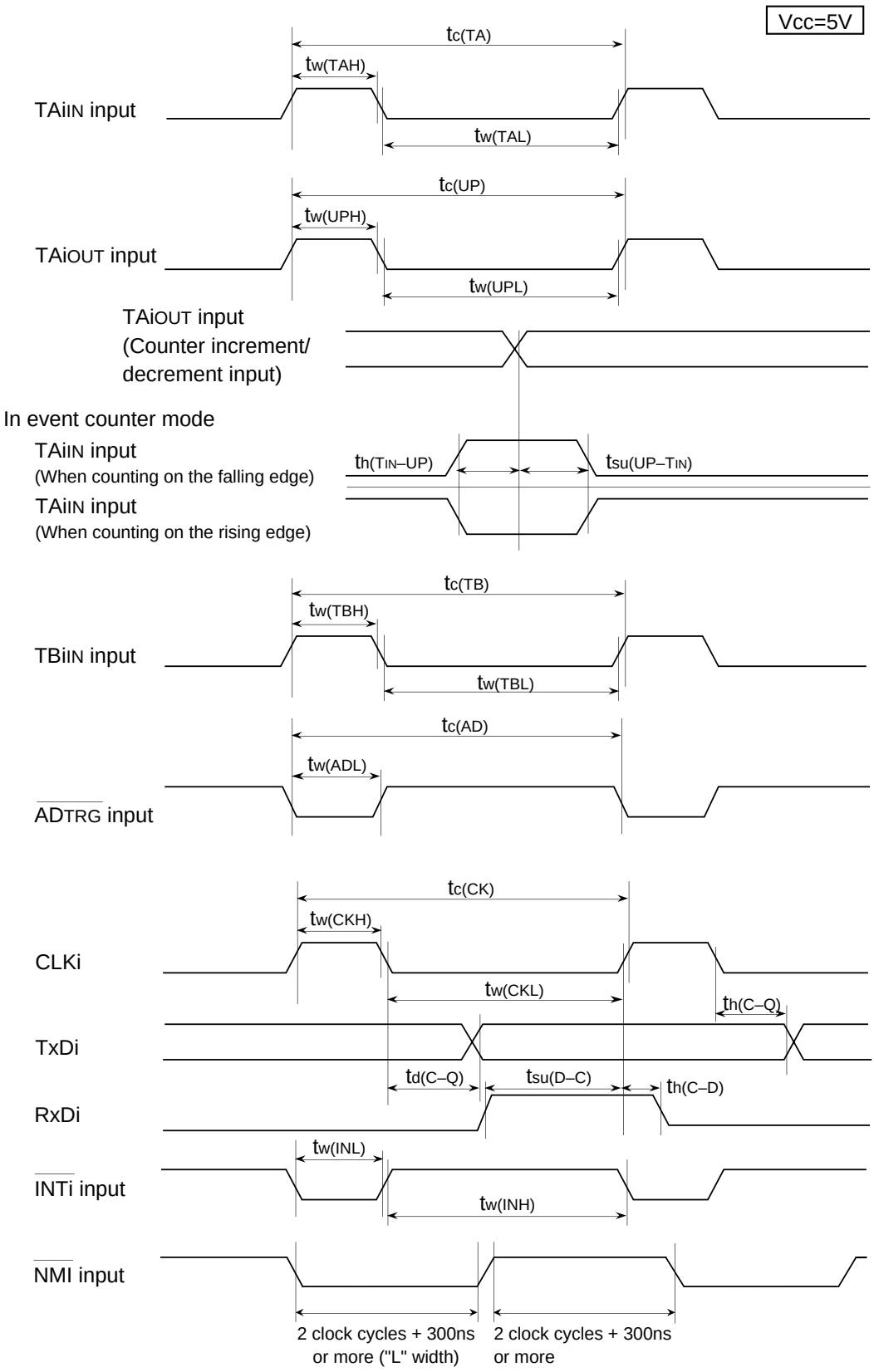


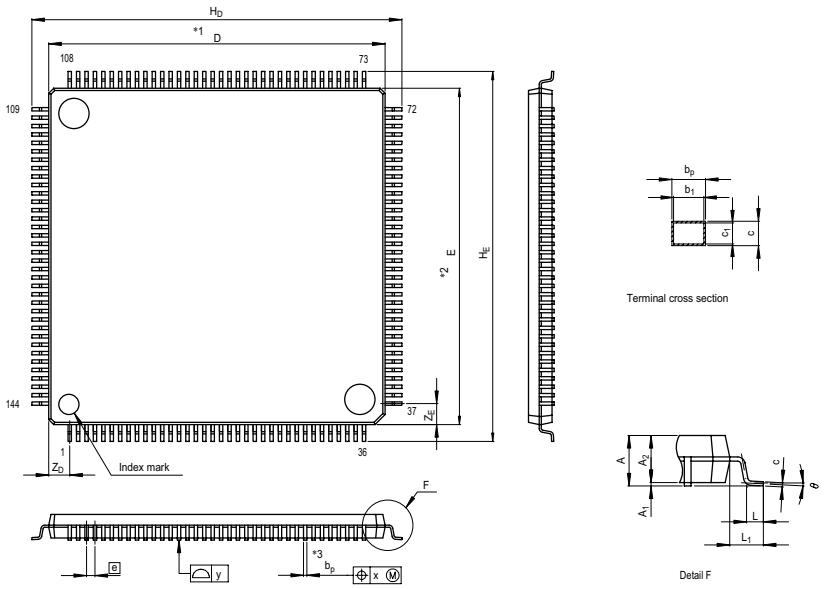
Figure 5.19 VCC = 5 V Timing Diagram(1)

Package Dimensions

PLQ0144KA-A (144P6Q-A)

Plastic 144pin 20 X 20 mm body LQFP

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g



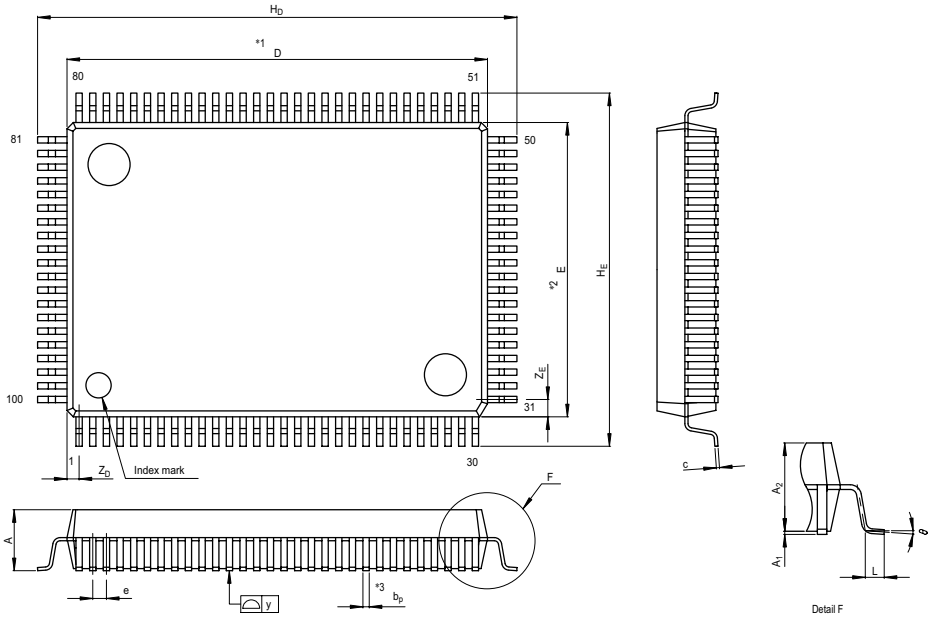
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

PRQP0100JB-A (100P6S-A)

Plastic 100pin 14 X 20 mm body LQFP

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x20-0.65	PRQP0100JB-A	100P6S-A	1.6g



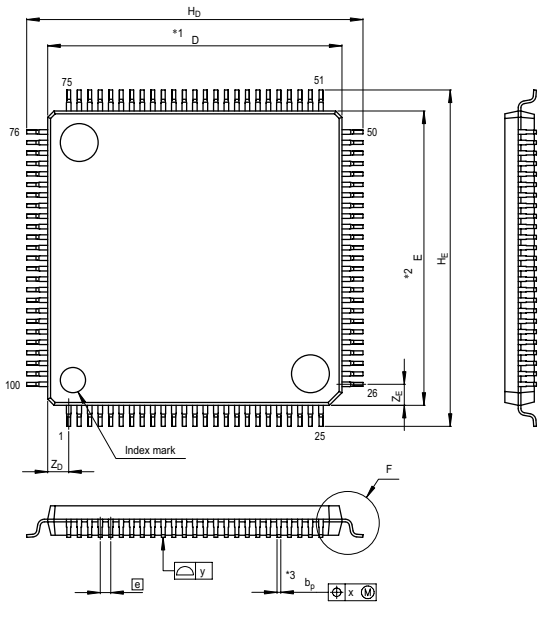
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

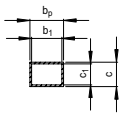
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	0.5	0.65	0.8
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.825	—
L	0.4	0.6	0.8

PLQP0100KB-A (100P6Q-A)

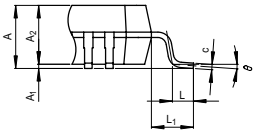
Plastic 100pin 14 X 14 mm body LQFP

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

REVISION HISTORY	M32C/83 GROUP (M32C/83, M32C/83T) Datasheet

Rev.	Date	Description	
		Page	Summary
1.10	**2003-9**	-	New Document
1.20	**2003-12**		Maximum operating frequency changed from 30 MHz to 32 MHz. Overview, Electrical Characteristics Table 1.1 M32C/83 Group Performance (144-Pin Package) Table 1.2 M32C/83 Group Performance (100-Pin Package) Table 5.2 Recommended Operating Conditions Table 5.3 Electrical Characteristics
1.30	**2004-06**	All pages	Words standardized: On-chip oscillator, A/D converter and D/A converter
1.41	**2006-01**	All Pages	**M32C/83T version** added; Package code changed: 144P6Q-A to PLQP0144KA-A, 100P6Q-A to PLQP0100KB-A, 100P6S-A to PRQP0100JB-A
		All Pages	Word standardized: Clock Generation Circuit , On-chip Oscillator, A/D Converter, D/A Converter, XY Conversion, Low -power consumption
			Overview
		1	• **1.1 Applications** Automobile added
		2, 3	• **Tables 1.1 and 1.2 M32C/83 Group (M32C/83, M32C/83T) Performance**
		5	• **Table 1.3 M32C/83 Group (1) (M32C/83)** Information updated
			• **Table 1.3 M32C/83 Group (2) (M32C/83T)** M32C/83T product information added
			• **Figure 1.2 Product Numbering System** Classification modified
			• **Table 1.4 Pin Characteristics for 144-Pin Package** Note 1 added
			• **Table 1.5 Pin Characteristics for 100-Pin Package** Note 1 added
			• **Table 1.6 Pin Description** modified, notes added
			Memory
		21	• **Figure 3.1 Memory Map** modified; Note 2 modified, notes 3 and 4 added
			Special Function Registers (SFR)
		22 to 23	• Note 2 added
			Reset
		45	• **Figure 5.2 Reset Sequence** Note 2 added
			Electrical Characteristics
		46	• **Table 5.3 Electrical Characteristics** Minimum standard values for V_{OH} revised, values for I_{CC} when f(X_{IN})=32 MHz, square wave, no division revised, one condition of "f(X_{IN})=32 MHz, square wave, no division" deleted
		54	• **Table 5.23 Memory Expansion Mode and Microprocessor Mode** Symbols for Row Address Output Delay Time and for Row Address Output Hold Time (BCLK standard) modified
		62	• **Figure 5.8 V_{CC}=5 V Timing Diagram (7)** Timing for $\overline{NMI}$ input added
		64	• **Table 5.24 Electrical Characteristics** Minimum standard value for V_{OH} revised

REVISION HISTORY	M32C/83 GROUP (M32C/83, M32C/83T) Datasheet

Rev.	Date	Description	
		Page	Summary
		72	• **Table 5.44 Memory Expansion Mode and Microprocessor Mode** Symbols for Row Address Output Delay Time and for Row Address Output Hold Time (BCLK standard) modified
		79	• **Figure 5.8 Vcc=3.3 V Timing Diagram (7)** Timing for $\overline{\text{NMI}}$ input added
		81-89	• **5.2 Electrical Characteristics (M32C/83T)** Newly added

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