1.25 GHz Dual Integrated DCL with PPMU, Level Setting DACs, and On-Chip Calibration Registers

Data Sheet

ADATE320

FEATURES

- 1.25 GHz, 2.5 Gbps data rate
- 3-level driver with high-Z and reflection clamps
- Window and differential comparators
- ±25 mA active load
- Per pin parametric measurement unit (PMU) with a −1.5 V to +4.5 V range
- Low leakage mode (typically <5 nA)
- Integrated 16-bit DACs with offset and gain correction
- 1.2 W power dissipation per channel (ADATE320)
- 1.3 W power dissipation per channel (ADATE320-1)
- Driver
  - Voltage range: −1.5 V to +4.5 V
  - Precision trimmed termination: 50.0 Ω
  - Unterminated swing: 50 mV minimum to 6.0 V maximum
  - 400 ps minimum pulse width, 1.0 V programmed swing
  - 25 ps deterministic jitter
- Comparator
  - Differential and single-ended window modes
  - 100 ps equivalent input rise/fall time (ERT/EFT)
  - 250 mV current mode logic (CML) outputs (ADATE320)
  - 400 mV CML outputs (ADATE320-1)
- Load
- Per pin PMU (PPMU)
  - Force voltage/compliance range: −1.5 V to +4.5 V
  - 5 current ranges
    - ±40 mA, ±1 mA, ±100 µA, ±10 µA, ±2 µA
  - Dedicated go/no-go comparators
- DC levels
  - Fully integrated and dedicated 16-bit DACs
  - On-chip gain and offset calibration registers with automatic add/multiply function
- 84-lead, 10 mm × 10 mm LFCSP (0.4 mm pitch)

APPLICATIONS

- Automatic test equipment (ATE)
- Semiconductor/board test systems
- Instrumentation and characterization equipment

GENERAL DESCRIPTION

The ADATE320 is a complete, single-chip ATE solution that performs the pin electronics functions of a driver, comparator, and active load (DCL), and a four quadrant per pin parametric measurement unit (PPMU). Dedicated 16-bit digital-to-analog converters (DACs) with on-chip calibration registers provide all the necessary dc levels for operation of the device.

The driver features three active modes: high, low, and terminate, as well as a high impedance inhibit state. The inhibit state, in conjunction with the integrated dynamic clamps, facilitates significant attenuation of transmission line reflections when the driver is not actively terminating the line. The open-circuit drive capability is −1.5 V to +4.5 V to accommodate a standard range of ATE and instrumentation applications.

The ADATE320 can be used as a dual, single-ended pin electronics channel or as a single differential channel. In addition to per channel high speed window comparators, the ADATE320 provides a programmable threshold differential comparator for differential ATE applications.

All dc levels for DCL and PPMU functions are generated by dedicated, on-chip, 16-bit DACs. To facilitate the programming of accurate levels, the ADATE320 includes an integrated calibration function to correct for the gain and offset errors of each functional block. Correction coefficients can be stored on chip, and any values written to the DACs adjust automatically using the appropriate correction factors.

The ADATE320 uses a serial programmable interface (SPI) bus to program all functional blocks, DACs, and on-chip calibration constants. It also has an on-chip temperature sensor and overvoltage/undervoltage fault clamps that monitor and report the device temperature and any output pin or transient PPMU voltage faults that may occur during operation.

The ADATE320 is available in two options. The standard option has high speed comparator outputs with 250 mV output swing. The ADATE320-1 has 400 mV output swing. See the Ordering Guide for more information.

Rev. B
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

ADATE320* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Data Sheet

- ADATE320: 1.25 GHz Dual Integrated DCL with PPMU, Level Setting DACs, and On-Chip Calibration Registers Data Sheet

DESIGN RESOURCES

- ADATE320 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADATE320 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

9/2016—Rev. A to Rev. B

Changes to Time Constant 1 Parameter and Time Constant 2 Parameter, Table 2 ... 7
Changes to IOx Offset Parameter, and IOHx Offset Parameter, Table 6 ... 11
Change to AGND Pin Number Column ... 29
Change to SPI Reset Sequence and the $\overline{\text{RST}}$ Pin Section ... 50
Changes to the SPI Clock Cycles and $\overline{\text{BUSY}}$ Pin Section ... 51
Changes to Table 24 ... 54
Changes to Figure 137 ... 65

10/2015—Revision A: Initial Version

FUNCTIONAL BLOCK DIAGRAM

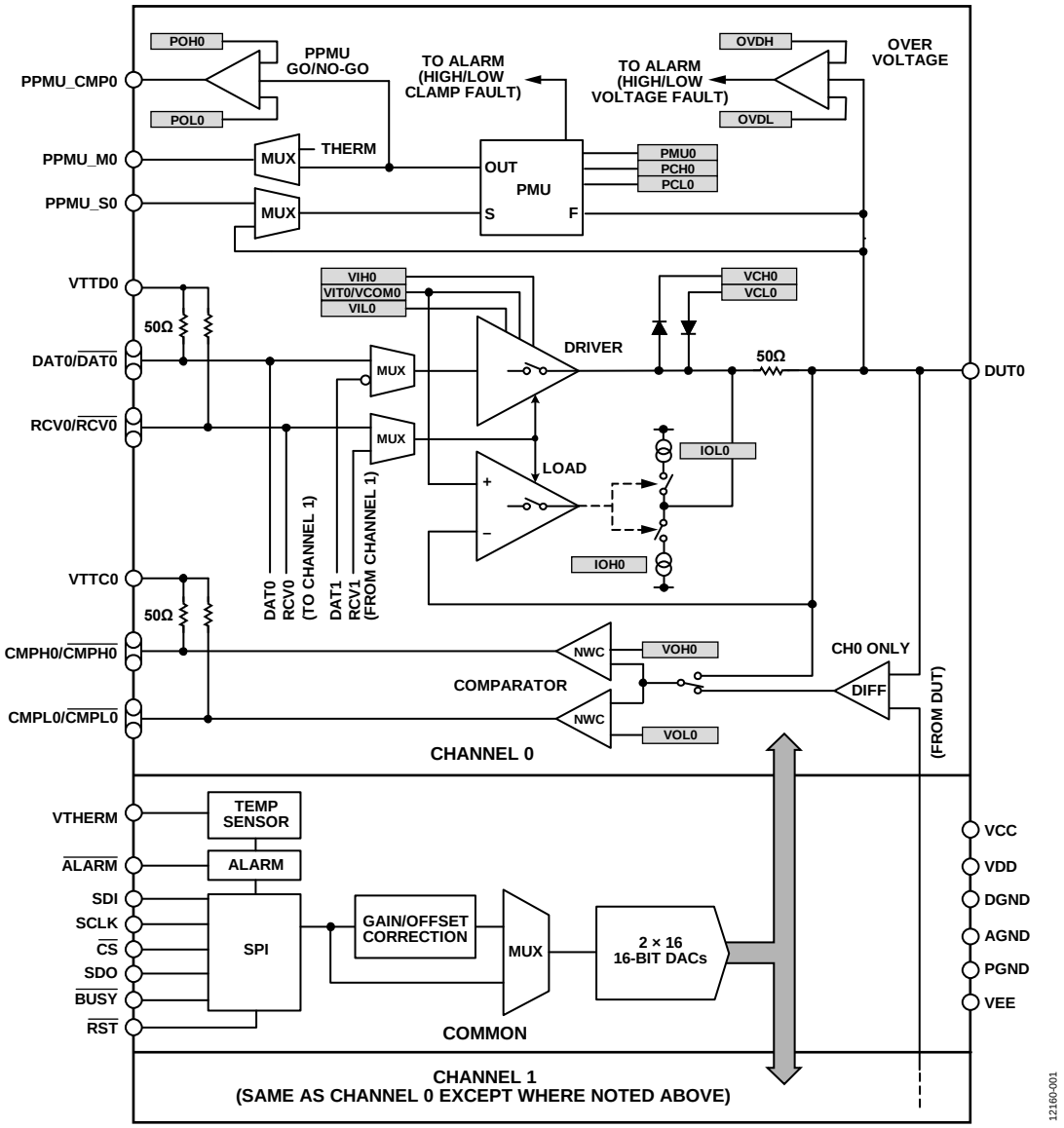


Figure 1.

SPECIFICATIONS

V_{CC} = 8.0 V, V_{DD} = 1.8 V, V_{EE} = −5.0 V, V_{TTCx} = V_{TTDx} = 1.2 V, V_{REF} = 2.500 V, V_{REFGND} = 0.000 V. All default test conditions are as defined in Table 30. All specified values are at T_J = 60°C, where T_J corresponds to the typical internal temperature sensor reading (VTHERM pin), unless otherwise noted. Temperature coefficients are measured around T_J = 40°C, 60°C, 80°C, and 100°C. Typical values are based on the statistical mean of the design, simulation analyses, and/or limited bench evaluation data. Typical values are neither tested nor guaranteed. Test level codes are defined in the Explanation of Test Levels section.

ELECTRICAL SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DUTx PIN CHARACTERISTICS						
Output Leakage Current						
DCL Disable						
PPMU Range E	−10.0	+5.0	+10.0	nA	P	−1.5 V < V_{DUTx} < +4.5 V, PPMU and DCL disabled, PPMU Range E, VCLx = −2.5 V, VCHx = +7.5 V
PPMU Range A to Range D		5.0		nA	C_T	−1.5 V < V_{DUTx} < +4.5 V, PPMU and DCL disabled, PPMU Range A, Range B, Range C, and Range D, VCLx = −2.5 V, VCHx = +7.5 V
Driver High-Z Mode	−0.4		+0.4	µA	P	−1.5 V < V_{DUTx} < +4.5 V, PPMU disabled and DCL enabled, RCV active, VCLx = −2.5 V, VCHx = +7.5 V
Capacitance		0.4		pF	S	Drive VITx = 0.0 V
Voltage Range	−1.5		+4.5	V	D	
POWER SUPPLIES						Power measured with the DUTx pin high-Z, 10 K to 0.0 V
Positive DCL Supply, V_{CC}	7.6	8.0	8.4	V	D	Defines dc power supply rejection (PSR) conditions
Negative DCL Supply, V_{EE}	−5.25	−5.0	−4.75	V	D	Defines dc PSR conditions
Digital Supply, V_{DD}	1.7	1.8	1.9	V	D	
Comparator Termination, V_{TTCx}	0.5	1.2	1.8	V	D	VTTC0 is not electrically connected to VTTC1
Driver Termination, V_{TTDx}	0.0	1.2	1.8	V	D	VTTD0 is not electrically connected to VTTD1
Positive DCL Supply Current, I_{CC}						Load and PPMU power-down
ADATE320	145	169	185	mA	P	
ADATE320-1	145	169	185	mA	P	
Negative DCL Supply Current, I_{EE}						Load and PPMU power-down
ADATE320	190	222	235	mA	P	
ADATE320-1	220	247	265	mA	P	
Digital Core Supply Current, I_{DD}	−125	+10	+125	µA	P	Quiescent (SPI is static)
Comparator Termination Supply Current, V_{TTCx}						0.5 V ≤ V_{TTCx} ≤ 1.8 V
ADATE320		41		mA	C_T	
ADATE320-1		66		mA	C_T	
Driver Termination Supply Current, V_{TTDx}		0		mA	C_T	0.0 V ≤ V_{TTDx} ≤ 1.8 V, (DATx + $\overline{DATx}$)/2 = (RCVx + $\overline{RCVx}$)/2 = V_{TTDx}
Total Power Dissipation						Load and PPMU power-down
ADATE320	2.10	2.52	2.75	W	P	
ADATE320-1	2.25	2.66	2.90	W	P	

DRIVER SPECIFICATIONS

VIH − VIL ≥ 100 mV to meet dc and ac performance specifications.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DC SPECIFICATIONS						
High Speed Differential Input Characteristics						
High Speed Input Termination Resistance: DATx/$\overline{\text{DATx}}$, RCVx/$\overline{\text{RCVx}}$	48	50	52	Ω	P	Impedance between VTTDx and respective DATx and RCVx pins; force 4 mA into each pin, measure voltage from VTTDx; calculate resistance (ΔV/ΔI)
Input Voltage Range: DATx/$\overline{\text{DATx}}$, RCVx/$\overline{\text{RCVx}}$	0.0		1.8	V	P_F	
Input Voltage Differential	0.2	0.4	1.0	V	P_F	|DATx − $\overline{\text{DATx}}$|, |RCVx − $\overline{\text{RCVx}}$|
Output Characteristics						
Output Range						
High, VIH	−1.4		+4.5	V	D	
Low, VIL	−1.5		+4.4	V	D	
Output Term Range, VIT	−1.5		+4.5	V	D	
Functional Amplitude (VIH − VIL)	0.05		6.0	V	D	
DC Output Current Limit						
Source	75		120	mA	P	Drive high, VIH = 4.5 V, V_{DUTx} = −2.0 V, measure current
Sink	−120		−75	mA	P	Drive low, VIL = −1.5 V, V_{DUTx} = 5.0 V, measure current
Output Resistance, ±40 mA	46	48.5	52	Ω	P	$\Delta V_{DUTx}/\Delta I_{DUTx}$; source: VIHx = 3.0 V, I_{DUTx} = 1 mA, 40 mA; sink: VIL = 0.0 V, I_{DUTx} = −1 mA, −40 mA
DC ACCURACY						VIH tests with VIL = −2.5 V, VIT = −2.5 V; VIL tests with VIH = 7.5 V, VIT = 7.5 V; VIT tests with VIL = −2.5 V, VIH = 7.5 V, unless otherwise noted within this parameter
VIH, VIL, VIT						
Offset Error	−500		+500	mV	P	Measured at DAC Code 0x4000 (0.0 V), uncalibrated
Offset Temperature Coefficient (TC)		±200		µV/°C	C_T	
Gain	1.0		1.1	V/V	P	Gain derived from measurement at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V); based on an ideal DAC transfer function (see Table 24)
Gain TC		±50		ppm/°C	C_T	
Differential Nonlinearity (DNL)		±250		µV	C_T	After two-point gain/offset calibration; calibration points at 0x4000 (0.0 V) output; 0x8CCC (3.0 V); measured over full specified output range
Integral Nonlinearity (INL) Focused Range	−5		+5	mV	P	After two-point gain/offset calibration; calibration points at 0x4000 (0.0 V) and 0x8CCC (3.0 V); measured over −0.5 V to +3.5 V output range
INL Full Range	−20		+20	mV	P	After two-point gain/offset calibration; calibration points at 0x4000 (0.0 V) and 0x8CCC (3.0 V); measured over full specified output range
Resolution		153		µV	D	
DUTGND Voltage Accuracy	−5	±1	+5	mV	P	Over ±0.1 V range; measured over −0.5 V to +3.5 V focused driver output range
DC Levels Interaction						DC interaction on VIL, VIH, and VIT output levels while other driver DAC levels are varied
VIH vs. VIL		±1.0		mV	C_T	Monitor interaction on VIH = +4.5 V; sweep VIL = −1.5 V to +4.4 V, VIT = +1.0 V
VIH vs. VIT		±1.0		mV	C_T	Monitor interaction on VIH = +4.5 V; sweep VIT = −1.5 V to +4.5 V, VIL = 0.0 V
VIL vs. VIH		±1.0		mV	C_T	Monitor interaction on VIL = −1.5 V; sweep VIH = −1.4 V to +4.5 V, VIT = +1.0 V

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
VIL vs. VIT		±1.0		mV	C_T	Monitor interaction on VIL = −1.5 V; sweep VIT = −1.5 V to +4.5 V, VIH = +2.0 V
VIT vs. VIH		±2.0		mV	C_T	Monitor interaction on VIT = 1.0 V; sweep VIH = −1.4 V to +4.5 V, VIL = −1.5 V
VIT vs. VIL		±2.0		mV	C_T	Monitor interaction on VIT = 1.0 V; sweep VIL = −1.5 V to +4.4 V, VIH = +4.5 V
Overall Voltage Accuracy Focused Range		±5		mV	C_T	VIH − VIL ≥ 100 mV; sum of INL, dc interaction, DUTGND and TC errors over ±5°C, after calibration
VIH, VIL, VIT DC PSR		+15		mV/V	C_T	Measured at calibration points, see Table 1 for power supply ranges
AC SPECIFICATIONS						All ac specifications performed after dc calibration
Rise/Fall Times						Toggle DATx, VIL = 0.0 V, terminated
0.2 V Programmed Swing						
t_{RISE}		150		ps	C_B	20% to 80%, VIH = 0.2 V
t_{FALL}		170		ps	C_B	20% to 80%, VIH = 0.2 V
0.5 V Programmed Swing						
t_{RISE}		150		ps	C_B	20% to 80%, VIH = 0.5 V
t_{FALL}		170		ps	C_B	20% to 80%, VIH = 0.5 V
1.0 V Programmed Swing						
t_{RISE}		150		ps	C_B	20% to 80%, VIH = 1.0 V
t_{FALL}		170		ps	C_B	20% to 80%, VIH = 1.0 V
2.0 V Programmed Swing						
t_{RISE}	120	160	230	ps	P	20% to 80%, VIH = 2.0 V
t_{FALL}	120	180	230	ps	P	20% to 80%, VIH = 2.0 V
4.0 V Programmed Swing						
t_{RISE}		320		ps	C_B	10% to 90%, VIH = 4.0 V, unterminated
t_{FALL}		320		ps	C_B	10% to 90%, VIH = 4.0 V, unterminated
t_{RISE} to t_{FALL} Mismatch		−20		ps	C_B	$t_{RISE} - t_{FALL}$ (20% to 80%) within one channel, VIH = 2.0 V, VIL = 0.0 V, terminated
Trailing Edge Timing Error						Toggle DATx
Programmed Swing						VIL = 0.0 V, terminated, 400 ps ≤ pulse width (PW) ≤ 10 ns
0.2 V		±15		ps	C_B	VIH = 0.2 V
0.5 V		±15		ps	C_B	VIH = 0.5 V
1.0 V		±15		ps	C_B	VIH = 1.0 V
2.0 V		±15		ps	C_B	VIH = 2.0 V
Maximum Toggle Rate						Toggle DATx
Programmed Swing						VIL = 0.0 V, terminated ≤10% amplitude loss
0.2 V		2.8		Gbps	C_B	VIH = 0.2 V
0.5 V		3.2		Gbps	C_B	VIH = 0.5 V
1.0 V		3.2		Gbps	C_B	VIH = 1.0 V
2.0 V		2.8		Gbps	C_B	VIH = 2.0 V
Dynamic Performance						Toggle DATx, drive VIL to/from VIH
Propagation Delay						VIH = 2.0 V, VIL = 0.0 V, terminated
Time		750		ps	C_B	
TC		2		ps/°C	C_T	
Delay Matching						VIH = 2.0 V, VIL = 0.0 V, terminated
Edge to Edge		10		ps	C_B	$t_{LH0} - t_{HL0}$; $t_{LH1} - t_{HL1}$
Channel to Channel		35		ps	C_B	$t_{LH0} - t_{LH1}$; $t_{HL0} - t_{HL1}$
Delay Change vs. Duty Cycle		±7		ps	C_B	VIH = 2.0 V, VIL = 0.0 V, terminated, 1 MHz, 5% to 95%
Overshoot and Undershoot		50		mV	C_B	VIH = 2.0 V, VIL = 0.0 V, terminated, minimum driver CLC
Settling Time (VIH to VIL)						Toggle DATx
To Within 3% of Final Value		1		ns	C_B	VIH = 2.0 V, VIL = 0.0 V, from 50% crossing, terminated
To Within 1% of Final Value		10		ns	C_B	VIH = 2.0 V, VIL = 0.0 V, from 50% crossing, terminated

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
Dynamic Performance						
Drive Active to/from VIT						Toggle RCVx, VIH = 2.0 V, VIT = 1.0 V, VIL = 0.0 V, terminated
Transition Time						20% to 80%
Active to VIT		200		ps	C_B	
VIT to Active		170		ps	C_B	
Propagation Delay		1.0		ns	C_B	
TC		2		ps/°C	C_T	
Drive Active to/from Inhibit						Toggle RCVx, VIH = 1.0 V, VIL = −1.0 V, terminated
Transition Time						20% to 80%
Inhibit to Active		250		ps	C_B	
Active to Inhibit		850		ps	C_B	
Propagation Delay						
Inhibit to VIH		2.1		ns	C_B	
Inhibit to VIL		2.5		ns	C_B	
Matching Inhibit to VIL vs. Inhibit to VIH		0.4		ns	C_B	
VIH to Inhibit		2.5		ns	C_B	
VIL to Inhibit		2.1		ns	C_B	
Input/Output Spike		125		mV p-p	C_B	VIH = 0.0 V, VIL = 0.0 V, terminated, toggle RCVx
Cable Loss Compensation (CLC)						VIH = 2.0 V, VIL = 0.0 V, terminated
Amplitude		20		%	C_B	Maximum CLC setting
Resolution		3		Bits	D	
Time Constant 1		400		ps	S	Maximum CLC setting
Time Constant 2		1.5		ns	S	Maximum CLC setting

REFLECTION CLAMP SPECIFICATIONS

Clamp accuracy specifications apply only when VCHx − VCLx > 0.8 V.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
VCH						
Functional Range	−0.5		+5.0	V	D	
Offset Error	−300		+300	mV	P	Driver high-Z, sinking 1 mA, measured at DAC Code 0x4000 (0.0 V), uncalibrated
Offset TC		±0.25		mV/°C	C_T	
Gain	1.0		1.1	V/V	P	Driver high-Z, sinking 1 mA, gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V), based on an ideal DAC transfer function (see Table 24)
Gain TC		±25		ppm/°C	C_T	
Resolution		153		µV	D	
DNL		±250		µV	C_T	Driver high-Z, sinking 1 mA, after two-point gain/offset calibration; calibration points at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V), measured over the functional range
INL	−20		+20	mV	P	Driver high-Z, sinking 1 mA, after two-point gain/offset calibration; calibration points at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V), measured over the functional range
VCL						
Functional Range	−2.0		+3.5	V	D	
Offset Error	−300		+300	mV	P	Driver high-Z, sourcing 1 mA, measured at DAC Code 0x4000 (0.0 V), uncalibrated
Offset TC		±0.25		mV/°C	C_T	

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
Gain	1.0		1.1	V/V	P	Drive high-Z, sourcing 1 mA, gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V), based on an ideal DAC transfer function (see Table 24)
Gain TC		±25		ppm/°C	C_T	
Resolution		153		µV	D	
DNL		±250		µV	C_T	Drive high-Z, sourcing 1 mA, after two-point gain/offset calibration; calibration points at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V), measured over the functional range
INL	−20		+20	mV	P	Drive high-Z, sourcing 1 mA, after two-point gain/offset calibration; calibration points at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V), measured over the functional range
DC CLAMP CURRENT LIMIT						Drive high-Z
VCHx	−105		−60	mA	P	VCHx = −1.0 V, VCLx = −2.0 V, V_{DUTx} = 4.5 V
VCLx	+60		+105	mA	P	VCHx = 5.0 V, VCLx = 4.0 V, V_{DUTx} = −1.5 V
DUTGND VOLTAGE ACCURACY	−10	±2	+10	mV	P	Over ±0.1 V range, measured at end points of VCHx and VCLx functional range

NORMAL WINDOW COMPARATOR (NWC) SPECIFICATIONS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DC SPECIFICATIONS						
Input Voltage Range	−1.5		+4.5	V	D	
Differential Voltage Range	±0.1		±6.0	V	D	
Input Offset Voltage	−250		+250	mV	P	Measured at DAC Code 0x4000 (0.0 V); uncalibrated
Input Offset Voltage TC		±150		µV/°C	C_T	
Gain	1.0		1.1	V/V	P	Gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V); based on an ideal DAC transfer function (see Table 24)
Gain TC		±10		ppm/°C	C_T	
Threshold Resolution		153		µV	D	
Threshold DNL		±0.25		mV	C_T	Measured over −1.5 V to +4.5 V functional range after two-point gain/offset calibration; calibration points at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
Threshold INL						After two-point gain/offset calibration; calibration points at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
Focused Range	−5		+5	mV	P	Measured over −0.5 V to +3.5 V range
Full Range	−7		+7	mV	P	Measured over −1.5 V to +4.5 V range
DUTGND Voltage Accuracy	−5	±1	+5	mV	P	Over ±0.1 V range; measured over −0.5 V to +3.5 V focused NWC input range
Uncertainty Band		10		mV	C_B	V_{DUTx} = 0.0 V, sweep comparator threshold to determine the uncertainty band
Programmable Hysteresis		100		mV	C_B	
Hysteresis Resolution		4		Bits	D	
DC PSR		±5		mV/V	C_T	Measured at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V) calibration points
Digital Output Characteristics						
Internal Pull-up Resistance to Comparator, VTTCx	46	50	54	Ω	P	Source 1 mA and 10 mA from the output pin in high state, measure ΔV to calculate resistance; R = ΔV/9 mA; repeat for all output pins

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
Common-Mode Voltage						Measured relative to V_{TTCx}, with 100 Ω differential termination
ADATE320		−250		mV	C_T	
ADATE320-1		−400		mV	C_T	
Differential Mode Voltage						Measured differentially
100 Ω Differential Termination						
ADATE320		250		mV	C_T	
ADATE320-1		400		mV	C_T	
No External Termination						
ADATE320	450	500	550	mV	P	
ADATE320-1	700	800	900	mV	P	
AC SPECIFICATIONS						Unless otherwise specified, all ac tests are performed after dc levels calibration; input transition time: 50 ps 20% to 80%; outputs terminated 50 Ω to 0.0 V; comparator CLC set to ¼ scale (010)
Rise/Fall Times, 20% to 80%		100		ps	C_B	Measured with 50 Ω to 0.0 V
Propagation Delay		580		ps	C_B	V_{DUTx} = 0.0 V to 1.0 V swing, drive term mode, VIT = 0.0 V, comparator threshold = 0.5 V
Propagation Delay TC		1		ps/°C	C_T	V_{DUTx} = 0.0 V to 1.0 V swing, drive term mode, VIT = 0.0 V, comparator threshold = 0.5 V
Propagation Delay Matching High Transition to Low Transition		10		ps	C_B	V_{DUTx} = 0.0 V to 1.0 V swing, drive term mode, VIT = 0.0 V, comparator threshold = 0.5 V
Propagation Delay Matching High to Low Comparator		10		ps	C_B	V_{DUTx} = 0.0 V to 1.0 V swing, drive term mode, VIT = 0.0 V, comparator threshold = 0.5 V
Propagation Delay Dispersion						Drive term mode, VIT = 0.0 V
Slew Rate: 400 ps vs. 1.0 ns (20% to 80%)		20		ps	C_B	V_{DUTx} = 0.0 V to 0.5 V swing, comparator threshold = 0.25 V
Overdrive: 250 mV vs. 1.0 V		25		ps	C_B	For 250 mV: V_{DUTx}: 0.0 V to 0.50 V swing; for 1.0 V: V_{DUTx}: 0.0 V to 1.25 V swing, comparator threshold = 0.25 V
1.0 V Pulse Width: 0.4 ns, 0.5 ns, 1 ns, 5 ns, 10 ns		25		ps	C_B	V_{DUTx} = 0.0 V to 1.0 V swing, 32 MHz, comparator threshold = 0.5 V
0.5 V Pulse Width: 0.4 ns, 0.5 ns, 1 ns, 5 ns, 10 ns		25		ps	C_B	V_{DUTx} = 0.0 V to 0.5 V swing, 32 MHz, comparator threshold = 0.25 V
Duty Cycle: 5% to 95%		10		ps	C_B	V_{DUTx} = 0.0 V to 1.0 V swing, 32 MHz, comparator threshold = 0.5 V
Minimum Detectable Pulse Width		200		ps	C_B	V_{DUTx} = 0.0 V to 1.0 V swing, 32 MHz, greater than 50% output differential amplitude
Input Equivalent Rise/Fall Time, 1.0 V, Terminated		110		ps	C_B	V_{DUTx} = 0.0 V to 1.0 V swing, drive term mode, VIT = 0.0 V, CLC = 010, measured from digitized plot, 20% to 80% transition time of digitized plot is root-sum square (RSS) of input equivalent rise/fall and 50 ps input stimulus
Input Equivalent Rise/Fall Time, 2.0 V, Unterminated		500		ps	C_B	V_{DUTx} = 0.0 V to 2.0 V swing, drive high-Z, measured from digitized plot, 20% to 80% transition time of digitized plot is root-sum square (RSS) of input equivalent rise/fall and 50 ps input stimulus
Cable Loss Compensation (CLC)						V_{DUTx} = 0.0 V to 1.0 V swing, drive term mode, VIT = 0.0 V, maximum CLC setting
CLC Amplitude		20		%	C_B	
CLC Resolution		3		Bits	D	
CLC Time Constant 1		280		ps	S	
CLC Time Constant 2		4.8		ns	S	

DIFFERENTIAL MODE COMPARATOR (DMC) SPECIFICATIONS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DC SPECIFICATIONS						VOHx tests at VOLx = −1.5 V, VOLx tests at VOHx = 1.5 V
Input Voltage Range	−1.5		+4.5	V	D	
Functional Differential Range	±0.05		±1.1	V	D	
Maximum Differential Input			±6.0	V	D	
Input Offset Voltage	−250		+250	mV	P	Offset interpolated from measurements at DAC Code 0x2666 (−1.0 V) and DAC Code 0x5999 (1.0 V), with V_{CM} = 0.0 V
Input Offset Voltage TC		±150		µV/°C	C_T	
Gain	1.0		1.1	V/V	P	Gain derived from measurements at DAC Code 0x2666 (−1.0 V) and DAC Code 0x5999 (1.0 V); based on an ideal DAC transfer function (see Table 24)
Gain TC		±40		ppm/°C	C_T	
VOHx, VOLx Resolution		153		µV	D	
VOHx, VOLx DNL		±250		µV	C_T	After two-point gain/offset calibration; V_{CM} = 0.0 V; calibration points at DAC Code 0x2666 (−1.0 V) and DAC Code 0x5999 (1.0 V)
VOHx, VOLx INL	−8		+8	mV	P	After two-point gain/offset calibration; V_{CM} = 0.0 V; calibration points DAC Code 0x2666 (−1.0 V) and DAC Code 0x5999 (1.0 V), measured over VOHx/VOLx range of −1.1 V to +1.1 V
Uncertainty Band		11		mV	C_B	V_{DUTx} = 0.0 V, sweep comparator threshold to determine the uncertainty band
Programmable Hysteresis		200		mV	C_B	
Hysteresis Resolution		4		Bits	D	
Common-Mode Rejection Ratio (CMRR)	−1.0		+1.0	mV/V	P	ΔOffset measured at V_{CM} = −1.5 V and +4.5 V, V_{DM} = 0.0 V
DC PSR		±5		mV/V	C_T	ΔOffset measured at V_{CM} = 0.0 V, V_{DM} = calibration points DAC Code 0x2666 (−1.0 V) and DAC Code 0x5999 (1.0 V)
AC SPECIFICATIONS						All ac tests are performed after dc levels calibration; input transition time = 50 ps 20% to 80%; outputs terminated 50 Ω to VTTCx, comparator CLC set to ¼ scale (010)
Propagation Delay		580		ps	C_B	V_{DUT0} = 0.0 V, V_{DUT1} = −0.5 V to +0.5 V swing, drive termination mode, VIT = 0.0 V, comparator threshold = 0.0 V, repeat with VDUTx inputs reversed
Propagation Delay TC		2		ps/°C	C_T	V_{DUT0} = 0.0 V, V_{DUT1} = −0.5 V to +0.5 V swing, drive termination mode, VIT = 0.0 V, comparator threshold = 0.0 V, repeat with VDUTx inputs reversed
Propagation Delay Matching High Transition to Low Transition		15		ps	C_B	V_{DUT0} = 0.0 V, V_{DUT1} = −0.5 V to +0.5 V swing, drive termination mode, VIT = 0.0 V, comparator threshold = 0.0 V, repeat with VDUTx inputs reversed
Propagation Delay Matching High to Low Comparator		15		ps	C_B	V_{DUT0} = 0.0 V, V_{DUT1} = −0.5 V to +0.5 V swing, drive termination mode, VIT = 0.0 V, comparator threshold = 0.0 V, repeat with VDUTx inputs reversed
Propagation Delay Dispersion						V_{DUT0} = 0.0 V, VIT = 0.0 V, drive termination mode, repeat with VDUTx inputs reversed
Slew Rate: 400 ps vs. 1 ns (20% to 80%)		30		ps	C_B	V_{DUT1} = −0.5 V to +0.5 V swing, comparator threshold = 0.0 V
Overdrive: 250 mV vs. 750 mV		25		ps	C_B	For 250 mV: V_{DUT1} = 0.0 V to 0.5 V swing; for 750 mV: V_{DUT1} = 0.0 V to 1.0 V swing, comparator threshold = −0.25 V, repeat with VDUTx inputs reversed with comparator threshold = +0.25 V
1.0 V Pulse Width: 0.7 ns, 1.0 ns, 5.0 ns, 10 ns		25		ps	C_B	V_{DUT1} = −0.5 V to +0.5 V swing, 32 MHz, comparator threshold = 0.0 V
0.5 V Pulse Width: 0.6 ns, 1.0 ns, 5.0 ns, 10 ns		25		ps	C_B	V_{DUT1} = −0.25 V to +0.25 V swing, 32 MHz, comparator threshold = 0.0 V

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
Duty Cycle: 5% to 95%		5		ps	C_B	V_{DUT1} = −0.5 V to +0.5 V swing, 32 MHz, comparator threshold = 0.0 V
Minimum Detectable Pulse Width		200		ps	C_B	V_{DUT0} = 0.0 V, V_{DUT1} = −0.5 V to +0.5 V swing, 32 MHz, drive term mode, VIT = 0.0 V, comparator threshold = 0.0 V, greater than 50% output differential amplitude, repeat with VDUTx inputs reversed
Input Equivalent Rise/Fall Time		110		ps	C_B	V_{DUT0} = 0.0 V, V_{DUT1} = −0.5 V to +0.5 V swing, drive term mode, VIT = 0.0 V, comparator threshold = 0.0 V, CLC = ¼ scale, measured from digitized plot, $t = \sqrt{(t_{CMP}^2 - t_{IN}^2)}$
Cable Loss Compensation (CLC)						V_{DUT0} = 0.0 V, V_{DUT1} = −0.8 V to +0.8 V swing, drive term mode, VIT = 0.0 V, comparator threshold = 0.0 V, comparator CLC set to maximum CLC setting, repeat with VDUTx inputs reversed
CLC Amplitude		20		%	C_B	
CLC Resolution		3		Bits	D	
CLC Time Constant 1		280		ps	S	
CLC Time Constant 2		4.8		ns	S	

ACTIVE LOAD SPECIFICATIONS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DC SPECIFICATIONS						Load in active on state, RCVx active
Input Characteristics						
Active Load Commutation Voltage (VCOMx) Range	−1.5		+4.5	V	D	IOHx = IOLx = 1 mA, VDUTx open circuit
VCOMx Offset	−200		+200	mV	P	Measured at DAC Code 0x4000 (0.0 V), uncalibrated
VCOMx Offset TC		±100		µV/°C	C_T	
VCOMx Gain	1.0		1.1	V/V	P	Gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
VCOMx Gain TC		±20		ppm/°C	C_T	
VCOMx Resolution		153		µV	D	
VCOMx DNL		±250		µV	C_T	IOHx = IOLx = 12.5 mA, after two-point gain/offset calibration; measured over VCOMx range −1.5 V to +4.5 V; calibration points DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
VCOMx INL						IOHx = IOLx = 12.5 mA; after two-point gain/offset calibration; calibration points DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
Focused Range	−5		+5	mV	P	Measured over VCOMx range of −0.5 V to +3.5 V
Full Range	−10		+10	mV	P	Measured over VCOMx range of −1.5 V to +4.5 V
DUTGND Voltage Accuracy	−5	±1	+5	mV	P	Over ±0.1 V range; measured over −0.5 V to +3.5 V focused VCOMx range
Output Characteristics						
Maximum Source Current (IOLx)	25			mA	D	$V_{DUTx} \leq$ 3.5 V (a compliance limit is set by a 50 Ω internal resistor as illustrated in Figure 142)
IOLx Offset	−600		+600	µA	P	IOHx = −2.5 mA, VCOMx = 1.5 V, V_{DUTx} = 0.0 V; offset extrapolated from measurements at DAC Code 0x451F (1 mA) and DAC Code 0xA666 (20 mA)
IOLx Offset TC		±1		µA/°C	C_T	
IOLx Gain Error	0		+25	%	P	IOHx = −2.5 mA, VCOMx = 1.5 V, V_{DUTx} = 0.0 V; gain derived from measurements at DAC Code 0x451F (1 mA) and DAC Code 0xA666 (20 mA); based on an ideal dc transfer function
IOLx Gain TC		±100		ppm/°C	C_T	

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
IOLx Resolution		763		nA	D	
IOLx DNL		±1.25		µA	C_T	IOHx = −2.5 mA, VCOMx = 1.5 V, V_{DUTx} = 0.0 V; after two-point gain/offset calibration; measured over IOLx range 0 mA to 25 mA; calibrated at DAC Code 0x451F (1 mA) and DAC Code 0xA666 (20 mA)
IOLx INL	−100		+100	µA	P	IOHx = −2.5 mA, VCOM = 1.5 V, V_{DUTx} = 0.0 V, after two-point gain/offset calibration
IOLx 90% Commutation Voltage		0.25	0.4	V	P	IOHx = IOLx = 25 mA, VCOM = 2.0 V, measure IOLx reference at V_{DUTx} = −1.0 V, measure IOLx current at V_{DUTx} = 1.6 V, check > 90% of reference current
		0.1		V	C_T	IOHx = IOLx = 1 mA, VCOM = 2.0 V, measure IOLx reference at V_{DUTx} = −1.0 V, measure IOLx current at V_{DUTx} = 1.9 V, check > 90% of reference current
Maximum Sink Current (IOHx)	25			mA	D	$V_{DUTx} \geq$ −0.5 V (a compliance limit is set by a 50 Ω internal resistor as illustrated in Figure 142)
IOHx Offset	−600		+600	µA	P	IOLx = −2.5 mA, VCOM = 1.5 V, V_{DUTx} = 3.0 V, offset extrapolated from measurements at DAC Code 0x451F (1 mA) and DAC Code 0xA666 (20 mA)
IOHx Offset TC		±1		µA/°C	C_T	
IOHx Gain Error	0		+25	%	P	IOLx = −2.5 mA, VCOM = 1.5 V, V_{DUTx} = 3.0 V, gain derived from measurements at DAC Code 0x451F (1 mA) and DAC Code 0xA666 (20 mA); based on an ideal DAC transfer function
IOHx Gain TC		±100		ppm/°C	C_T	
IOHx Resolution		763		nA	D	
IOHx DNL		±1.25		µA	C_T	IOLx = −2.5 mA, VCOM = 1.5 V, V_{DUTx} = 3.0 V, after two-point gain/offset calibration; measured over IOHx range of 0 mA to 25 mA; calibrated at DAC Code 0x451F (1 mA) and DAC Code 0xA666 (20 mA)
IOHx INL	−100		+100	µA	P	IOLx = −2.5 mA, VCOM = 1.5 V, V_{DUTx} = 3.0 V, after two-point gain/offset calibration
IOHx 90% Commutation Voltage		0.25	0.4	V	P	IOHx = IOLx = 25 mA, VCOM = 2.0 V, measure IOHx reference at V_{DUTx} = 4.0 V, measure IOHx current at V_{DUTx} = 2.4 V, ensure > 90% of reference current
		0.1		V	C_T	IOHx = IOLx = 1 mA, VCOM = 2.0 V, measure IOHx reference at V_{DUTx} = 4.0 V, measure IOHx current at V_{DUTx} = 2.1 V_{DUTx}, ensure > 90% of reference current
AC SPECIFICATIONS						All ac measurements are performed after dc calibration unless noted, load active on
Dynamic Performance						Toggle RCVx; DUTx terminated 50 Ω to 0.0 V; IOLx = IOHx = 20 mA, VIH = VIL = 0.0 V; VCOM = +1.5 V for IOLx and −1.5 V for IOHx
Propagation Delay, Load Active On to Load Active Off		1.7		ns	C_B	Measured from zero crossing of RCVx − $\overline{\text{RCVx}}$ to 50% of final output value; repeat for drive low and drive high
Propagation Delay, Load Active Off to Load Active On		2.9		ns	C_B	Measured from zero crossing of RCVx − $\overline{\text{RCVx}}$ to 50% of final output value; repeat for drive low and drive high
Propagation Delay Matching		1.2		ns	C_B	Active on vs. active off; repeat for drive low and drive high
Load Spike		140		mV	C_B	Repeat for drive low and drive high
Settling Time to Within 5%		2.5		ns	C_B	Measured from output crossing 50% final value to output within 5% final value

PPMU SPECIFICATIONS

PPMU enabled in force voltage mode unless noted.

Table 7.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
FORCE VOLTAGE (FV)						
Current Range A	−40		+40	mA	D	
Current Range B	−1		+1	mA	D	
Current Range C	−100		+100	µA	D	
Current Range D	−10		+10	µA	D	
Current Range E	−2		+2	µA	D	
FV Range at Output, Range A	−1.0		+4.0	V	D	Output range for full-scale source/sink
	−1.5		+4.5	V	D	Output range for ±25 mA or less
FV Range at Output, Range B, Range C, Range D, and Range E	−1.5		+4.5	V	D	Output range for full-scale source/sink
FV Offset, Range C	−100		+100	mV	P	Measured at DAC Code 0x4000 (0.0 V) in Range C
FV Offset, All Ranges		±30		mV	C_T	Measured at DAC Code 0x4000 (0.0 V) applies to all other ranges
FV Offset TC, All Ranges		±100		µV/°C	C_T	Measured at DAC Code 0x4000 (0.0 V)
FV Gain, Range C	1.0		1.1	V/V	P	Gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V); based on an ideal DAC transfer function
FV Gain, All Ranges		1.05		V/V	C_T	Gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V); based on an ideal DAC transfer function
FV Gain TC, All Ranges		±10		ppm/°C	C_T	Gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
FV INL						
Range A		±1.5		mV	C_T	After two-point gain/offset calibration, output range of −1.5 V to +4.5 V; calibration points DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V), PPMU Current Range A
Range C, Focused Range	−1.7		+1.7	mV	P	After two-point gain/offset calibration, output range of −0.5 V to +3.5 V; calibration points DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
Range C, Full Range	−5		+5	mV	P	After two-point gain/offset calibration, output range of −1.5 V to +4.5 V; calibration points DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
Range B, Range D, and Range E		±1.0		mV	C_T	After two-point gain/offset calibration, output range of −1.5 V to +4.5 V; calibration points DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
FV Compliance vs. Source/Sink Current, Range A (±40 mA)		±1		mV	C_T	Force −1.0 V; measure voltage while sinking 0.0 mA and full-scale current; measure ΔV; force 4.0 V; measure voltage while sourcing 0.0 mA and full-scale current; measure ΔV
FV Compliance vs. Source/Sink Current, Range A (±25 mA)		±1		mV	C_T	Force −1.5 V; measure voltage while sinking 0.0 mA and 25 mA; measure ΔV; force 4.5 V; measure voltage while sourcing 0.0 mA and 25 mA; measure ΔV

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
FV Compliance vs. Source/Sink Current, Range B, Range C, Range D, and Range E		±1		mV	C_T	Force −1.5 V; measure voltage while sinking 0.0 mA and full-scale current; measure ΔV; force 4.5 V; measure voltage while sourcing 0.0 mA and full-scale current; measure ΔV
DUTGND Voltage Accuracy	−5	±1	+5	mV	P	Over ±0.1 V range; measured over −0.5 V to +3.5 V focused PPMU output range
FORCE CURRENT (FI)						PPMU enabled in force current/measure current (FIMI)
DUTx Pin Voltage Range, Range A	−1.0		+4.0	V	D	Full-scale source and sink current
	−1.5		+4.5	V	D	DUTx pin source and sink 25 mA or less
DUTx Pin Voltage Range, Range B, Range C, Range D, and Range E	−1.5		+4.5	V	D	Full-scale source and sink current
Zero-Current Offset, All Ranges	−14.5		+14.5	% FSR	P	Interpolated from measurements at PPMU DAC Code 0x4CCC (−80% FS) and DAC Code 0xB333 (80% FS) for each range
Zero-Current Offset TC		±0.02		% FSR/°C	C_T	
Gain Error, All Ranges	0		30	%	P	Derived from measurements at PPMU DAC Code 0x4CCC (−80% FS) and DAC Code 0xB333 (80% FS) for each range
Gain Drift						
Range A		±50		ppm/°C	C_T	PPMU self heating effects in Range A can influence gain drift measurements
Range B		±50		ppm/°C	C_T	
Range C, Range D, and Range E		±50		ppm/°C	C_T	
INL						After two-point gain/offset calibration
Range A	−0.12		+0.12	% FSR	P	Measured over FSR output of Range A (±40 mA)
Range B, Range C, and Range D	−0.04		+0.04	% FSR	P	Measured over FSR output of Range B (±1 mA), Range C (±100 µA), and Range D (±10 µA)
Range E	−0.045		+0.045	% FSR	P	Measured over FSR output of Range E (±2 µA)
FI Compliance vs. Voltage Load						
Range A	−0.3		+0.3	% FSR	P	Force positive full-scale current driving −1.0 V and +4.0 V, measure ΔI at DUTx pin; force negative full-scale current driving −1.0 V and +4.0 V, measure ΔI at DUTx pin
	−0.1		+0.1	% FSR	P	Force positive full-scale current driving 0.0 V and 3.0 V, measure ΔI at DUTx pin; force negative full-scale current driving 0.0 V and 3.0 V, measure ΔI at DUTx pin
Range B and Range C	−0.3		+0.3	% FSR	P	Force positive full-scale current driving −1.5 V and +4.5 V, measure ΔI at DUTx pin; force negative full-scale current driving −1.5 V and +4.5 V, measure ΔI at DUTx pin
	−0.06		+0.06	% FSR	P	Force positive full-scale current driving 0.0 V and 3.0 V, measure ΔI at DUTx pin; force negative full-scale current driving 0.0 V and 3.0 V, measure ΔI at DUTx pin
Range D	−0.3		+0.3	% FSR	P	Force positive full-scale current driving −1.5 V and +4.5 V, measure ΔI at DUTx pin; force negative full-scale current driving −1.5 V and +4.5 V, measure ΔI at DUTx pin
Range E	−0.85		+0.85	% FSR	P	Force positive full-scale current driving −1.5 V and +4.5 V, measure ΔI at DUTx pin; force negative full-scale current driving −1.5 V and +4.5 V, measure ΔI at DUTx pin; allows 10 nA DUTx pin leakage

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
MEASURE VOLTAGE (MV)						PPMU enabled, force voltage/measure voltage (FVMV)
Range	−1.5		+4.5	V	D	
Offset	−25		+25	mV	P	Range B, V_{DUTx} = 0.0 V, offset = (PPMU_Mx − V_{DUTx})
Offset TC		±50		µV/°C	C_T	
Gain	0.98		1.02	V/V	P	Range B, derived from measurements at V_{DUTx} = 0.0 V and 3.0 V
Gain TC		±5		ppm/°C	C_T	
INL	−1.7		+1.7	mV	P	Range B, measured over −1.5 V to +4.5 V
MEASURE CURRENT (MI)						PPMU enabled in FIMI
DUTx Pin Voltage Range						Full-scale source and sink current
Range A	−1.0		+4.0	V	D	
Range B, Range C, Range D, and Range E	−1.5		+4.5	V	D	
Zero-Current Offset						
Range B	−4		+4	%FSR	P	Interpolated from measurements sourcing and sinking 80% FS current each range; for example, 2% FSR is 40 µA in Range B
All Ranges		±0.5		%FSR	C_T	
Zero-Current Offset TC						
Range A		±0.01		%FSR/°C	C_T	
Range B, Range C, and Range D		±0.01		%FSR/°C	C_T	
Range E		±0.02		%FSR/°C	C_T	
Gain Error						Derived from measurements sourcing and sinking 80% FS current
Range B	−30		+5	%	P	
All Ranges		−10		%	C_T	
Gain TC						
Range A		±50		ppm/°C	C_T	
Range B, Range C, and Range D		±50		ppm/°C	C_T	
Range E		±50		ppm/°C	C_T	
INL						After two-point gain/offset calibration at ±80% FS current
Range A		±0.02		%FSR	C_T	Measured over FSR output of −40 mA to +40 mA
Range B	−0.02		+0.02	%FSR	P	Measured over FSR output of −1 mA to +1 mA
Range C, Range D, and Range E		±0.01		%FSR	C_T	Measured over FSR output of Range C, Range D, and Range E
DUTx Pin Voltage Rejection	−1.3		+1.3	µA	P	Range B, FVMI, force −1.0 V and +4.0 V into 0.5 mA load, measure ΔI reported at PPMU_Mx pin
DUTGND Voltage Accuracy	−5	±1	+5	mV	P	Over ±0.1 V range
MEASURE PIN DC CHARACTERISTICS						
Output Range	−1.5		+5.0	V	D	
Output Impedance			200	Ω	P	PPMU enabled in FVMV, source resistance: PPMU force 4.5 V into 0.0 mA, −1.0 mA, sink resistance: PPMU force −1.5 V into 0.0 mA, 1.0 mA, resistance = ΔV/ΔI at PPMU_Mx pin
Output Leakage Current When Tristated	−1		+1	µA	P	Tested at −1.7 V and +5.2 V
Output Short Circuit Current	−10		+10	mA	P	PPMU enabled in FVMV, source: PPMU force +4.5 V, PPMU_Mx = −1.5 V, sink: PPMU force −1.5 V, PPMU_Mx = 5.0 V

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
PPMU_Mx Pin, Parasitic Output Capacitance			2	pF	S	Parasitic capacitance contributed by pin
PPMU_Mx Pin, External Load Capacitance	100			pF	S	External capacitance tolerated by pin (exceeding this value may cause instability)
PPMU VOLTAGE CLAMPS (FI)						PPMU enabled in FIMI, PPMU clamps enabled; clamp accuracy applies only when |PCHx − PCLx| ≥ 1.0 V
Low Voltage Clamp Range (PCLx)	−1.5		+3.5	V	D	
High Voltage Clamp Range (PCHx)	−0.5		+4.5	V	D	
Offset, Voltage Clamps (PCHx/PCLx)	−300		+300	mV	P	Range B, PPMU force ±0.5 mA into open; PCHx measured at DAC Code 0x4000 (0.0 V) with PCLx at DAC Code 0x0000 (−2.5 V); PCLx measured at DAC Code 0x4000 (0.0 V) with PCHx at DAC Code 0xFFFF (+7.5 V)
Offset TC, Voltage Clamps (PCHx/PCLx)		±0.5		mV/°C	C_T	
Gain, Voltage Clamps (PCHx/PCLx)	1.0		1.1	V/V	P	Range B, PPMU force ±0.5 mA into open; PCHx gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V) with PCLx at DAC Code 0x0000 (−2.5 V); PCLx gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V) with PCHx at DAC Code 0xFFFF (7.5 V)
Gain TC, Voltage Clamps (PCHx/PCLx)		±25		ppm/°C	C_T	
INL, Voltage Clamps (PCHx/PCLx)	−20		+20	mV	P	Range B, PPMU force ±0.5 mA into open after two-point gain/offset calibration; measured over PPMU clamp functional range
Positive Voltage Clamp, Voltage Droop (Source)	−50		+50	mV	P	ΔV at DUTx pin, Range A, PCHx = +4.0 V, PCLx = −1.0 V, PPMU force 5.0 mA and 40 mA into open circuit, calibrated
Negative Voltage Clamp, Voltage Droop (Sink)	−50		+50	mV	P	ΔV at DUTx pin, Range A, PCHx = +4.0 V, PCLx = −1.0 V, PPMU force −5.0 mA and −40 mA into open circuit, calibrated
DUTGND Voltage Accuracy	−5	±1	+5	mV	P	Over ±0.1 V range; measured at end points of clamp functional range
PPMU CURRENT CLAMPS (FV)						PPMU enabled in FVMV, dc accuracy of the current clamps only applies over the following conditions: 30% FS ≤ PCHx ≤ 100% FS or −100% FS ≤ PCLx ≤ −30% FS
Functional Range						
Low Current Clamp (PCLx)	−120		−20	%FS	S	For example, −120% FS in Range A is −48 mA and −20% FS in Range A is −8 mA
High Current Clamp (PCHx)	20		120	%FS	S	For example, 20% FS in Range A is 8 mA and 120% FS in Range A is 48 mA
DC Accuracy Range						
Low Current Clamp (PCLx)	−100		−30	%FS	D	For example, −100% FS in Range A is −40 mA and −30% FS in Range A is −12 mA
High Current Clamp (PCHx)	30		100	%FS	D	For example, 30% FS in Range A is 12 mA and 100% FS in Range A is 40 mA
Static Current Limit, Source and Sink, All Ranges	±120	±140	±160	%FS	P	PCLx at DAC Code 0x0000 (−2.5 V), PCHx at DAC Code 0xFFFF (7.5 V), sink: force −1.5 V, short DUTx to 4.5 V, source: force 4.5 V, short DUTX to −1.5 V
Offset, Current Clamps (PCHx/PCLx)	−10		+10	%FSR	P	All ranges; PPMU force ±1.0 V into 0.0 V[1]
Offset TC, Current Clamps (PCHx/PCLx)		±0.02		%FSR/°C	C_T	All ranges

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
Gain Error, Current Clamps (PCHx/PCLx)	0		30	%	P	All ranges; PPMU force ±1.0 V into 0.0 V[2]
Gain TC, Current Clamps (PCHx/PCLx)		±50		ppm/°C	C_T	All ranges
INL, Current Clamps (PCHx/PCLx)	−0.15		+0.15	%FSR	P	All ranges; PPMU force ±1.0 V into 0.0 V, after two-point gain/offset calibration; PCHx calibration at DAC Code 0xA000 (3.75 V or 50% FS) and DAC Code 0xB333 (4.50 V or 80% FS); PCLx calibration at DAC Code 0x6000 (1.25 V or −50% FS) and DAC Code 0x4CCC (0.50 V or −80% FS); measured over dc accuracy range
Current Droop						
Low Current Clamp (PCLx), Sink	−2		+2	%FSR	P	PCLx = 0.5 V (−80% FS), PCHx = 4.5 V (80% FS), PPMU force −0.5 V and +3.5 V into V_{DUTx} = 4.5 V, measure ΔI at the DUTx pin in Range A
High Current Clamp (PCHx), Source	−2		+2	%FSR	P	PCLx = 0.5 V (−80% FS), PCHx = 4.5 V (80% FS), PPMU force −0.5 V and +3.5 V into V_{DUTx} = −1.5 V, measure ΔI at the DUTx pin in Range A
SETTLING/SWITCHING TIMES						
FV Settling Time to 0.1% of Final Value						
Range A, 200 pF and 2000 pF Load		20		µs	S	PPMU enabled in FV, Range A, step from 0.0 V to 4.0 V
Range B, 200 pF and 2000 pF Load		25		µs	S	PPMU enabled in FV, Range B, DCL disabled, step from 0.0 V to 4.0 V
Range C, 200 pF Load		25		µs	S	PPMU enabled in FV, Range C, DCL disabled, step from 0.0 V to 4.0 V
Range C, 2000 pF Load		65		µs	S	PPMU enabled in FV, Range C, DCL disabled, step from 0.0 V to 4.0 V
FV Settling Time to 1.0% of Final Value						
Range A, 200 pF and 2000 pF Load		16		µs	C_B	PPMU enabled in FV, Range A, DCL disabled, step from 0.0 V to 4.0 V
Range B, 200 pF and 2000 pF Load		14		µs	C_B	PPMU enabled in FV, Range B, DCL disabled, step from 0.0 V to 4.0 V
Range C, 200 pF and 2000 pF Load		18		µs	C_B	PPMU enabled in FV, Range C, DCL disabled enabled, step from 0.0 V to 4.0 V
FI Settling Time to 0.1% of Final Value						
Range A, 200 pF in Parallel with 120 Ω		16		µs	S	PPMU enabled in FI, Range A, DCL disabled, step from 0.0 mA to 40 mA
Range B, 200 pF in Parallel with 1.5 kΩ		10		µs	S	PPMU enabled in FI, Range B, DCL disabled, step from 0.0 mA to 1 mA
Range C, 200 pF in Parallel with 15.0 kΩ		40		µs	S	PPMU enabled in FI, Range C, DCL disabled, step from 0.0 mA to 100 µA
FI Settling Time to 1.0% of Final Value						
Range A, 200 pF in Parallel with 120 Ω		8		µs	C_B	PPMU enabled in FI, Range A, DCL disabled, step from 0.0 mA to 40 mA
Range B, 200 pF in Parallel with 1.5 kΩ		8		µs	C_B	PPMU enabled in FI, Range B, DCL disabled, step from 0.0 mA to 1 mA
Range C, 200 pF in Parallel with 15.0 kΩ		8		µs	C_B	PMU enabled in FI, Range C, DCL disabled, step from 0.0 mA to 100 µA

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
INTERACTION AND CROSSTALK						
Measure Voltage Channel to Channel Crosstalk		10		µV	C_T	PPMU enabled in FIMV, Range B, channel under test: force 0.0 mA into 0.0 V; other channel: force 0.0 mA into V_{DUTx}; sweep V_{DUTx} from −1.5 V to +4.5 V; measure ΔV at PPMU_Mx under test
Measure Current Channel to Channel Crosstalk		0.0001		%FSR	C_T	PPMU enabled in FVMI, Range B; channel under test: force 0.0 V into open circuit; other channel: force 0.0 V into I_{DUTx}; sweep I_{DUTx} from −1.0 mA to +1.0 mA; measure ΔV at PPMU_Mx under test

[1] PCHx offset is derived from measurements at DAC Code 0xA000 (3.75 V or 50% FS) and DAC Code 0xB333 (4.50 V or 80% FS), with PCLx at DAC Code 0x0000 (−2.5 V). PCLx offset is derived from measurements at DAC Code 0x6000 (1.25 V or −50% FS) and DAC Code 0x4CCC (0.50 V or −80% FS), with PCHx at DAC Code 0xFFFF (7.5 V).
[2] PCHx gain is derived from the measurements at DAC Code 0xA000 (3.75 V or 50% FS) and DAC Code 0xB333 (4.50 V or 80% FS), with PCLx at DAC Code 0x0000 (−2.5 V). PCLx gain is derived from measurements at DAC Code 0x6000 (1.25 V or −50% FS) and DAC Code 0x4CCC (0.50 V or −80% FS), with PCHx at DAC Code 0xFFFF (7.5 V). For example, the ideal gain is ±FS per 2.5 V in all ranges; in Range B, the ideal gain is ±400 µA/V; therefore, 30% error is ±520 µA/V.

PPMU GO/NO-GO COMPARATORS SPECIFICATIONS

Table 8.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DC SPECIFICATIONS						
Compare Voltage Range	−1.5		+5.0	V	D	
Input Offset Voltage	−250		+250	mV	P	Measured at DAC Code 0x4000 (0 V)
Input Offset Voltage TC		±100		µV/°C	C_T	
Gain	1.0		1.1	V/V	P	Gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
Gain TC		±10		ppm/°C	C_T	Gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
Comparator Threshold Resolution		153		µV	D	
Comparator Threshold DNL		±250		µV	C_T	After two-point calibration; measured over POHx/POLx range −1.5 V to +5.0 V; calibration points DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
Comparator Threshold INL	−7		+7	mV	P	After two-point calibration; measured over POHx/POLx range −1.5 V to +5.0 V; calibration points DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
DUTGND Voltage Accuracy	−5	±1	+5	mV	P	Over ±0.1 V range

PPMU EXTERNAL SENSE PINS SPECIFICATIONS

Table 9.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DC SPECIFICATIONS						
Voltage Range	−1.5		+4.5	V	D	PPMU input select, in all states
Leakage	−2	0.0	+2	nA	P	Tested at −1.5 V and +4.5 V
Maximum Load Capacitance	2000			pF	S	Capacitive load tolerated at DUTx sense pins

VREF, VREFGND, AND DUTGND REFERENCE INPUT PINS SPECIFICATIONS

Table 10.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DC SPECIFICATIONS						
VREF Input Voltage Range	2.475	2.500	2.525	V	D	Provided externally, V_{REF} = 2.500 V, V_{REFGND} = 0.000 V
VREF Input Bias Current			10	µA	P	Tested with 2.500 V applied
DUTGND Input Voltage Range, Referenced to AGND	−0.1		+0.1	V	D	
DUTGND Input Bias Current	−10		+10	µA	P	Tested at −100 mV and +100 mV

TEMPERATURE MONITOR SPECIFICATIONS

Table 11.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DC SPECIFICATIONS						
Temperature Sensor Gain		10		mV/K	D	3.00 V at room temperature, 300 K (23°C)
Temperature Sensor Accuracy		±10		°C	C_T	20°C < T_C < 80°C, $V_{CCTHERM}$ only (T_J = T_C)

ALARM FUNCTIONS SPECIFICATIONS

Table 12.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DC SPECIFICATIONS						
Overvoltage Alarm High, OVDH						
Functional Voltage Range	−1.0		+5.0	V	D	OVDL DAC set to DAC Code 0x0000 (−2.5 V)
Uncalibrated Error at −1.0 V	−300		+200	mV	P	Includes 5% uncalibrated gain ±250 mV offset
Uncalibrated Error at 5.0 V	0		500	mV	P	Includes 5% uncalibrated gain ±250 mV offset
Offset Voltage TC		±0.5		mV/°C	C_T	
Gain		1.05		V/V	C_T	Gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V); based on an ideal DAC transfer function (see Table 24)
Hysteresis		140		mV	C_T	Hysteresis is only applied coming out of alarm
Overvoltage Alarm Low, OVDL						
Functional Voltage Range	−2.0		+4.0	V	D	OVDH DAC set to DAC Code 0xFFFF (7.5 V)
Uncalibrated Error at −2.0 V	−350		+150	mV	P	Includes 5% uncalibrated gain ±250 mV offset
Uncalibrated Error at 4.0 V	−50		+450	mV	P	Includes 5% uncalibrated gain ±250 mV offset
Offset Voltage TC		±0.5		mV/°C	C_T	
Gain		1.05		V/V	C_T	Gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V); based on an ideal DAC transfer function (see Table 24)
Hysteresis		140		mV	C_T	Hysteresis is only applied coming out of alarm
Thermal Alarm						
Setpoint Error		±10		°C	C_T	Relative to default alarm value, T_J = 100°C
Thermal Hysteresis		15		°C	C_T	

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
$\overline{\text{ALARM}}$ Output Characteristics						
Off State Leakage		10	500	nA	P	Disable alarm, apply V_{DD} to $\overline{\text{ALARM}}$ pin, and measure leakage current
Maximum On Voltage at 200 µA		0.1	0.7	V	P	$\overline{\text{ALARM}}$ pin asserted, force 200 µA into pin and measure voltage
AC SPECIFICATIONS						
Propagation Delay		0.5		µs	C_B	For OVDH: V_{DUTx} = 0.0 V to 4.5 V step, OVDH = 4.0 V, OVDL = −1.0 V; for OVDL: V_{DUTx} = 0.0 V to −1.5 V step, OVDH = 4.0 V, OVDL = −1.0 V

SERIAL PROGRAMMABLE INTERFACE (SPI) SPECIFICATIONS

Table 13.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DC SPECIFICATIONS						
Input Voltage						$\overline{\text{RST}}$, $\overline{\text{CS}}$, SCLK, SDI
Logic High	V_{DD} − 0.7		V_{DD}	V	P_F	
Logic Low	0.0		0.7	V	P_F	
Input Bias Current	−10	1	+10	µA	P	Tested at 0.0 V and V_{DD}; $\overline{\text{RST}}$ tested at V_{DD}; $\overline{\text{RST}}$ has an internal 50 kΩ pull-up to V_{DD}
SCLK Crosstalk on DUTx Pin		1		mV	C_B	DCL disabled, PPMU forcing 0.0 V
Serial Output						
Logic High	V_{DD} − 0.5		V_{DD}	V	P_F	SDO, sourcing 2 mA
Logic Low	0.0		0.5	V	P_F	Sinking 2 mA
$\overline{\text{BUSY}}$ Output Characteristics						Open-drain output
Off State Leakage		10	500	nA	P	$\overline{\text{BUSY}}$ pin not asserted, apply V_{DD} to pin and measure leakage current
Maximum On Voltage at 2 mA		0.01	0.7	V	P	$\overline{\text{BUSY}}$ pin asserted, force 2 mA into pin and measure voltage

SPI TIMING SPECIFICATIONS

Table 14.

Parameter	Symbol	Min	Typ	Max	Unit	Test Level	Description
SCLK Operating Frequency	f_{CLK}		50		MHz	P_F	
		0.5		100	MHz	S	
SCLK High Time	t_{CH}	4.5			ns	S	
SCLK Low Time	t_{CL}	4.5			ns	S	
$\overline{\text{CS}}$ to SCLK Setup at Assert	t_{CSAS}	1.5			ns	S	Setup time of $\overline{\text{CS}}$ assert to next rising edge of SCLK.
$\overline{\text{CS}}$ to SCLK Hold at Assert	t_{CSAH}	1.5			ns	S	Hold time of $\overline{\text{CS}}$ assert to next rising edge of SCLK.
$\overline{\text{CS}}$ to SCLK Setup at Release	t_{CSRS}	1.5			ns	S	Setup time of $\overline{\text{CS}}$ release to next rising edge of SCLK.
$\overline{\text{CS}}$ to SCLK Hold at Release	t_{CSRH}	1.5			ns	S	Hold time of $\overline{\text{CS}}$ release to next rising edge of SCLK. This parameter is only critical if the number of SCLK cycles from previous release of $\overline{\text{CS}}$ is the minimum specified by the t_{CSAM} parameter.
$\overline{\text{CS}}$ Assert to SDO Active	t_{CSO}	0		4	ns	S	Delay time from $\overline{\text{CS}}$ assert to SDO active state.
$\overline{\text{CS}}$ Release to SDO High-Z	t_{CSZ}	0		11	ns	S	Delay from $\overline{\text{CS}}$ release to SDO high-Z state, strongly influenced by external SDO pin loading.
$\overline{\text{CS}}$ Release to Next Assert	t_{CSAM}	3			Cycles	D	Minimum release time of $\overline{\text{CS}}$ between consecutive assertions of $\overline{\text{CS}}$. This parameter is specified in units of SCLK cycles, more specifically in terms of rising edges of the SCLK input.

Parameter	Symbol	Min	Typ	Max	Unit	Test Level	Description
SDI to SCLK Setup	t_{DS}	3			ns	S	Setup time of SDI data prior to next rising edge of SCLK.
SDI to SCLK Hold	t_{DH}	4			ns	S	Hold time of SDI data following previous rising edge of SCLK.
SCLK to Valid SDO	t_{DO}	0		6	ns	S	Propagation delay from rising edge of SCLK to valid SDO data.
$\overline{BUSY}$ Assert from $\overline{CS}$/$\overline{RST}$	t_{BUSA}	0		6	ns	S	Propagation delay from first rising SCLK following valid $\overline{CS}$ release (or $\overline{RST}$ release in the case of hardware reset) to $\overline{BUSY}$ assert.
$\overline{BUSY}$ Width	t_{BUSW}						
Following $\overline{CS}$		3		21	Cycles	D	Delay time from first rising SCLK after valid $\overline{CS}$ release to $\overline{BUSY}$ release. Satisfies the requirements detailed in the SPI Clock Cycles and the Pin section, except following $\overline{RST}$ or software reset.
Following $\overline{RST}$		744			Cycles	D	Delay time from first rising SCLK after $\overline{RST}$ release (or valid $\overline{CS}$ release in the case of software reset) to $\overline{BUSY}$ release. Satisfies the requirement of synchronous reset sequence detailed in the SPI Clock Cycles and the Pin section.
$\overline{BUSY}$ Release from SCLK	t_{BUSR}	0		10	ns	S	Propagation delay from qualifying SCLK edge to $\overline{BUSY}$ release.
Width of $\overline{RST}$ Assert	t_{RMIN}	5			ns	S	Minimum width of asynchronous $\overline{RST}$ assert, 5 pF external loading.
$\overline{RST}$ to SCLK Setup at Assert	t_{RS}	1.5			ns	S	Minimum setup time of $\overline{RST}$ release to next rising edge of SCLK.
SCLK Cycles per SPI Word	t_{SPI}	29			Cycles	D	Minimum number of SCLK rising edge cycles required per valid SPI operation, including the minimum t_{CSAM} requirement between consecutive $\overline{CS}$ assertions.
Internal DAC Settling to Within ±2 mV from $\overline{BUSY}$ Release	t_{DAC}		10		µs	C_B	Settling time of internal analog DAC levels to within ±2 mV. Settling time is relative to the release of $\overline{BUSY}$.[1]

[1] The overall settling time may be dominated by the characteristics of an analog block (such as the PPMU or driver) and its respective mode setting (such as Range A or Range B).

SPI TIMING DIAGRAMS

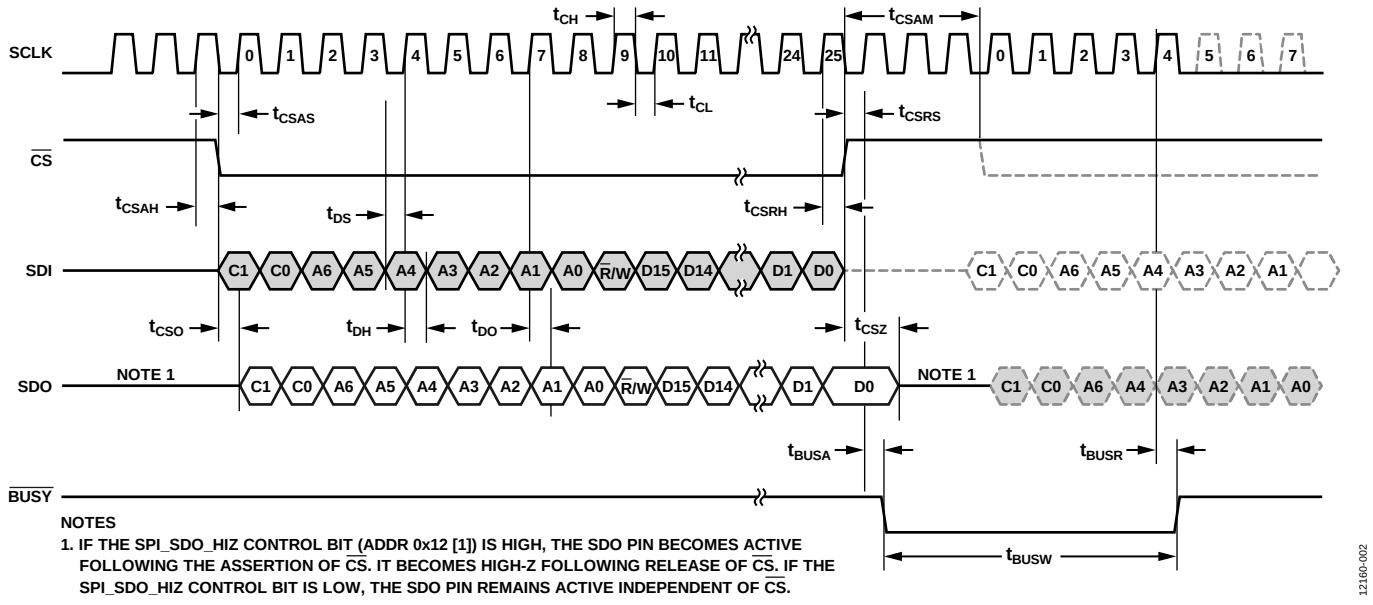


Figure 2. SPI Detailed Read/Write Timing Diagram

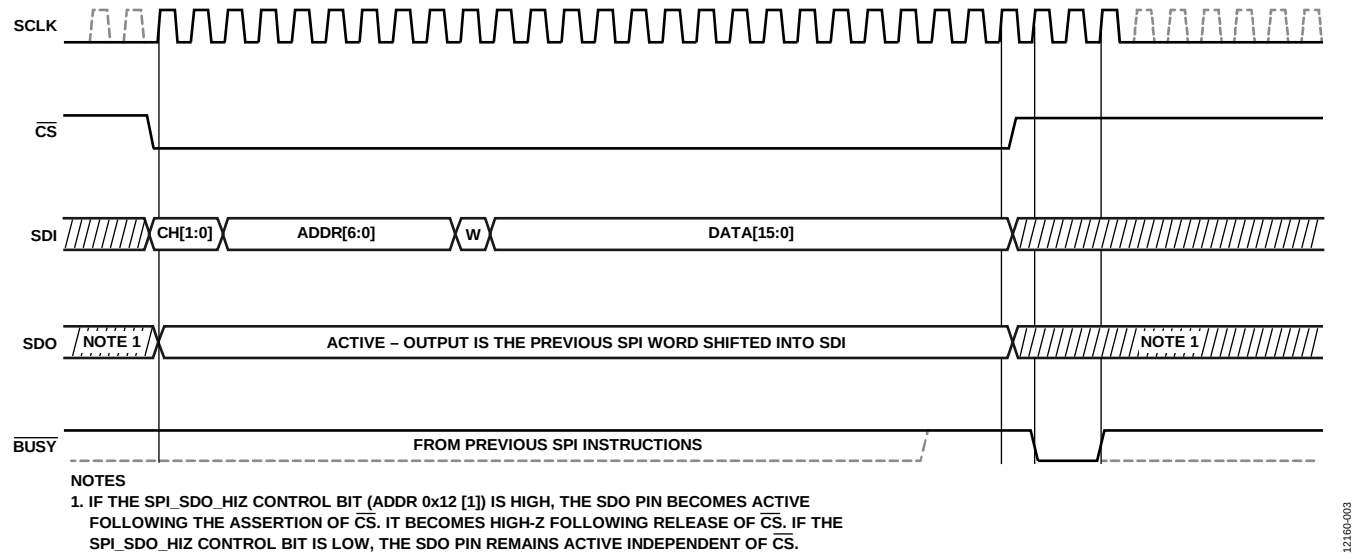


Figure 3. SPI Write Instruction Timing Diagram

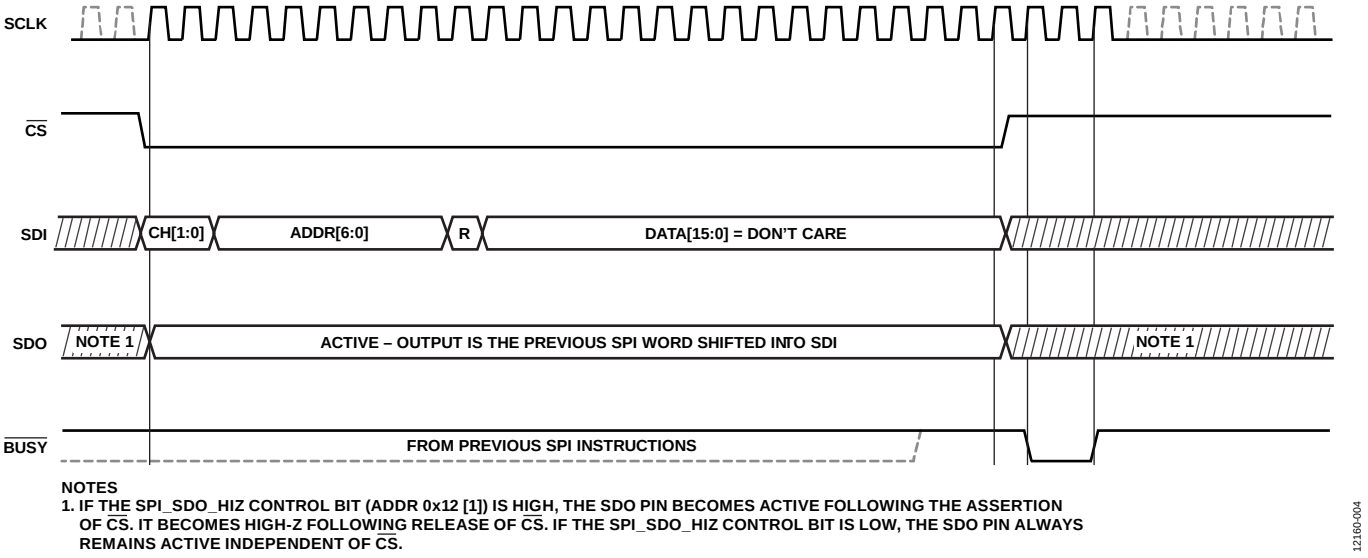
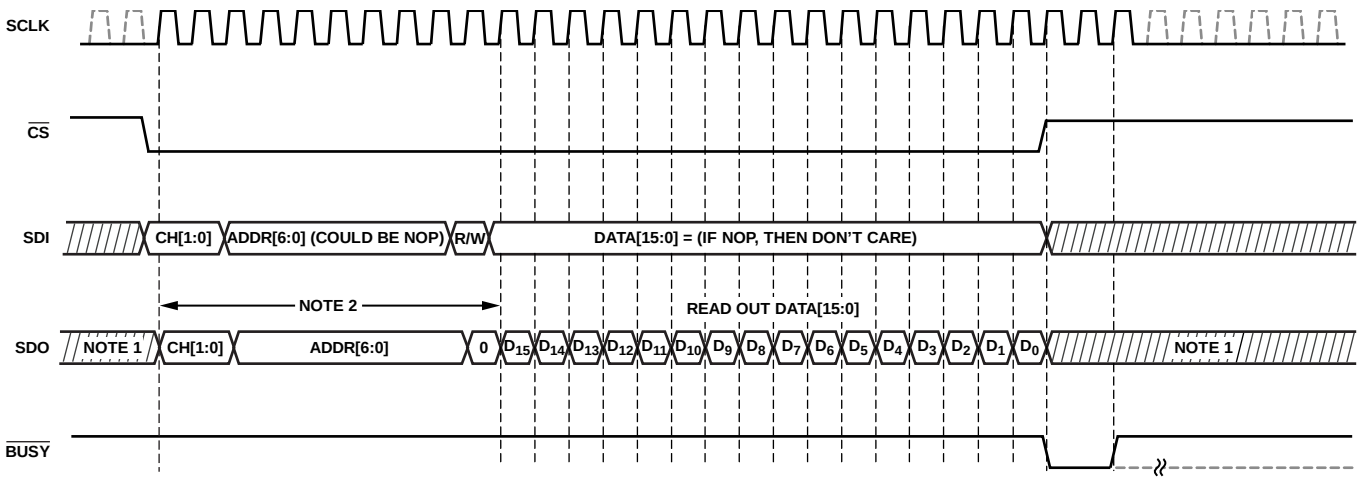


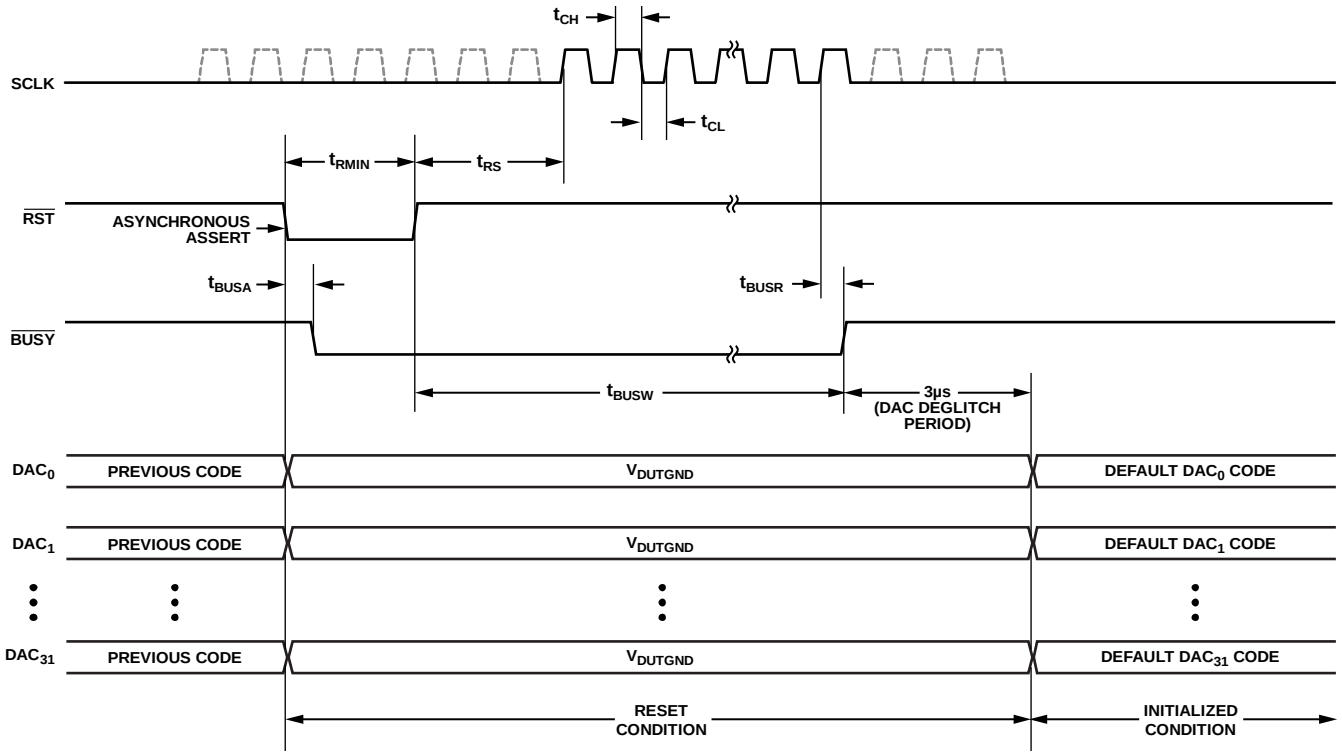
Figure 4. SPI Read Request Instruction Timing Diagram (Prior to Readout Instruction)



NOTES
1. IF THE SPI_SDO_HIZ CONTROL BIT (ADDR 0x12 [1]) IS HIGH, THE SDO PIN BECOMES ACTIVE FOLLOWING THE ASSERTION OF $\overline{CS}$. IT BECOMES HIGH-Z FOLLOWING RELEASE OF $\overline{CS}$. IF THE SPI_SDO_HIZ CONTROL BIT IS LOW, THE SDO PIN REMAINS ACTIVE INDEPENDENT OF $\overline{CS}$.
2. THE FIRST 10 BITS OF SDO FOLLOWING A READ REQUEST ECHO ADDRESS AND CHANNEL BITS OF THE PRECEDING REQUEST. THE R/W BIT POSITION IS SET LOW. THE FOLLOWING 16 BITS CONTAIN DATA FROM THE REQUESTED ADDRESS AND CHANNEL.

12160-005

Figure 5. SPI Readout Instruction Timing Diagram (Subsequent to Read Request Instruction)



12160-006

Figure 6. SPI Detailed Hardware Reset Timing Diagram

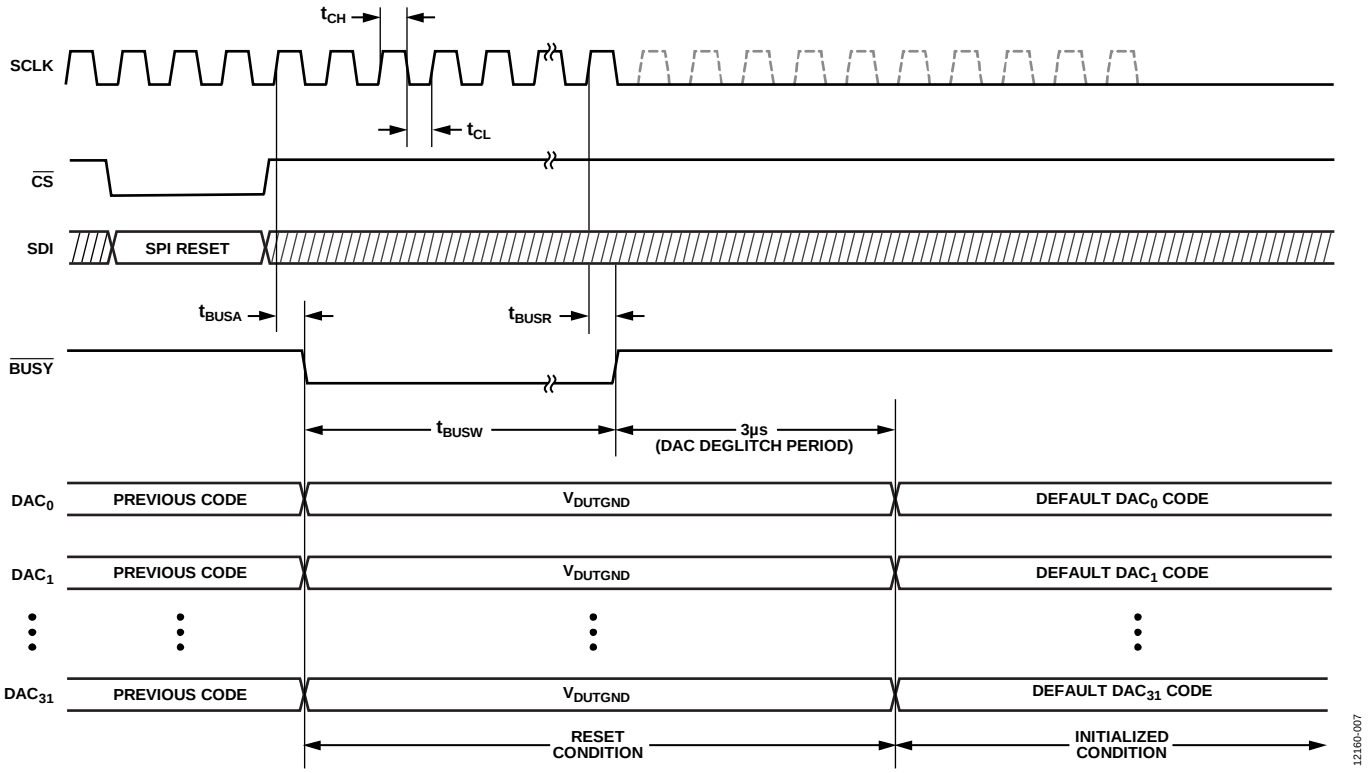


Figure 7. SPI Detailed Software Reset Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 15.

Parameter	Rating
Supply Voltages	
Positive Supply Voltage (V_{CC} to PGND)	−0.5 V to +9.0 V
Positive Supply Voltage (V_{DD} to DGND)	−0.5 V to +2.2 V
Negative Supply Voltage (V_{EE} to PGND)	−6.0 V to +0.5 V
Supply Voltage Difference (V_{CC} to V_{EE})	−1.0 V to +15.0 V
Reference Ground (DUTGND to AGND)	−0.5 V to +0.5 V
Supply Sequence or Dropout Condition	No limitations
Input/Output Voltages	
Digital Input Voltage Range	−0.5 V to V_{DD} + 0.5 V
VREF Input Voltage Range	−0.5 V to +3.5 V
VREFGND, DUTGND Input Voltage Range	−0.5 V to +0.5 V
DUTx Output Short-Circuit Voltage[1]	−3.0 V to +6.0 V
High Speed Termination (VTTCx, VTTDx) Input Voltage Range	−0.5 V to +2.2 V
High Speed DATx/RCVx Common-Mode Input Voltage Range[2]	−0.5 V to +2.2 V
High Speed DATx/RCVx Differential Mode Input Voltage Range[2]	−1.0 V to +1.0 V
High Speed CMPHx/CHPLx, PPMU_CMPHx/PPMU_CMPLx Absolute Output Voltage Range	−0.5 V to +2.2 V
DUTx Input/Output Pin Current Limit	
DCL Maximum Short-Circuit Current[3]	±120 mA
Operating Temperature, Junction	125°C
Storage Temperature Range	−65°C to +150°C

[1] R_L = 0 Ω, V_{DUTx} continuous short-circuit condition (VIH, VIL, VIT), high-Z, VCOM, and all clamp modes.
[2] DATx, $\overline{DATx}$, RCVx, $\overline{RCVx}$, R_{SOURCE} = 0 Ω, no pin to exceed either maximum common-mode input range or differential mode input range.
[3] R_L = 0 Ω, V_{DUTx} = −3 V to +6 V; DCL current limit. Continuous short-circuit condition. The ADATE320 is designed to withstand continuous short-circuit fault.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 16. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}	θ_{JC}	Unit
84-Lead LFCSP	N/A[1]	N/A[1]	3.2	°C/W
	0	45	N/A[1]	°C/W
	1	40	N/A[1]	°C/W
	2	37	N/A[1]	°C/W

[1] N/A means not applicable.

EXPLANATION OF TEST LEVELS

D Definition.

S Design verification simulation.

P 100% production tested.

P_F Functionally checked during production test.

C_T Characterized on tester.

C_B Characterized on bench.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

USER INFORMATION AND TRUTH TABLES

Table 17. Driver Truth Table[1]

DRV Control Register				High Speed Inputs[2]		
DRIVE_ENABLE_x, Address 0x19, Bit 0	DRIVE_FORCE_x, Address 0x19, Bit 1	DRIVE_FORCE_STATE_x, Address 0x19, Bits[3:2]	DRIVE_VT_HIZ_x, Address 0x19, Bit 4	DATx	RCVx	Driver State
0	X	XX	X	X	X	Low leakage
1	1	00	X	X	X	Active VIL
1	1	01	X	X	X	Active VIH
1	1	10	X	X	X	Active high-Z
1	1	11	X	X	X	Active VIT
1	0	XX	0	X	1	Active high-Z
1	0	XX	1	X	1	Active VIT
1	0	XX	X	0	0	Active VIL
1	0	XX	X	1	0	Active VIH

[1] X means don't care.
[2] See Figure 139 for more detailed information about high speed DATx/RCVx input multiplexing.

Table 18. Comparator Truth Table

DMC_ENABLE, Address 0x1A, Bit 0	Comparator State							
	CMPH0	State	CMPL0	State	CMPH1	State	CMPL1	State
0	V_{DUT0} < VOH0	0	V_{DUT0} < VOL0	0	V_{DUT1} < VOH1	0	V_{DUT1} < VOL1	0
	VOH0 < V_{DUT0}	1	VOL0 < V_{DUT0}	1	VOH1 < V_{DUT1}	1	VOL1 < V_{DUT1}	1
1[1]	$V_{DUT0} - V_{DUT1}$ < VOH0	0	$V_{DUT0} - V_{DUT1}$ < VOL0	0	V_{DUT1} < VOH1	0	V_{DUT1} < VOL1	0
	VOH0 < $V_{DUT0} - V_{DUT1}$	1	VOL0 < $V_{DUT0} - V_{DUT1}$	1	VOH1 < V_{DUT1}	1	VOL1 < V_{DUT1}	1

[1] Note that the Channel 1 normal window comparator continues to function while the device is in differential compare mode, but at a greatly reduced bandwidth.

Table 19. Active Load Truth Table[1]

LOAD/DRV Control Registers			High Speed Inputs[2]		
LOAD_ENABLE_x, Address 0x1B, Bit 0	LOAD_FORCE_x, Address 0x1B, Bit 1	DRIVE_VT_HIZ_x, Address 0x19, Bit 4	DATx	RCVx	Load State
0	X	X	X	X	Low leakage
1	1	X	X	X	Active on
1	0	X	X	0	Active off
1	0	0	X	1	Active on
1	0	1	X	1	Active off

[1] X means don't care.
[2] See Figure 139 for more detailed information about high speed DATx/RCVx input multiplexing.

Table 20. PPMU Go/No-Go Comparator Truth Table[1]

PPMU Control Register		PPMU Go/No-Go Comparator State[2]			
PPMU_ENABLE_x, Address 0x1C, Bit 0	PPMU_STANDBY_x, Address 0x1C, Bit 1	PPMU_CMPHx	State	PPMU_CMPLx	State
0	X	X	0	X	0
1	X	PPMUx MV/MI < POHx	0	PPMUx MV/MI < POLx	0
1	X	POHx < PPMUx MV/MI	1	POLx < PPMUx MV/MI	1

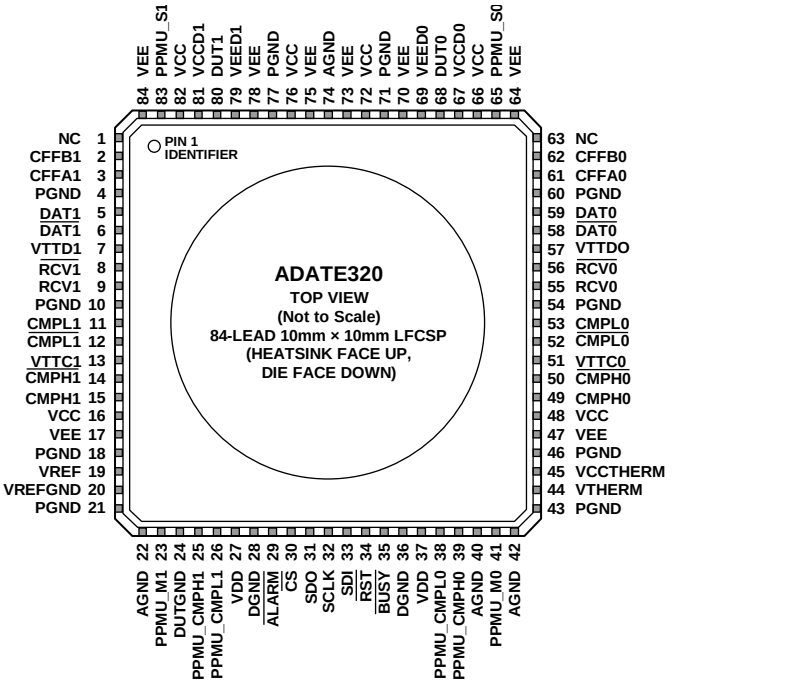
[1] X means don't care.
[2] The PPMUx MV/MI inputs to the PPMU go/no-go comparators always come directly from the respective internal PPMU instrumentation amplifiers, not from the PPMU_Mx output pins (see Figure 144). The internal instrumentation amplifiers are independently configured for either measure voltage (MV) or measure current (MI), depending on the settings of the PPMU_MEAS_VI_x control bit, as described in Figure 151. When PPMU power is not enabled, the respective go/no-go comparator outputs are locked to a static low state (see Table 21).

Table 21. PPMU Measure Pin Truth Table[1]

PPMU Control Register					
PPMU_ENABLE_x, Address 0x1C, Bit 0	**PPMU_STANDBY_x, Address 0x1C, Bit 1**	**PPMU_MEAS_ENABLE_x, Address 0x1C, Bit 13**	**PPMU_MEAS_SEL_x, Address 0x1C, Bit 14**	**PPMU_MEAS_VI_x, Address 0x1C, Bit 6**	**PPMU_Mx, Pin State**
X	X	0	X	X	High-Z
0	X	1	0	X	Active MV
0	X	1	1	X	Active VTHERM[2]
1	X	1	0	0	Active MV
1	X	1	0	1	Active MI
1	X	1	1	X	Active VTHERM[2]

[1] X means don't care.
[2] When applicable, PPMU_M0 is connected to the internal temperature sensor node (VTHERM), and PPMU_M1 is connected to the internal temperature sensor reference ground node (AGND) (see Figure 144).

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT.
2. THE EXPOSED PAD IS INTERNALLY CONNECTED VIA A HIGH IMPEDANCE DIE ATTACHED TO VEE (SUBSTRATE).

12160-008

Figure 8. Pin Configuration

Table 22. Pin Function Descriptions

Pin No.	Mnemonic	Description
59	DAT0	Driver High Speed Data Input, Channel 0.
58	$\overline{\text{DAT0}}$	Driver High Speed Data Input Complement, Channel 0.
57	VTTD0	Driver High Speed Input Termination, Channel 0.
55	RCV0	Driver High Speed Receive Input, Channel 0.
56	$\overline{\text{RCV0}}$	Driver High Speed Receive Input Complement, Channel 0.
5	DAT1	Driver High Speed Data Input, Channel 1.
6	$\overline{\text{DAT1}}$	Driver High Speed Data Input Complement, Channel 1.
7	VTTD1	Driver High Speed Input Termination, Channel 1.
9	RCV1	Driver High Speed Receive Input, Channel 1.
8	$\overline{\text{RCV1}}$	Driver High Speed Receive Input Complement, Channel 1.
53	CMPL0	Comparator High Speed Output Low, Channel 0.
52	$\overline{\text{CMPL0}}$	Comparator High Speed Output Low Complement, Channel 0.
51	VTTC0	Comparator High Speed Output Termination, Channel 0.
49	CMPH0	Comparator High Speed Output High, Channel 0.
50	$\overline{\text{CMPH0}}$	Comparator High Speed Output High Complement, Channel 0.
11	CMPL1	Comparator High Speed Output Low, Channel 1.
12	$\overline{\text{CMPL1}}$	Comparator High Speed Output Low Complement, Channel 1.
13	VTTC1	Comparator High Speed Output Termination, Channel 1.
15	CMPH1	Comparator High Speed Output High, Channel 1.
14	$\overline{\text{CMPH1}}$	Comparator High Speed Output High Complement, Channel 1.
61	CFFA0	PPMU External Compensation Capacitor Pin A, Channel 0.
62	CFFB0	PPMU External Compensation Capacitor Pin B, Channel 0.
65	PPMU_S0	PPMU External Sense Connect, Channel 0.
41	PPMU_M0	PPMU Analog Measure Output, Channel 0.
38	PPMU_CMPL0	PPMU Go/No-Go Comparator Output Low, Channel 0.

Pin No.	Mnemonic	Description
39	PPMU_CMPH0	PPMU Go/No-Go Comparator Output High, Channel 0.
3	CFFA1	PPMU External Compensation Capacitor Pin A, Channel 1.
2	CFFB1	PPMU External Compensation Capacitor Pin B, Channel 1.
83	PPMU_S1	PPMU External Sense Connect, Channel 1.
23	PPMU_M1	PPMU Analog Measure Output, Channel 1.
26	PPMU_CMPL1	PPMU Go/No-Go Comparator Output Low, Channel 1.
25	PPMU_CMPH1	PPMU Go/No-Go Comparator Output High, Channel 1.
34	$\overline{\text{RST}}$	Reset Input (Active Low).
32	SCLK	Serial Programmable Interface (SPI) Clock Input.
30	$\overline{\text{CS}}$	Serial Programmable Interface (SPI) Chip Select Input (Active Low).
33	SDI	Serial Programmable Interface (SPI) Serial Data Input.
31	SDO	Serial Programmable Interface (SPI) Serial Data Output.
29	$\overline{\text{ALARM}}$	Fault Alarm Open-Drain Output (Open-Collector, Active Low).
35	$\overline{\text{BUSY}}$	Serial Programmable Interface (SPI) Busy Output (Open-Collector, Active Low).
19	VREF	DAC Precision 2.500 V Reference Input.
20	VREFGND	DAC Precision 0.000 V Reference Input.
24	DUTGND	DUT Ground Sense Input.
68	DUT0	DUT Pin, Channel 0.
80	DUT1	DUT Pin, Channel 1.
45	VCCTHERM	Temperature Sensor VCC Supply (8.0 V).
44	VTHERM	Temperature Sensor Analog Output.
16, 48, 66, 67, 72, 76, 81, 82	VCC, VCCD0, VCCD1	Analog Supply (8.0 V).
27, 37	VDD	Digital Supply (1.8 V).
22, 40, 42, 74	AGND	Analog Ground (Quiet).
28, 36	DGND	Digital Ground.
4, 10, 18, 21, 43, 46, 54, 60, 71, 77	PGND	Power Ground.
17, 47, 64, 69, 70, 73, 75, 78, 79, 84	VEE, VEED0, VEED1	Analog Supply (−5.0 V).
1, 63	NC	No Connect. These pins can be grounded or left floating.
	EP	Exposed Pad. The exposed pad is internally connected via a high impedance die attached to VEE (substrate).

TYPICAL PERFORMANCE CHARACTERISTICS

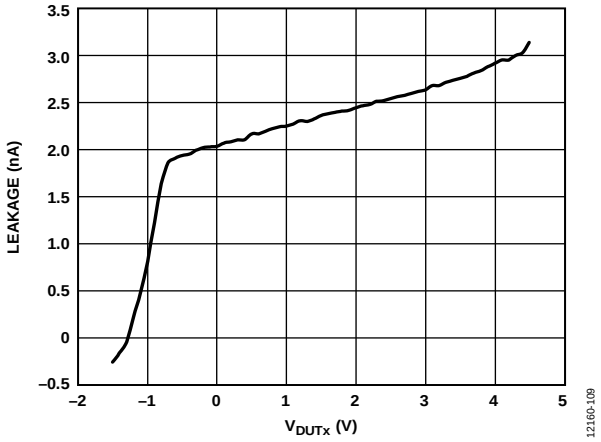


Figure 9. DUTx Pin Leakage in High-Z Mode

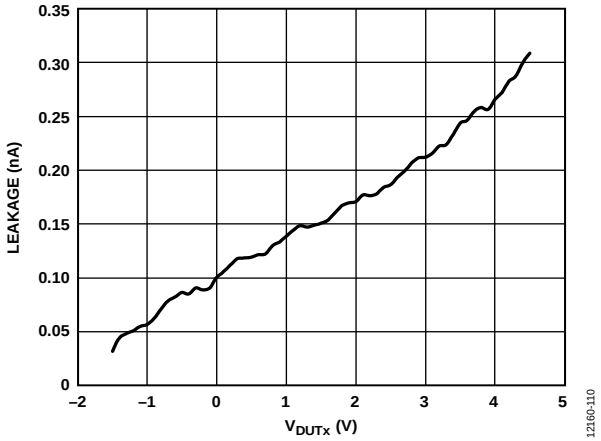


Figure 10. DUTx Pin Leakage in Low Leakage Mode

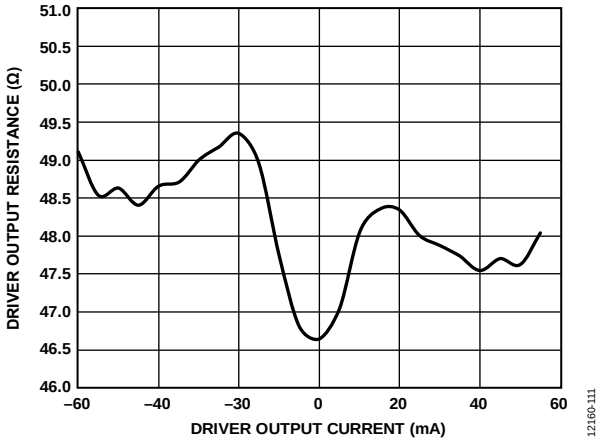


Figure 11. Driver Output Resistance vs. Driver Output Current

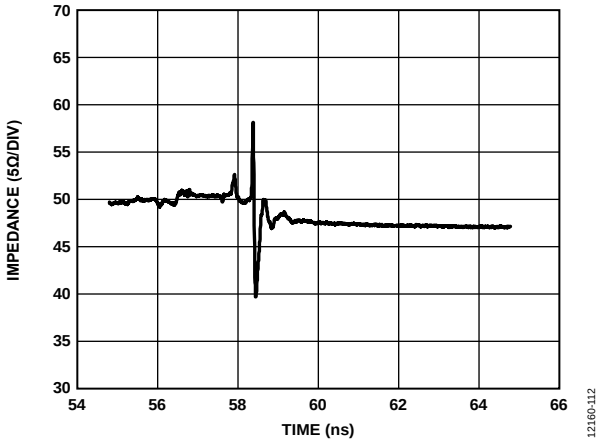


Figure 12. DUTx Pin Time-Domain Reflectometry (TDR) Response

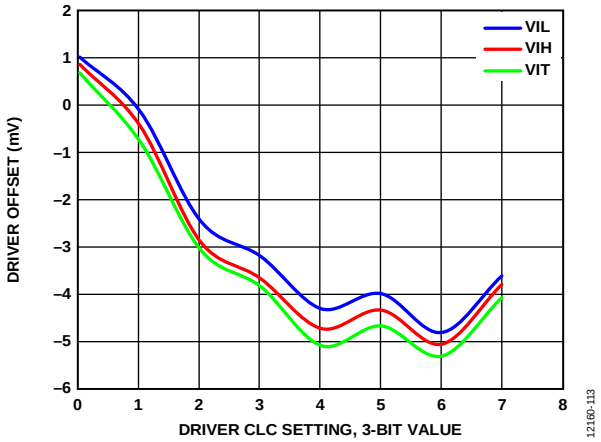


Figure 13. Driver Offset vs. Driver CLC Setting, 3-Bit Value

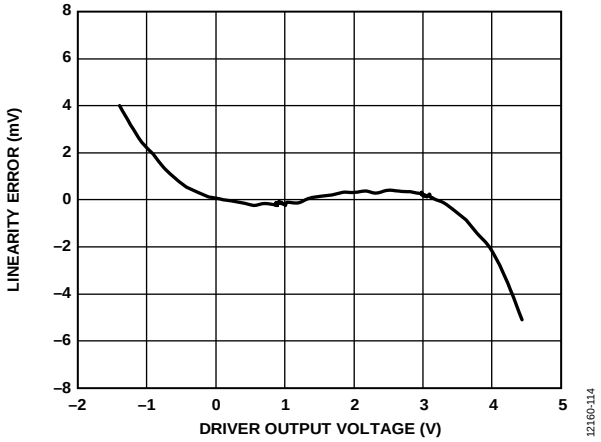


Figure 14. Driver VIH INL

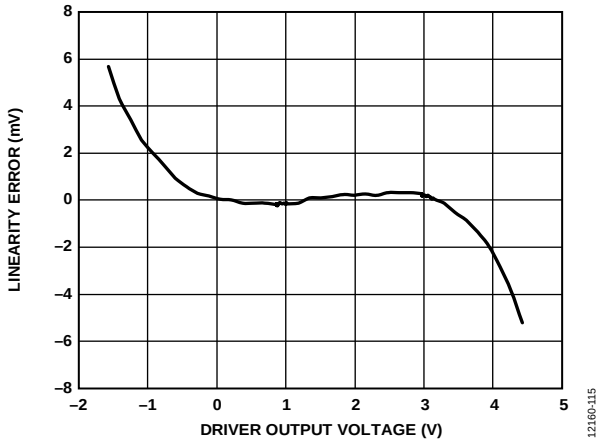


Figure 15. Driver VIL INL

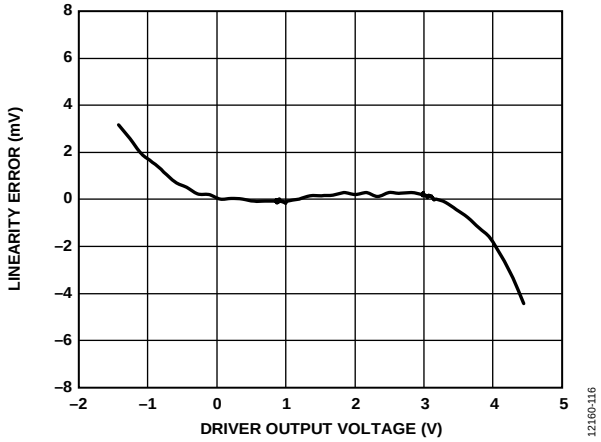


Figure 16. Driver VIT INL

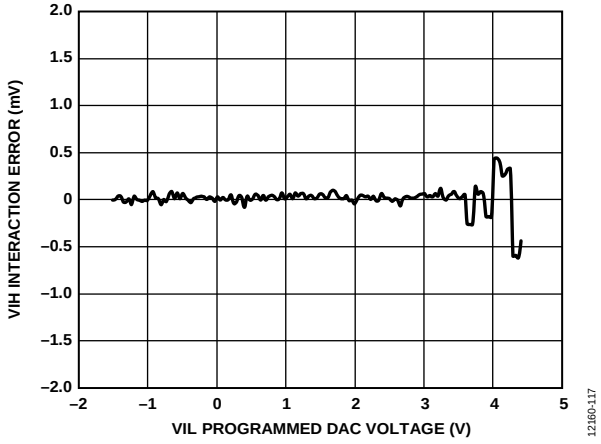


Figure 17. Driver VIH Interaction Error vs. VIL Programmed DAC Voltage

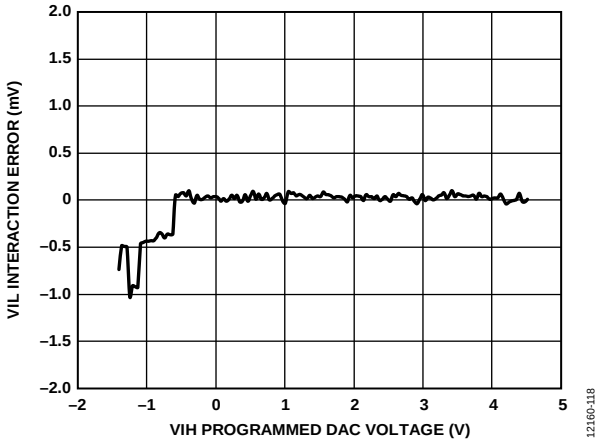


Figure 18. Driver VIL Interaction Error vs. VIH Programmed DAC Voltage

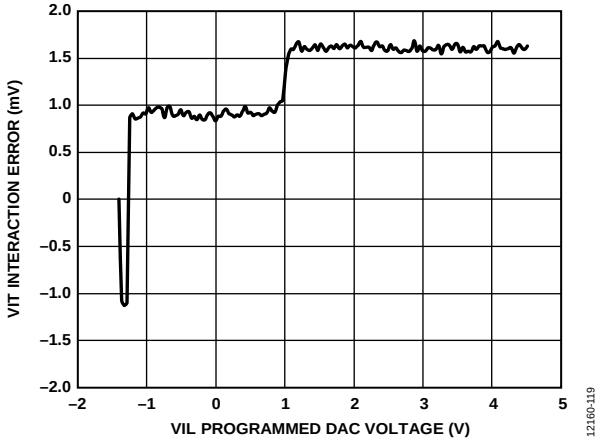


Figure 19. Driver VIT Interaction Error vs. VIH Programmed DAC Voltage

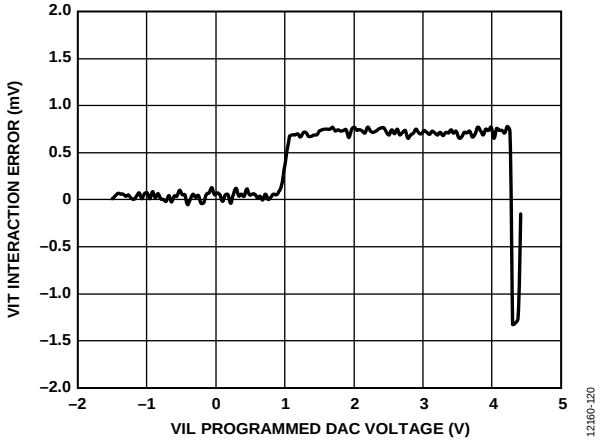


Figure 20. Driver VIT Interaction Error vs. VIL Programmed DAC Voltage

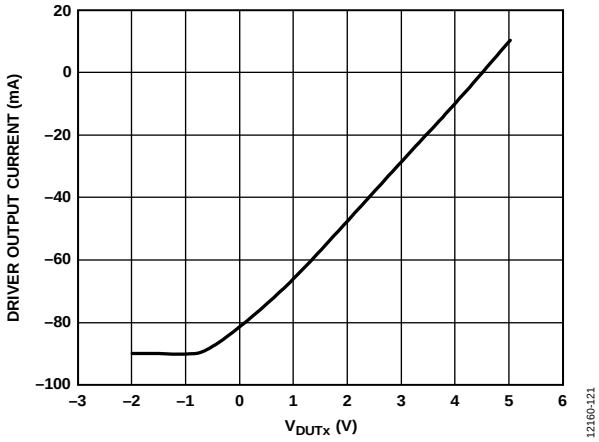


Figure 21. Driver Output Current Limit, Sink

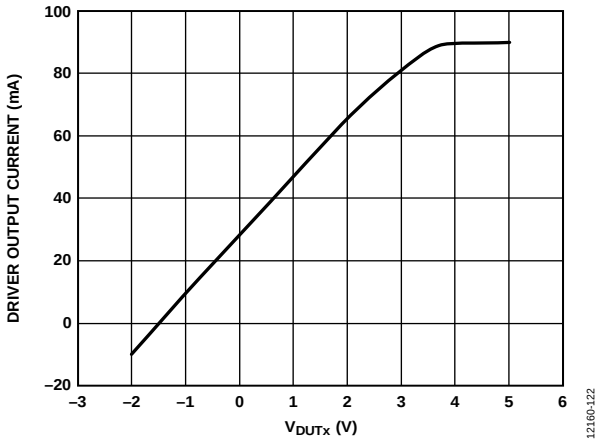


Figure 22. Driver Output Current Limit, Source

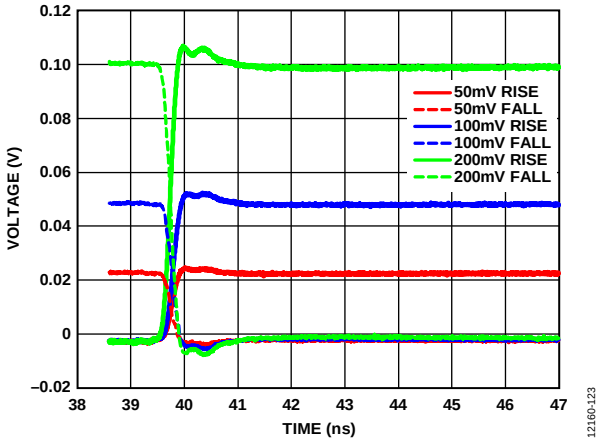


Figure 23. Driver Small Swing Response

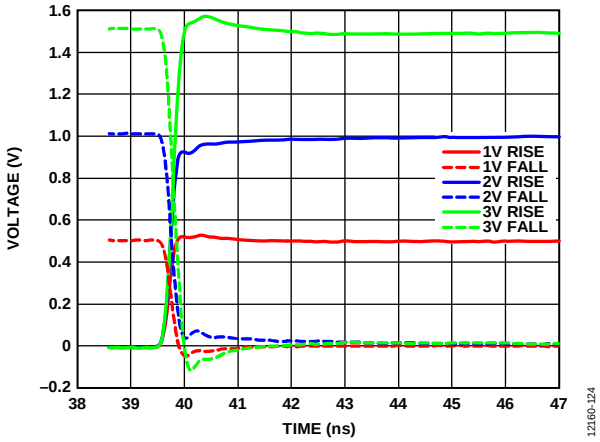


Figure 24. Driver Large Swing Response

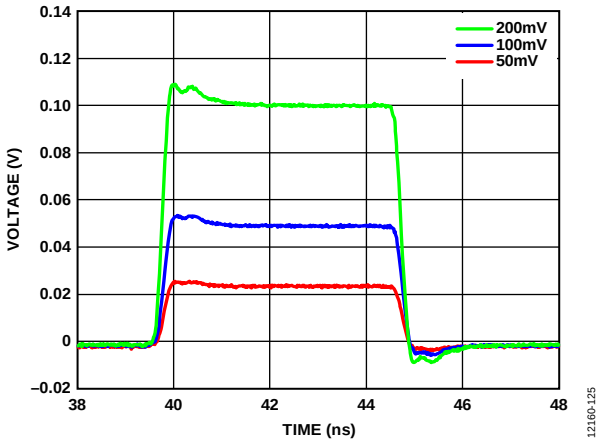


Figure 25. Driver 100 MHz Response, Small Swing

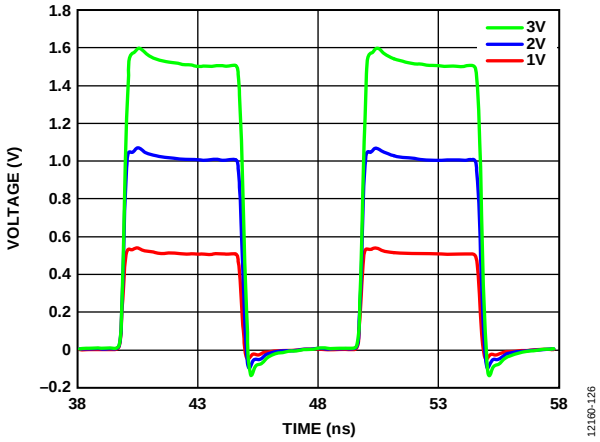


Figure 26. Driver 100 MHz Response, Large Swing

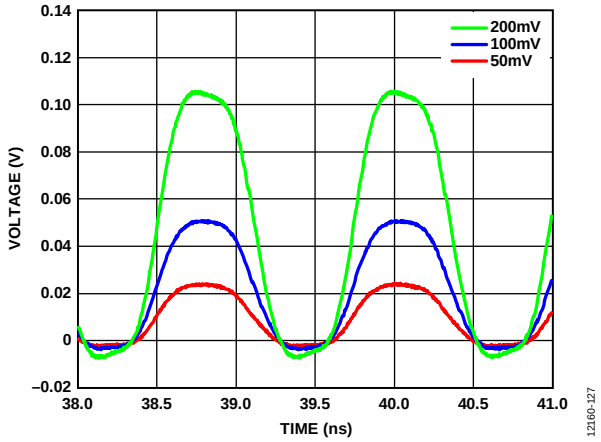


Figure 27. Driver 800 MHz Response, Small Swing

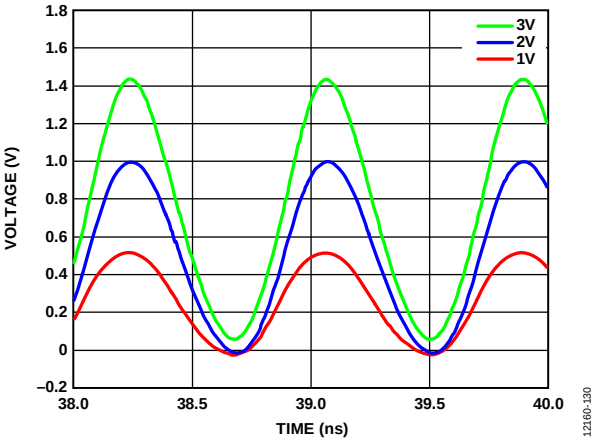


Figure 30. Driver 1.25 GHz Response, Large Swing

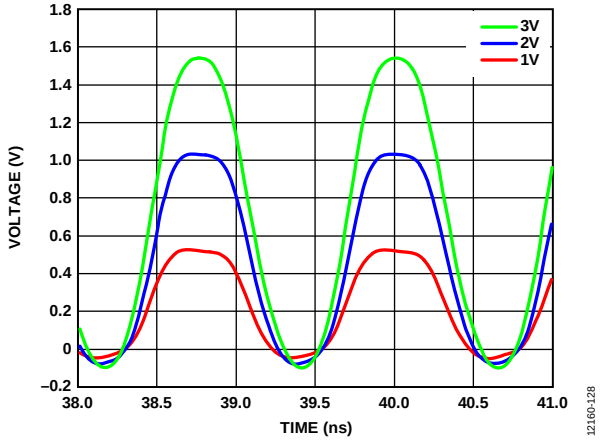


Figure 28. Driver 800 MHz Response, Large Swing

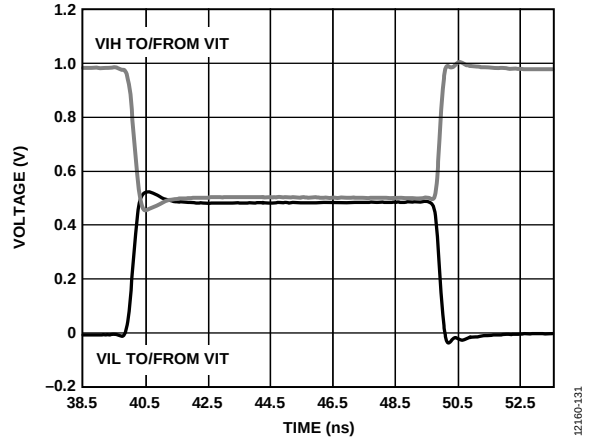


Figure 31. Driver VIL/VIH to/from VIT, VIH = 2.0 V, VIL = 0.0 V, VIT = 1.0 V; 50 Ω Terminated

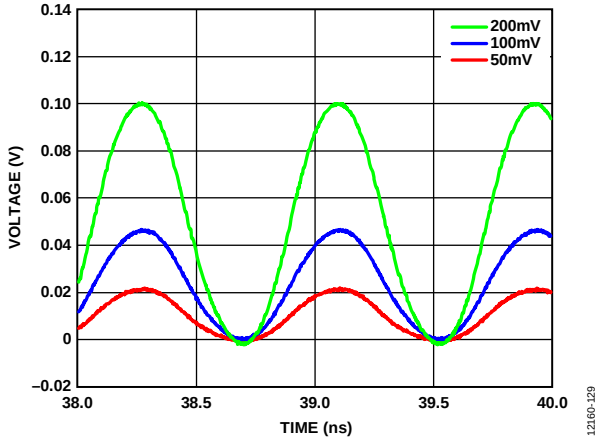


Figure 29. Driver 1.25 GHz Response, Small Swing

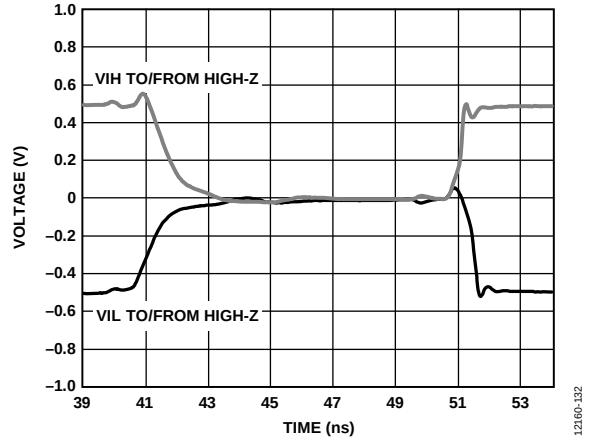


Figure 32. Driver VIL/VIH to/from High-Z, VIH = 1.0 V, VIL = −1.0 V; 50 Ω Terminated

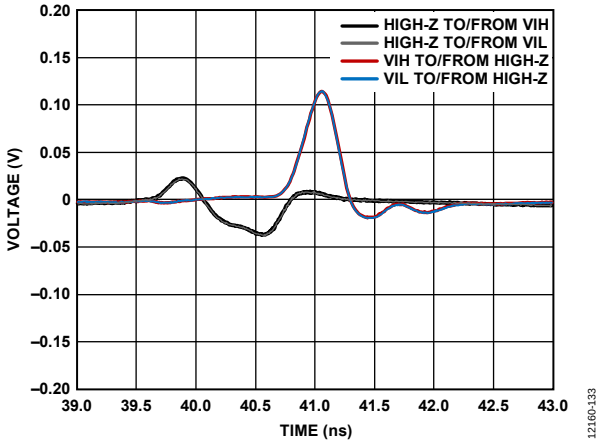


Figure 33. Driver to/from High-Z Transient Spike, VIH = VIL = 0.0 V; 50 Ω Terminated

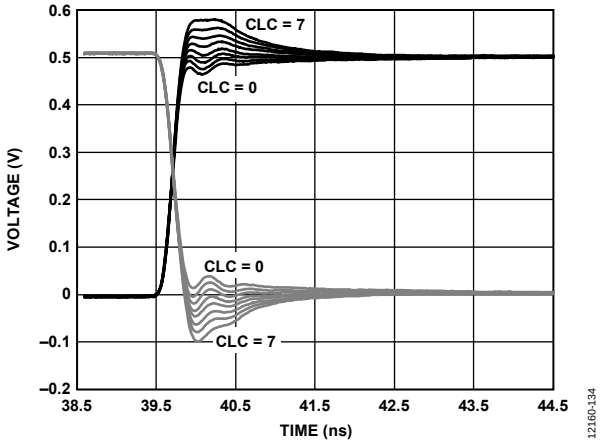


Figure 34. Driver Transition vs. CLC, VIH = 1.0 V, VIL = 0.0 V; 50 Ω Terminated

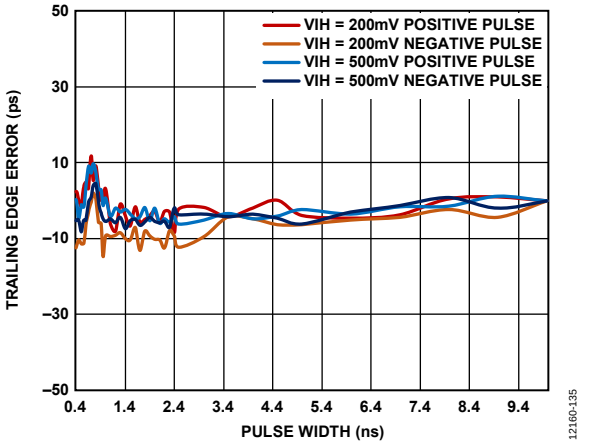


Figure 35. Driver Pulse Width (Positive/Negative) Trailing Edge Timing Error, VIH = 0.2 V, 0.5 V; VIL = 0.0 V; CLC = Midscale; 50 Ω Terminated

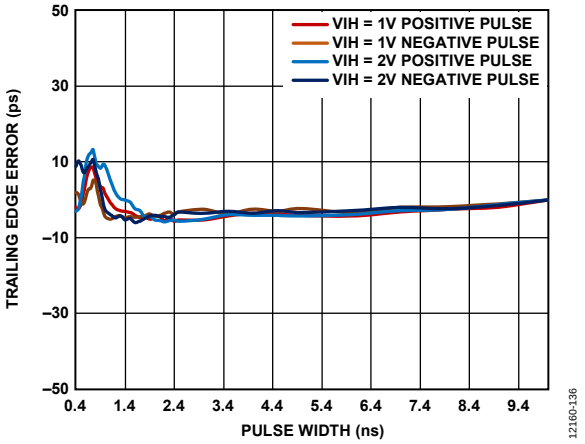


Figure 36. Driver Pulse Width (Positive/Negative) Trailing Edge Timing Error, VIH = 1.0 V, 2.0 V; VIL = 0.0 V; CLC = Midscale; 50 Ω Terminated

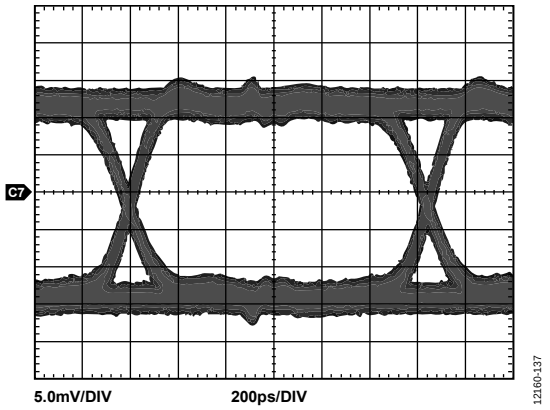


Figure 37. Driver Eye Diagram, 800 Mbps, PRBS31, VIH = 50 mV, VIL = 0.0 V; 50 Ω Terminated

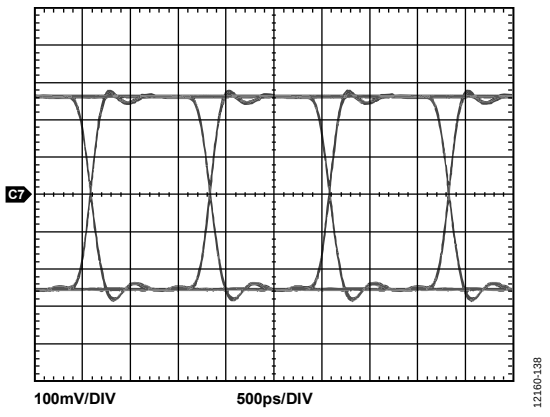


Figure 38. Driver Eye Diagram, 800 Mbps, PRBS31, VIH = 1.0 V, VIL = 0.0 V; 50 Ω Terminated

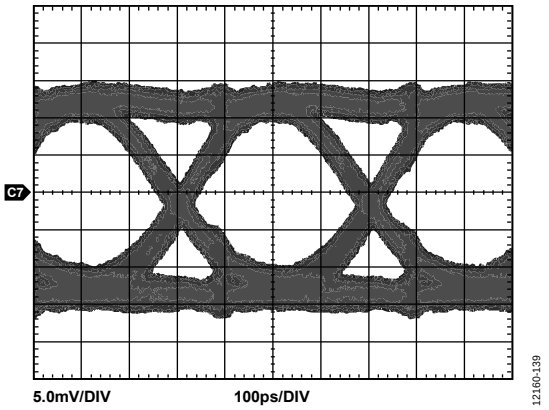


Figure 39. Driver Eye Diagram, 2.5 Gbps, PRBS31, VIH = 50 mV, VIL = 0.0 V; 50 Ω Terminated

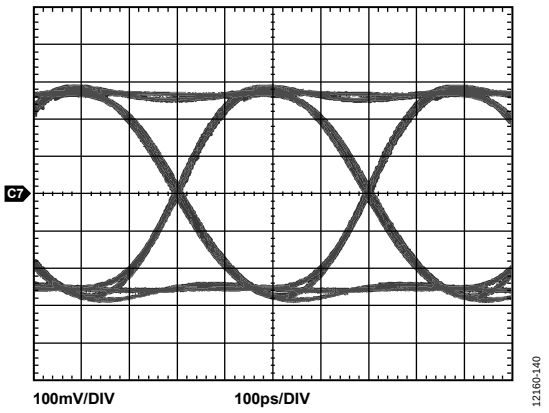


Figure 40. Driver Eye Diagram, 2.5 Gbps, PRBS31, VIH = 1.0 V, VIL = 0.0 V; 50 Ω Terminated

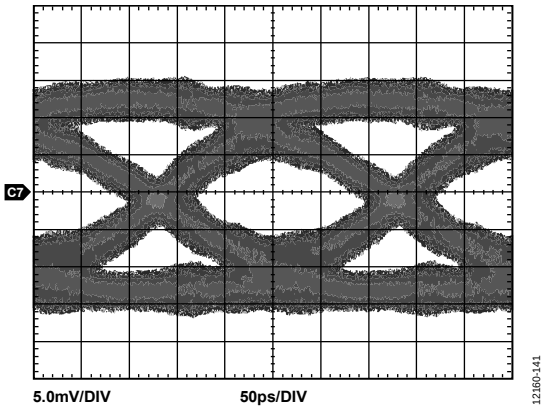


Figure 41. Driver Eye Diagram, 4.0 Gbps, PRBS31, VIH = 50 mV, VIL = 0.0 V; 50 Ω Terminated

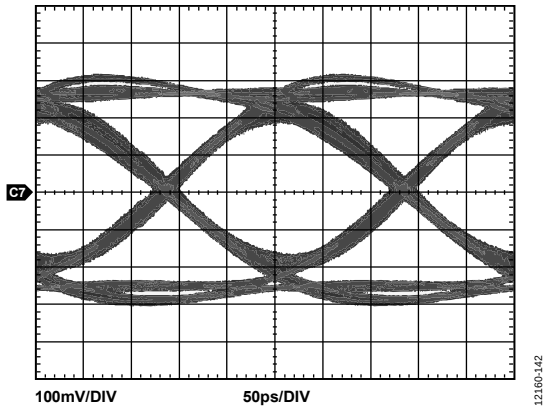


Figure 42. Driver Eye Diagram, 4.0 Gbps, PRBS31, VIH = 1.0 V, VIL = 0.0 V; 50 Ω Terminated

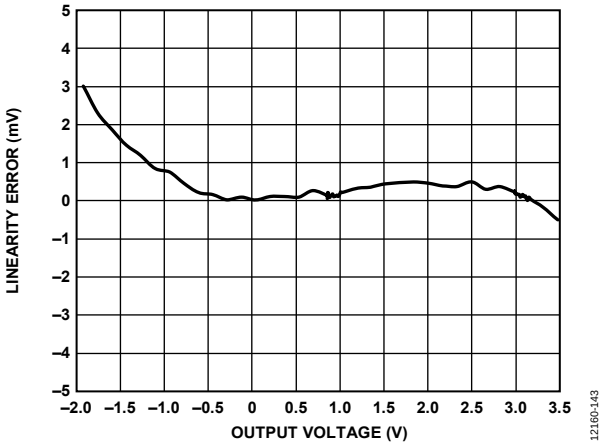


Figure 43. Reflection Clamp VCLx INL

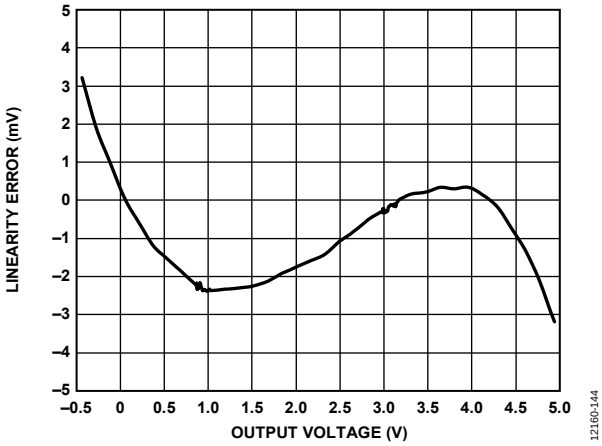


Figure 44. Reflection Clamp VCHx INL

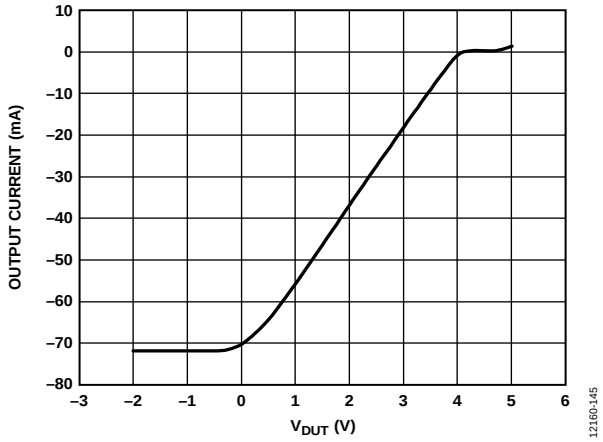


Figure 45. Reflection Clamp Current Limit, VCHx = 5.0 V, VCLx = 4.0 V; V_{DUTx} Swept from −2.0 V to +5.0 V

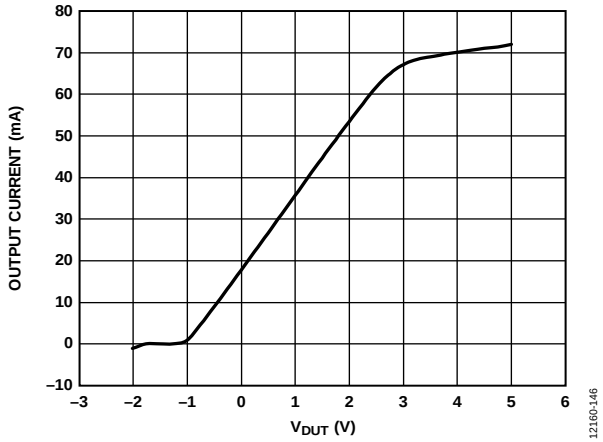


Figure 46. Reflection Clamp Current Limit, VCHx = −1.0 V, VCLx = −2.0 V; V_{DUTx} Swept from −2.0 V to +5.0 V

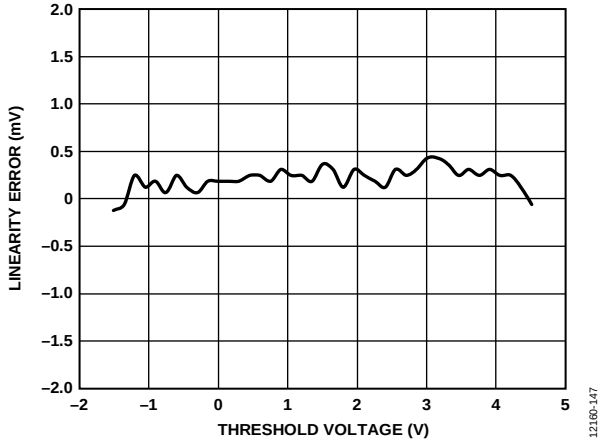


Figure 47. Normal Window Comparator Threshold INL

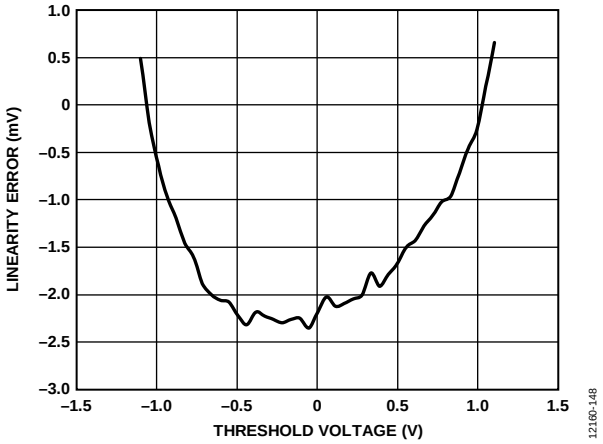


Figure 48. Differential Mode Comparator Threshold INL

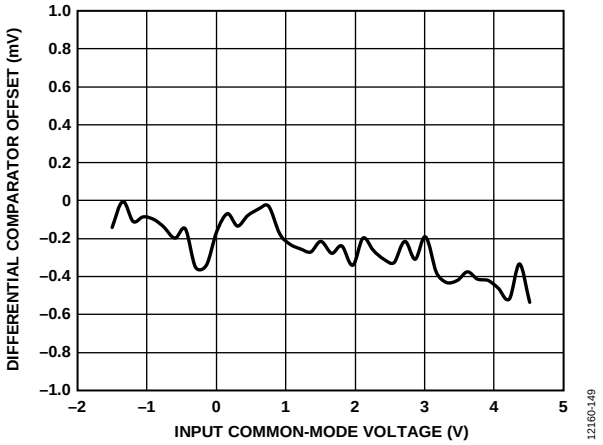


Figure 49. Differential Mode Comparator Common-Mode Rejection Error

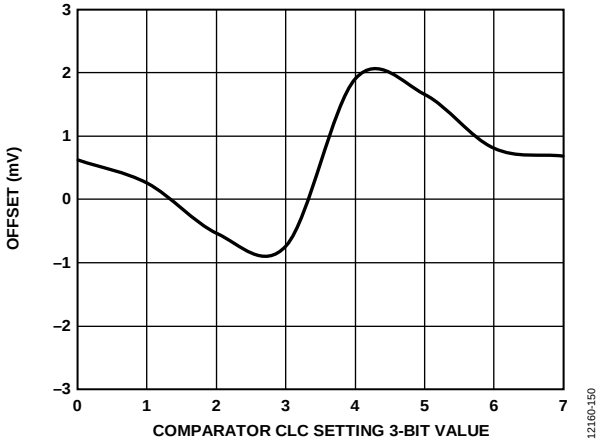


Figure 50. Normal Window Comparator Offset Error vs. CLC Setting

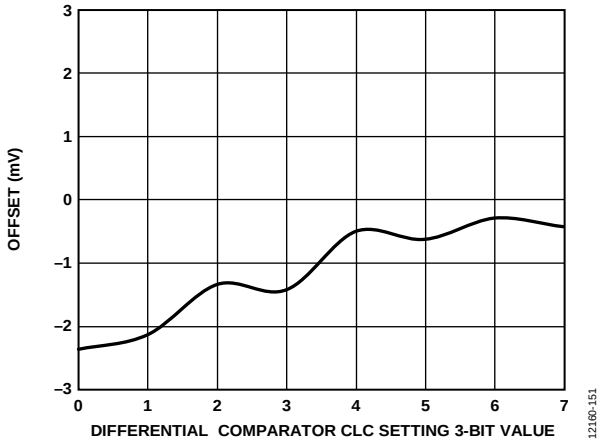


Figure 51. Differential Mode Comparator Offset Error vs. CLC Setting

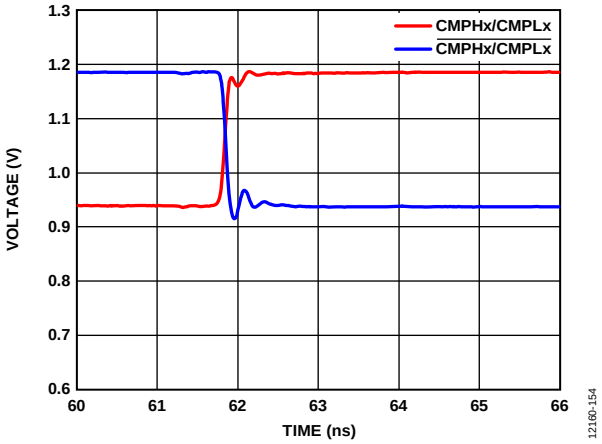


Figure 54. Comparator CML Output Waveform (ADATE320)

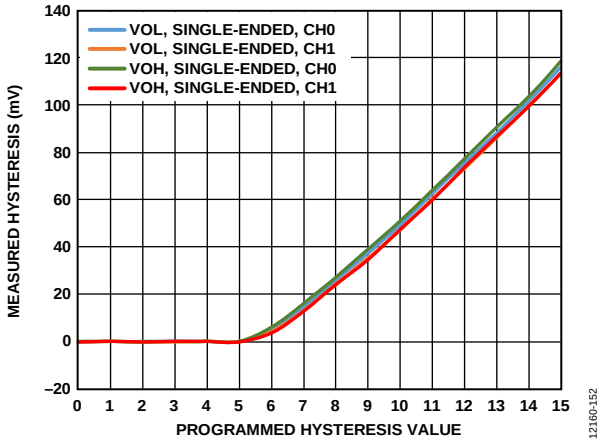


Figure 52. Normal Window Comparator Hysteresis vs. Programmed Hysteresis Value

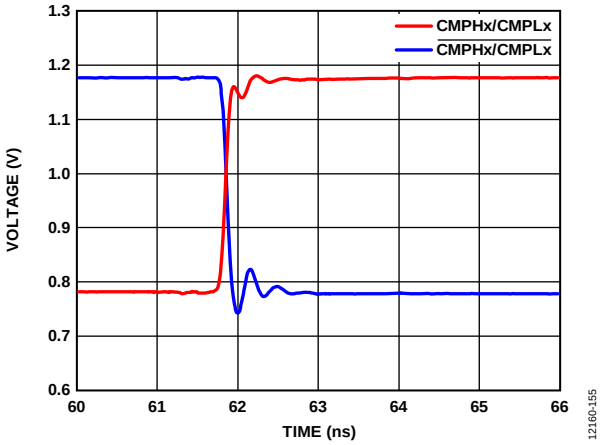


Figure 55. Comparator CML Output Waveform (ADATE320-1)

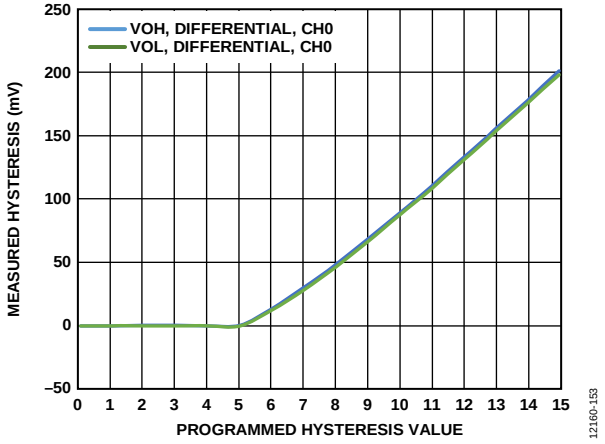


Figure 53. Differential Mode Comparator Hysteresis vs. Programmed Hysteresis Value

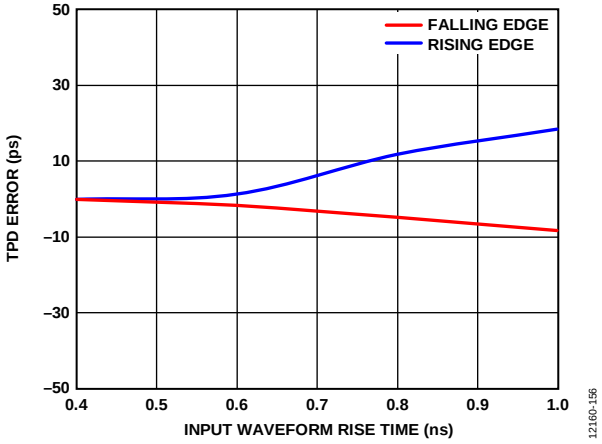


Figure 56. Normal Window Comparator Propagation Delay vs. Input Rise Time, 1.0 V Input Swing

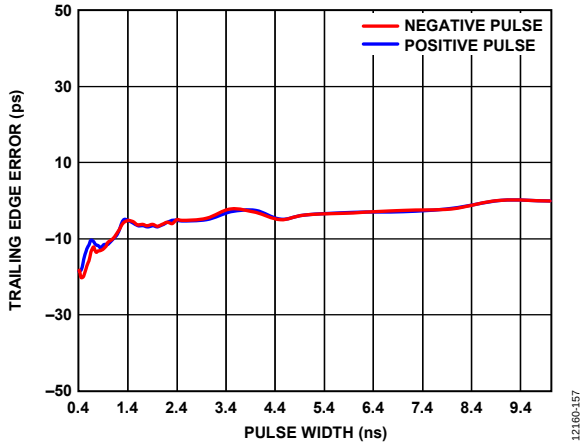


Figure 57. Normal Window Comparator Pulse Width (Positive/Negative) Trailing Edge Timing Error, 1.0 V Input Swing

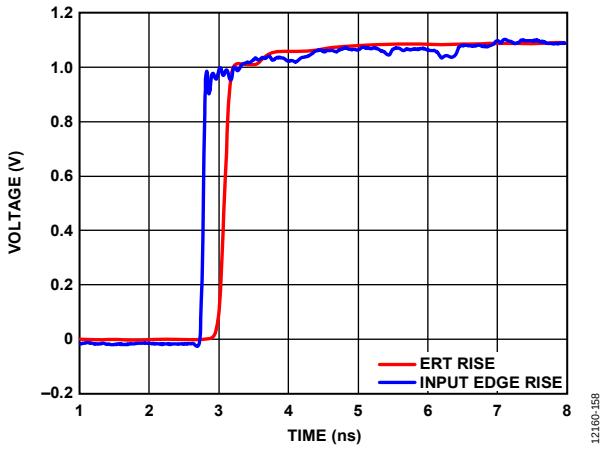


Figure 58. Normal Window Comparator Equivalent Rise Time (ERT), 1.0 V Input Swing, 50 ps 20% to 80%; 50 Ω Terminated

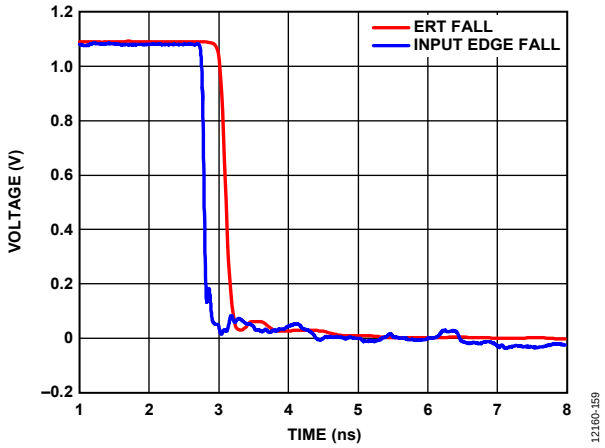


Figure 59. Normal Window Comparator Equivalent Fall Time (EFT), 1.0 V Input Swing, 50 ps 20% to 80%; 50 Ω Terminated

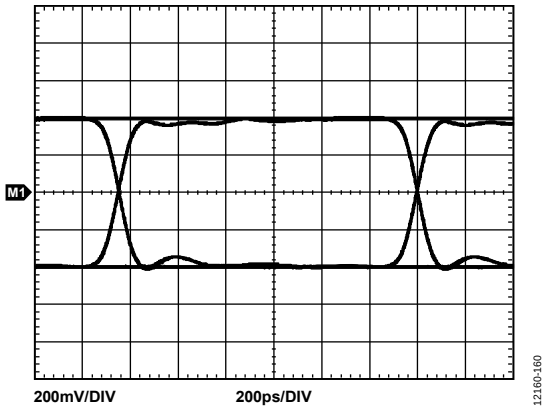


Figure 60. Normal Window Comparator Eye Diagram, 800 Mbps, PRBS31, 1.0 V Input Swing; 50 Ω Terminated

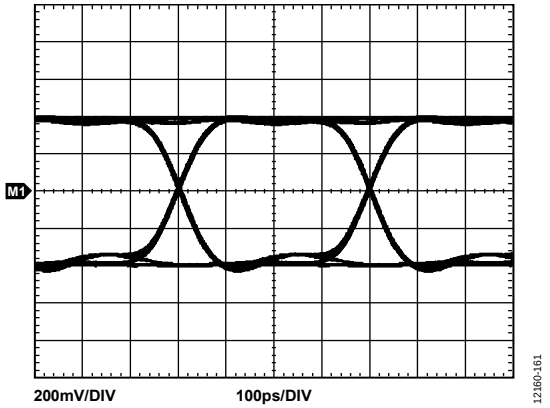


Figure 61. Normal Window Comparator Eye Diagram, 2.5 Gbps, PRBS31, 1.0 V Input Swing; 50 Ω Terminated

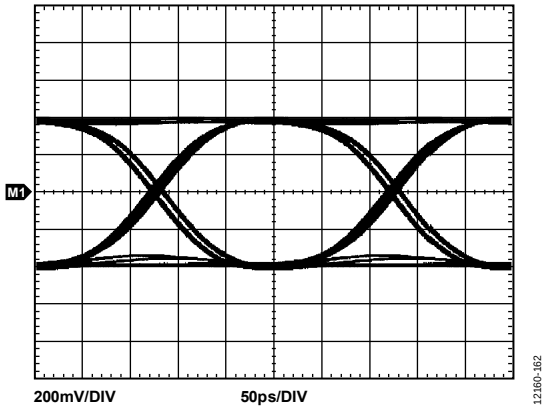


Figure 62. Normal Window Comparator Eye Diagram, 4.0 Gbps, PRBS31, 1.0 V Input Swing; 50 Ω Terminated

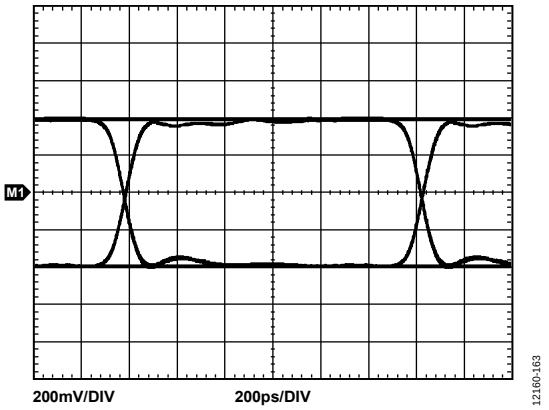


Figure 63. Differential Mode Comparator Eye Diagram, 800 Mbps, PRBS31, 1.0 V Input Swing; 50 Ω Terminated

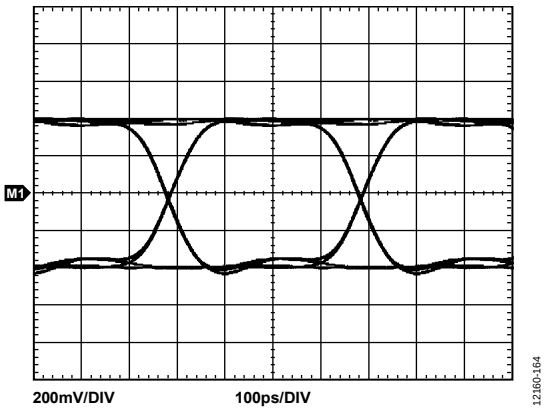


Figure 64. Differential Mode Comparator Eye Diagram, 2.5 Gbps, PRBS31, 1.0 V Input Swing; 50 Ω Terminated

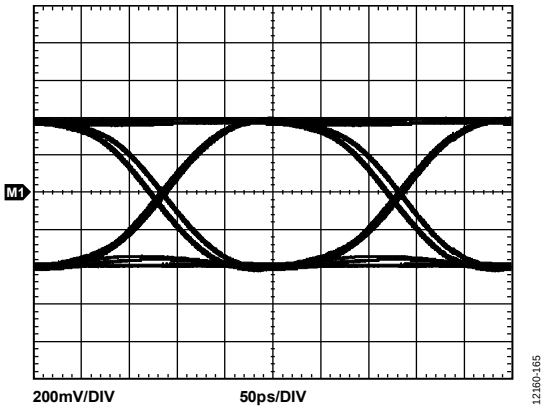


Figure 65. Differential Mode Comparator Eye Diagram, 4.0 Gbps, PRBS31, 1.0 V Input Swing; 50 Ω Terminated

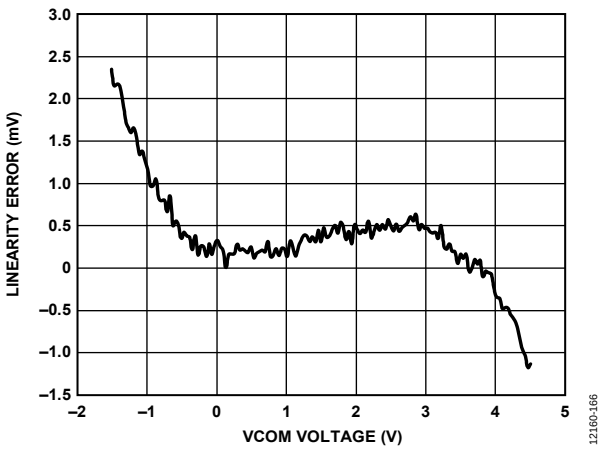


Figure 66. Active Load VCOM INL

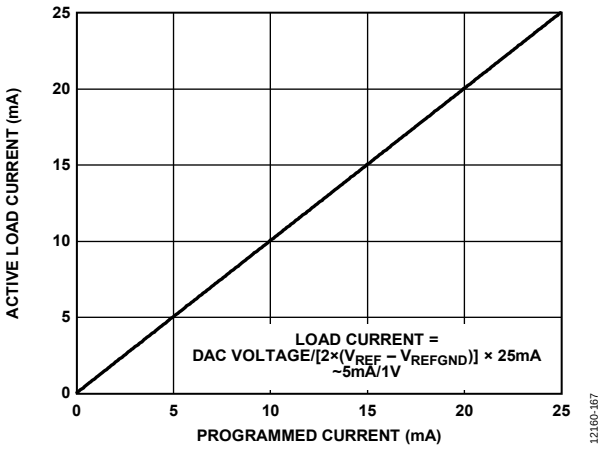


Figure 67. Active Load IOHx/IOLx Transfer Function

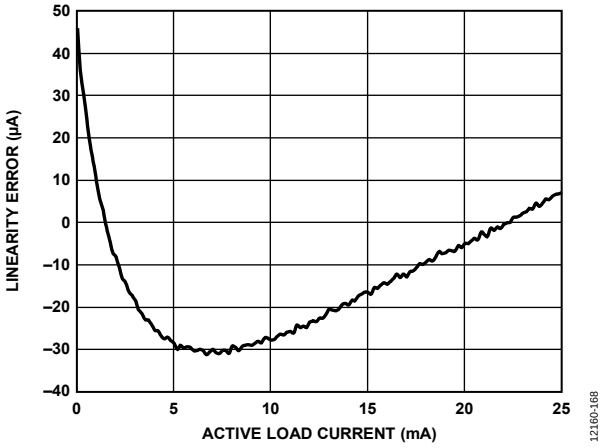


Figure 68. Active Load IOHx INL

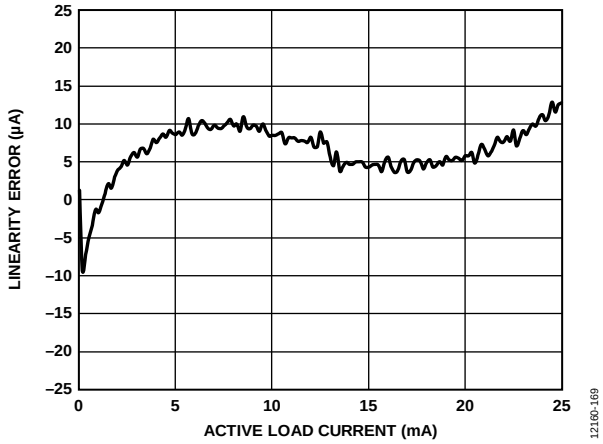


Figure 69. Active Load IOLx INL

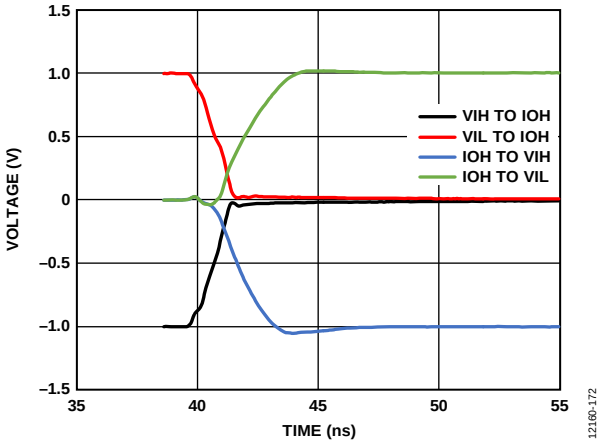


Figure 72. Active Load IOHx to/from Driver Transient Response, VIH = VIL = 0.0 V, IOHx = IOLx = 20 mA; 50 Ω Terminated

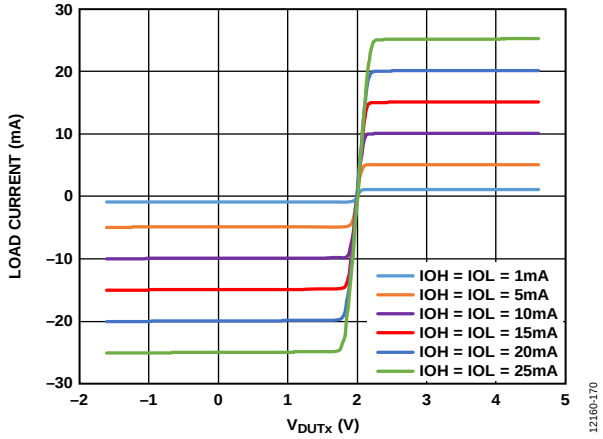


Figure 70. Active Load Commutation Response, VCOM = 2.0 V

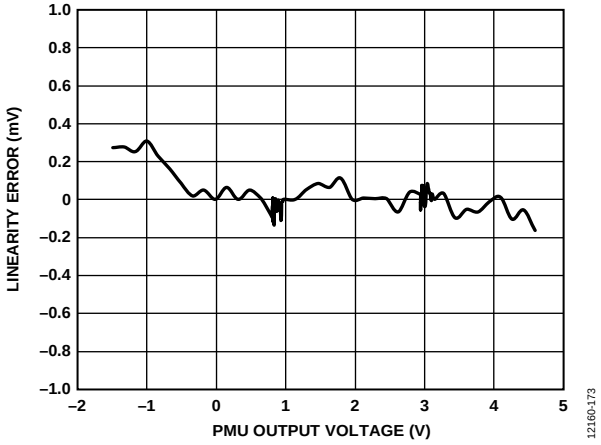


Figure 73. PPMU Force Voltage INL, All Ranges

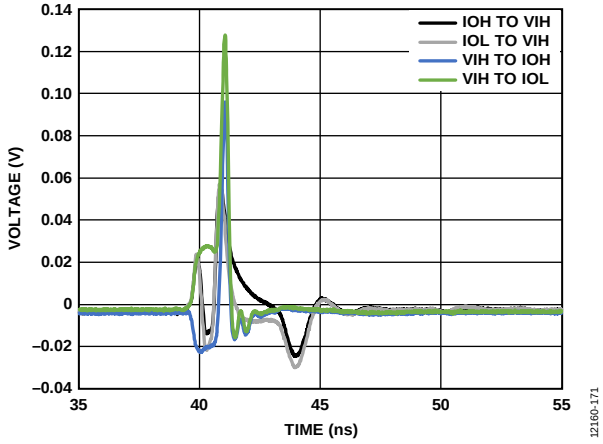


Figure 71. Active Load to/from Driver Input/Output Spike, VIH = VIL = 0.0 V, IOHx = IOLx = 0.0 mA; 50 Ω Terminated

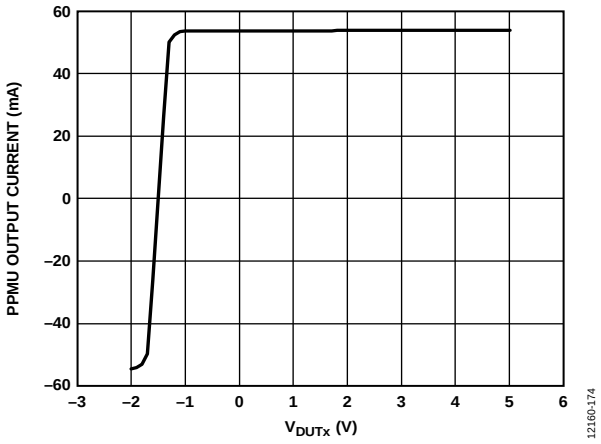


Figure 74. PPMU Force Voltage Output Current Limit, Range A, FV = −1.5 V, V_{DUTx} Swept −2.0 V to +5.0 V

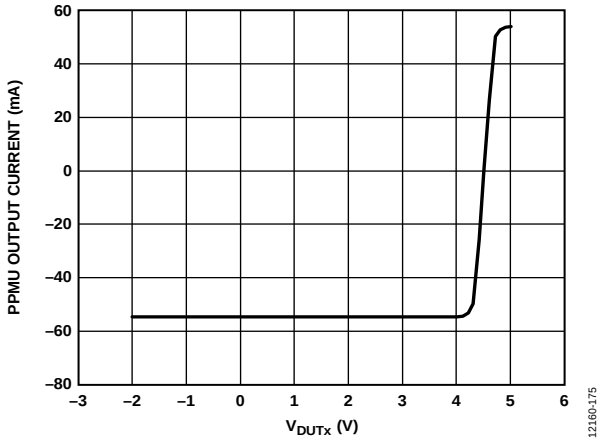


Figure 75. PPMU Force Voltage Output Current Limit, Range A, FV = 4.5 V, V_{DUTx} Swept −2.0 V to +5.0 V

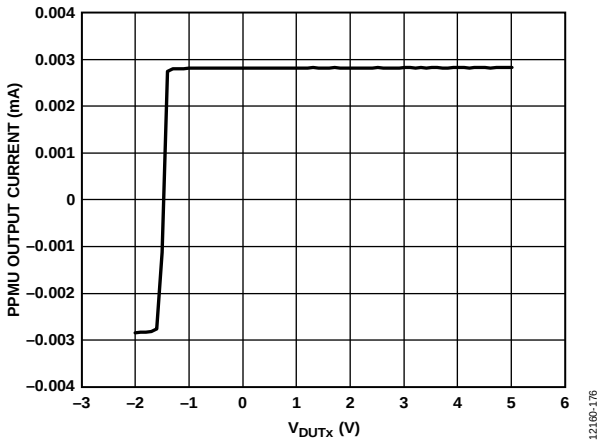


Figure 76. PPMU Force Voltage Output Current Limit, Range E, FV = −1.5 V, V_{DUTx} Swept −2.0 V to +5.0 V

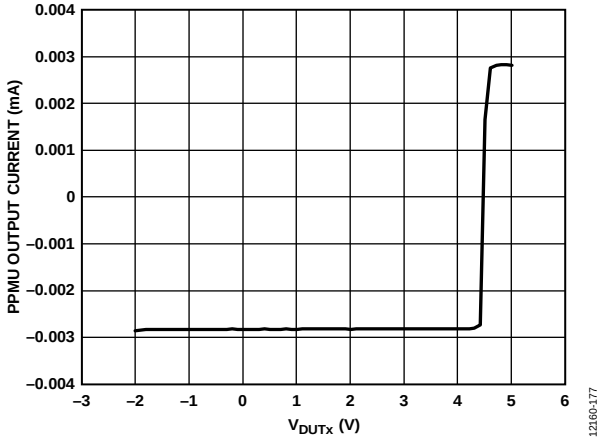


Figure 77. PPMU Force Voltage Output Current Limit, Range E, FV = 4.5 V, V_{DUTx} Swept −2.0 V to +5.0 V

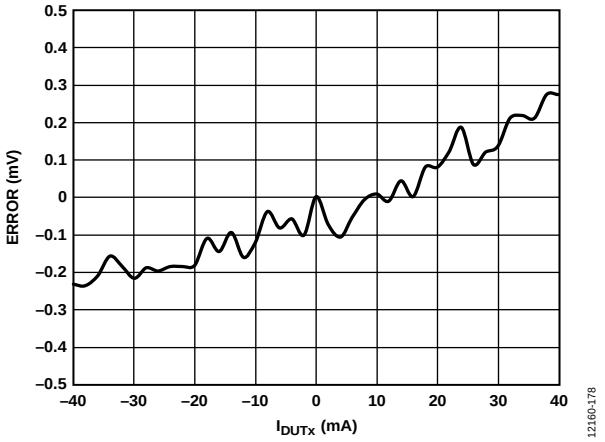


Figure 78. PPMU Force Voltage Compliance Error, Range A, FV = −1.0 V vs. Output Current, Internal Sense

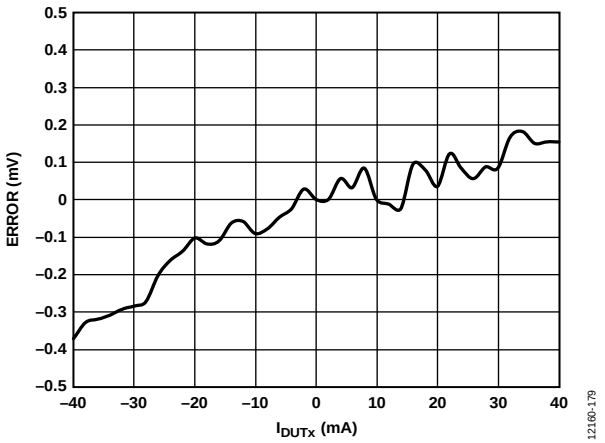


Figure 79. PPMU Force Voltage Compliance Error, Range A, FV = 4.0 V vs. Output Current (I_{DUTx}) , Internal Sense

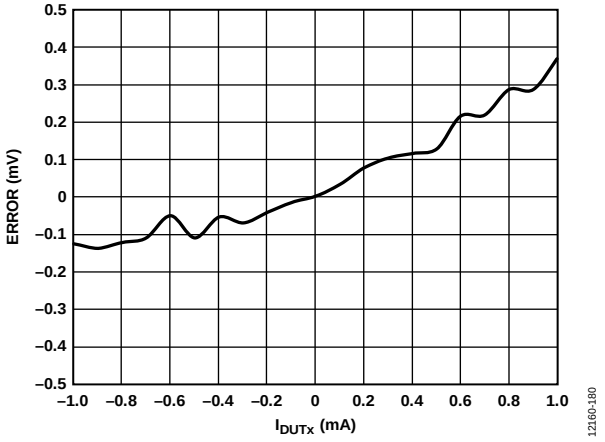


Figure 80. PPMU Force Voltage Compliance Error, Range B, FV = −1.5 V vs. Output Current(I_{DUTx}), Internal Sense

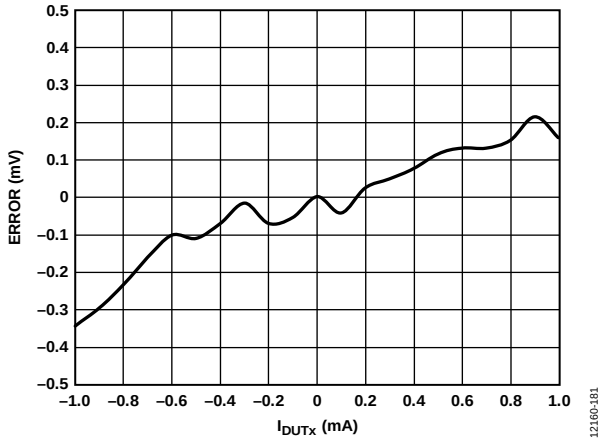


Figure 81. PPMU Force Voltage Compliance Error, Range B, FV = 4.5 V vs. Output Current (I_{DUTx}), Internal Sense

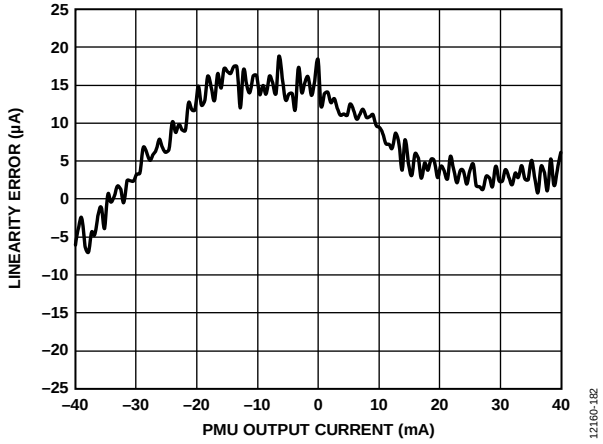


Figure 82. PPMU Force Current INL, Range A

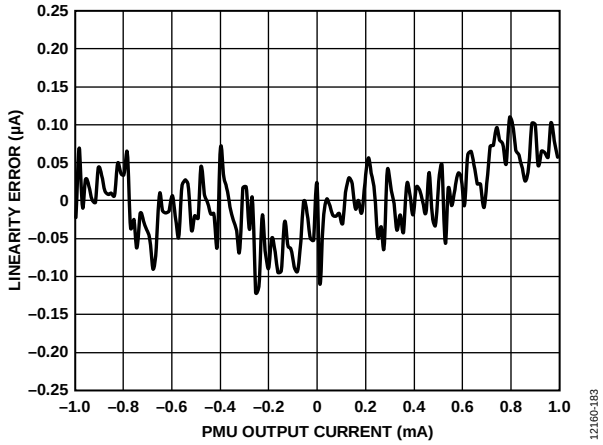


Figure 83. PPMU Force Current INL, Range B

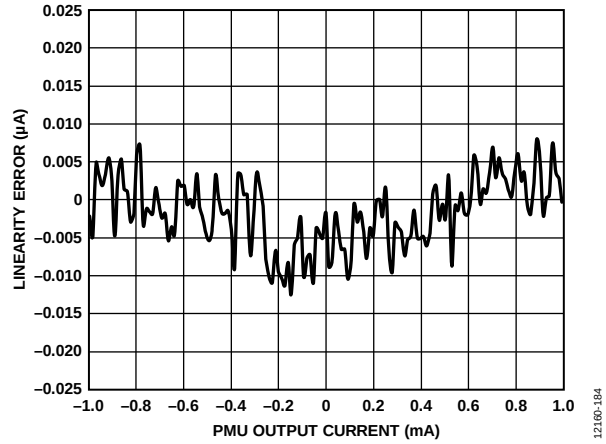


Figure 84. PPMU Force Current INL, Range C

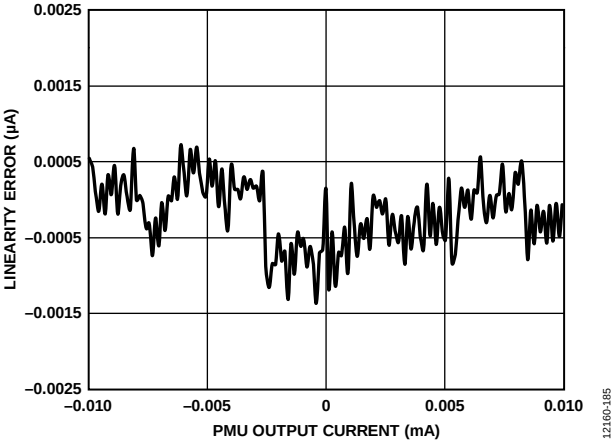


Figure 85. PPMU Force Current INL, Range D

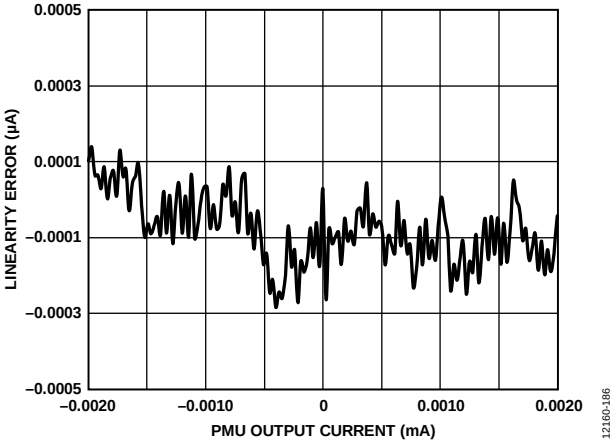


Figure 86. PPMU Force Current INL, Range E

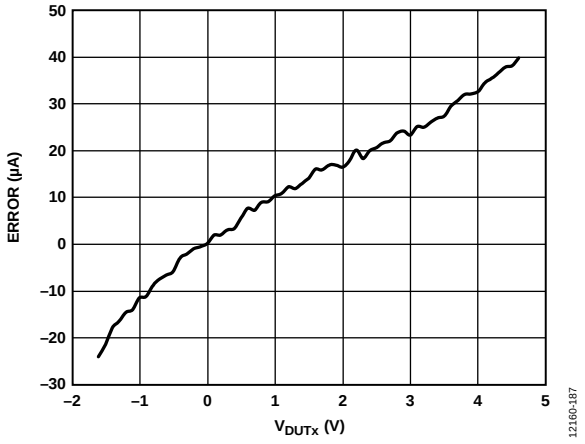


Figure 87. PPMU Force Current Compliance Error, Range A, FI = −40 mA vs. Output Voltage (V_{DUTx})

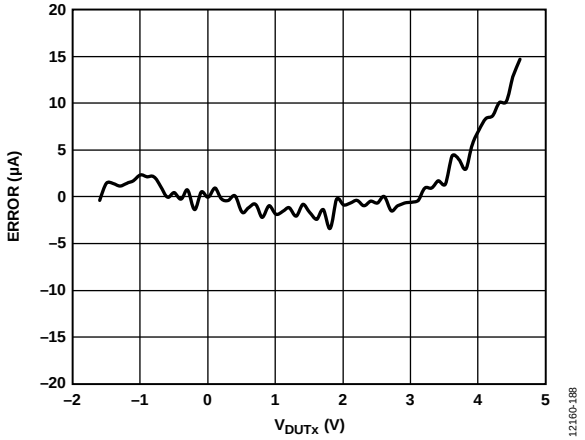


Figure 88. PPMU Force Current Compliance Error, Range A, FI = 40 mA vs. Output Voltage (V_{DUTx})

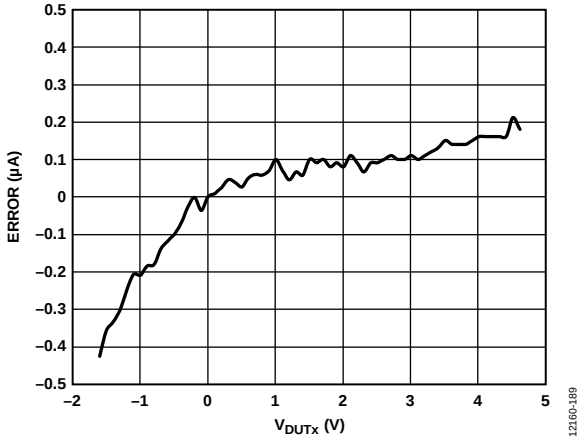


Figure 89. PPMU Force Current Compliance Error, Range B, FI = −1 mA vs. Output Voltage (V_{DUTx})

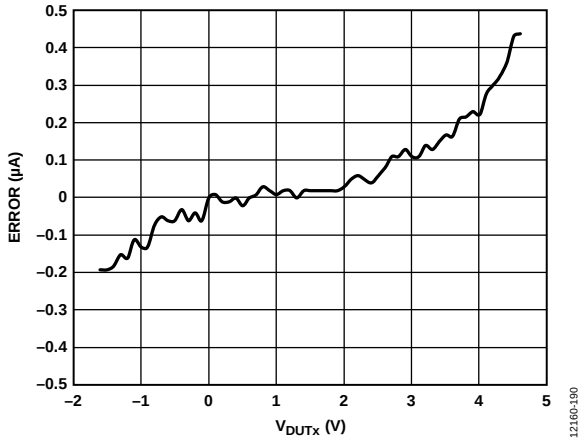


Figure 90. PPMU Force Current Compliance Error, Range B, FI = 1 mA vs. Output Voltage (V_{DUTx})

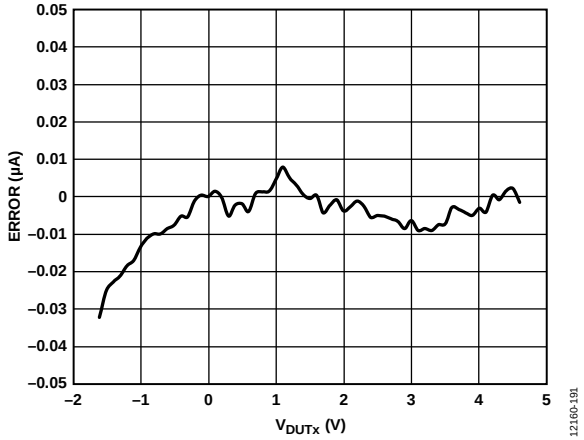


Figure 91. PPMU Force Current Compliance Error, Range C, FI = −100 µA vs. Output Voltage (V_{DUTx})

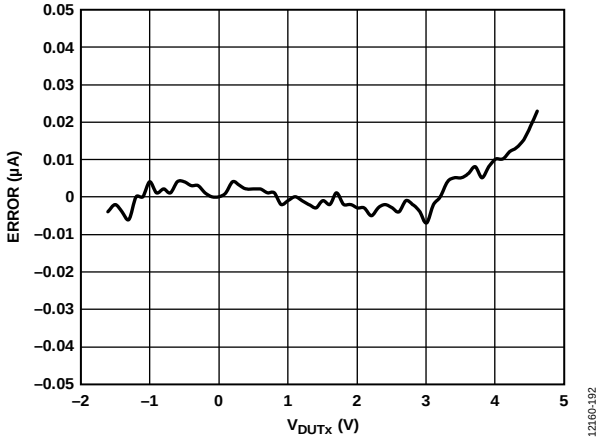


Figure 92. PPMU Force Current Compliance Error, Range C, FI = 100 µA vs. Output Voltage (V_{DUTx})

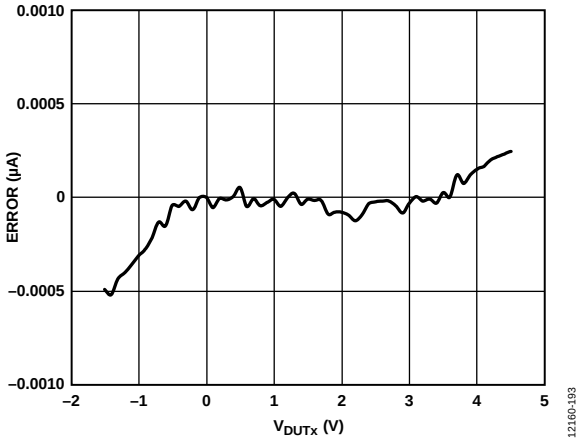


Figure 93. PPMU Force Current Compliance Error, Range E, FI = −2 µA vs. Output Voltage (V_{DUTx})

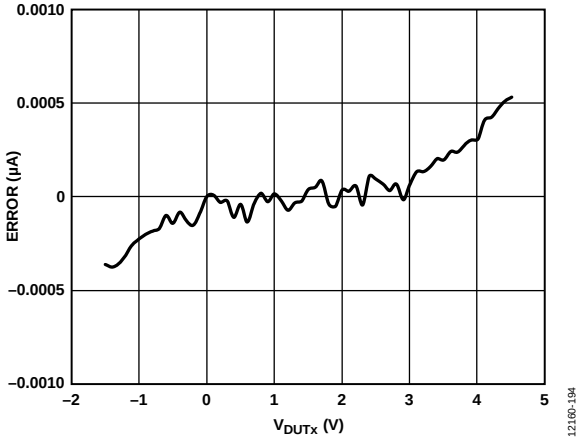


Figure 94. PPMU Force Current Compliance Error, Range E, FI = 2 µA vs. Output Voltage (V_{DUTx})

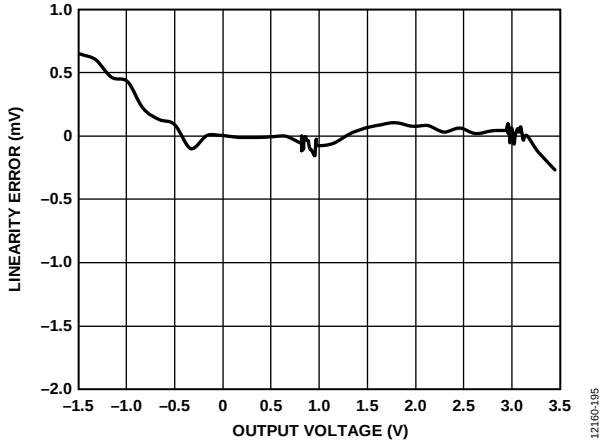


Figure 95. PPMU Voltage Clamp PCLx INL

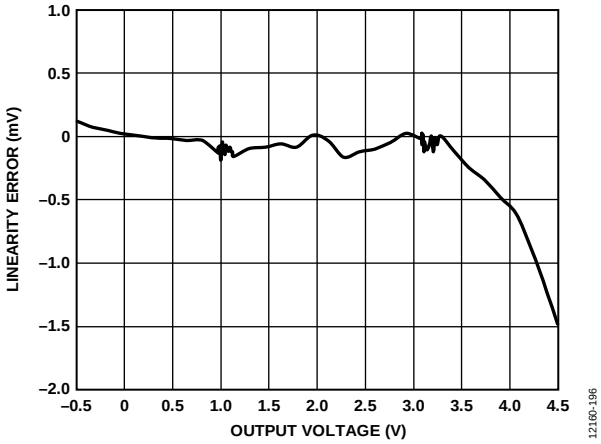


Figure 96. PPMU Voltage Clamp PCHx INL

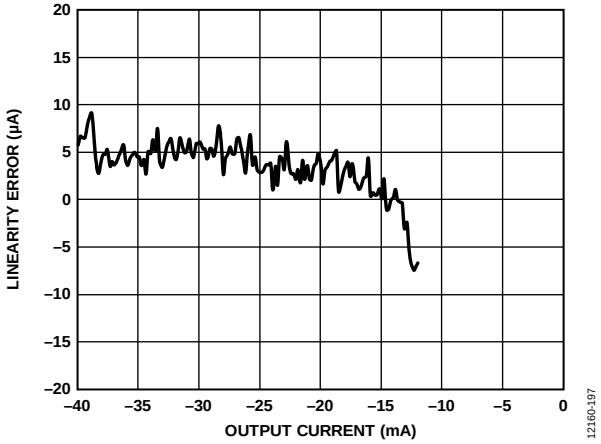


Figure 97. PPMU Current Clamp PCLx INL, Range A

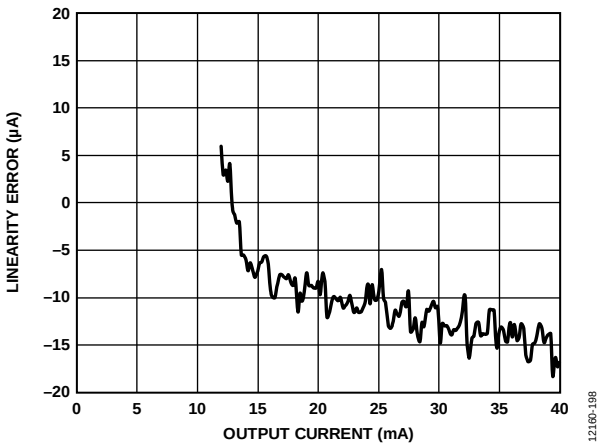


Figure 98. PPMU Current Clamp PCHx INL, Range A

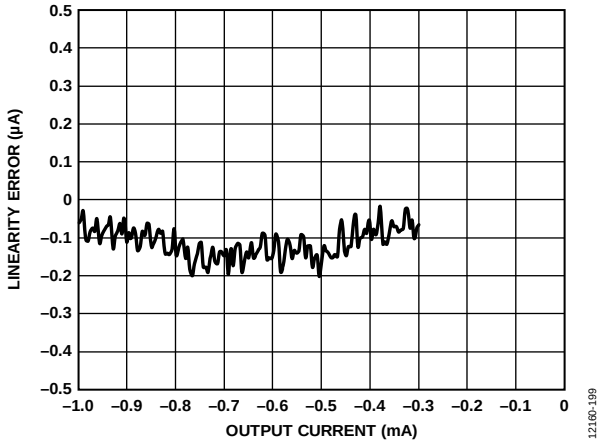


Figure 99. PPMU Current Clamp PCLx INL, Range B

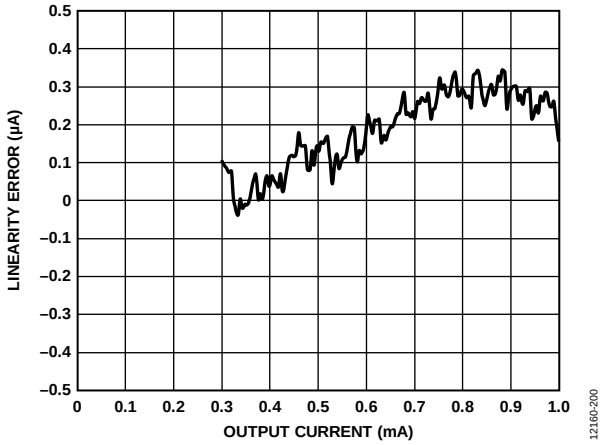


Figure 100. PPMU Current Clamp PCHx INL, Range B

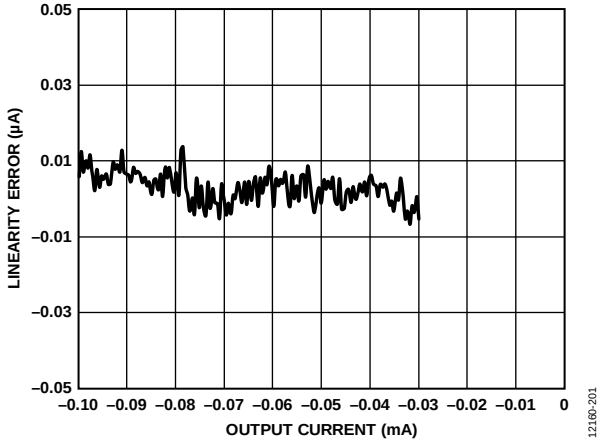


Figure 101. PPMU Current Clamp PCLx INL, Range C

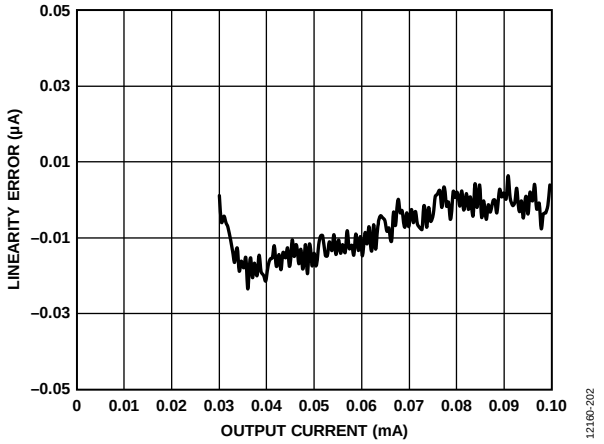


Figure 102. PPMU Current Clamp PCHx INL, Range C

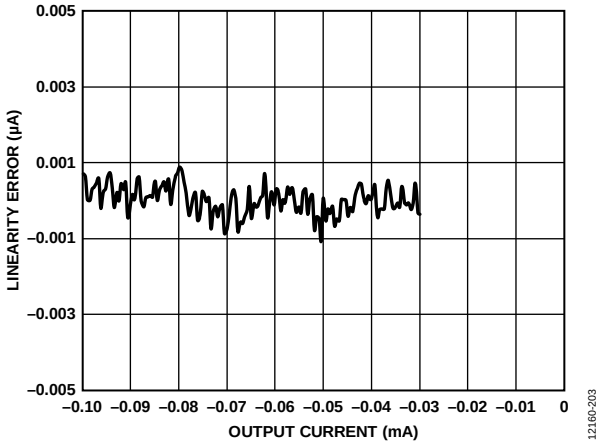


Figure 103. PPMU Current Clamp PCLx INL, Range D

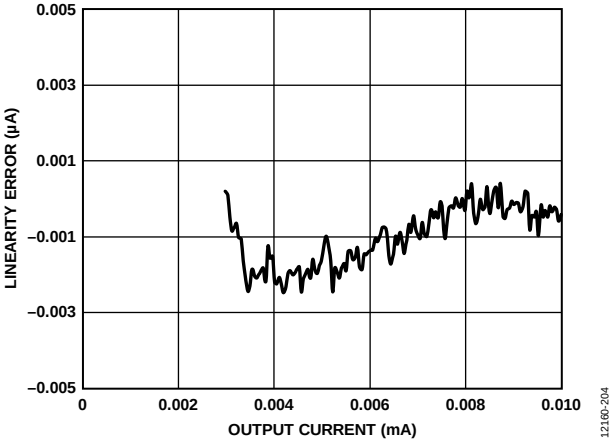


Figure 104. PPMU Current Clamp PCHx INL, Range D

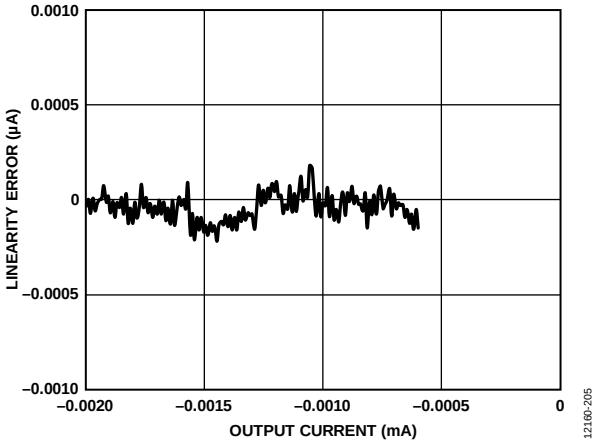


Figure 105. PPMU Current Clamp PCLx INL, Range E

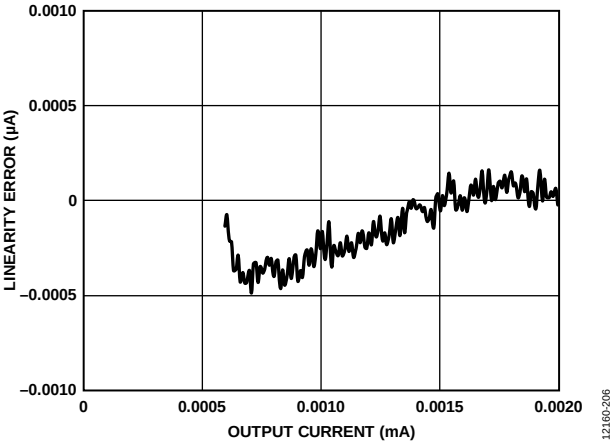


Figure 106. PPMU Current Clamp PCHx INL, Range E

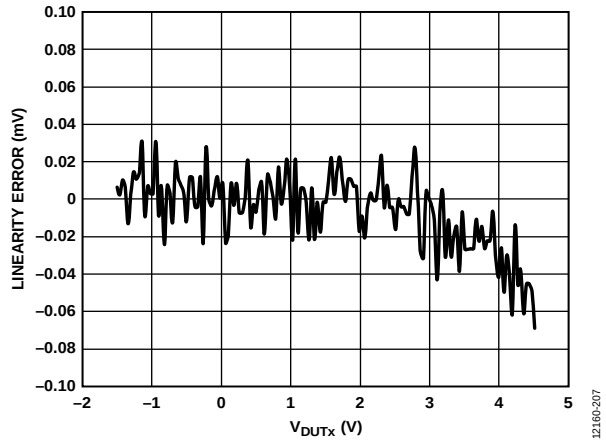


Figure 107. PPMU Measure Voltage INL, Range B

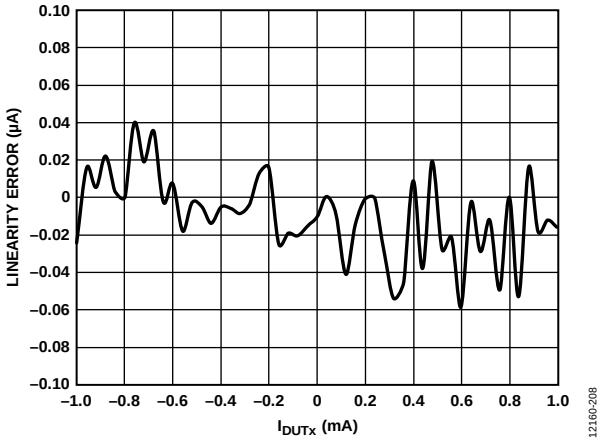


Figure 108. PPMU Measure Current INL, Range B

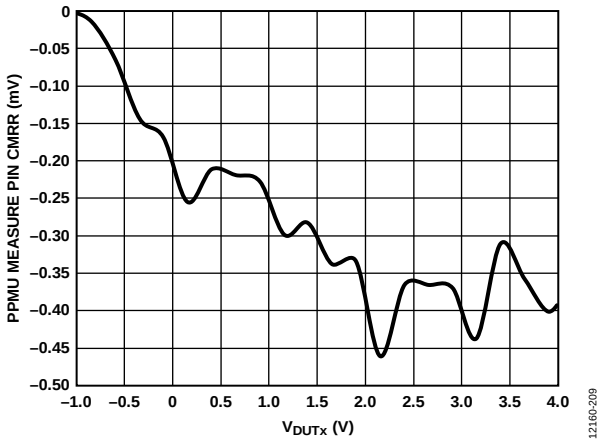


Figure 109. PPMU Measure Current Common-Mode Rejection Error, Force Voltage Measure Current (FVMI), Source 0.5 mA

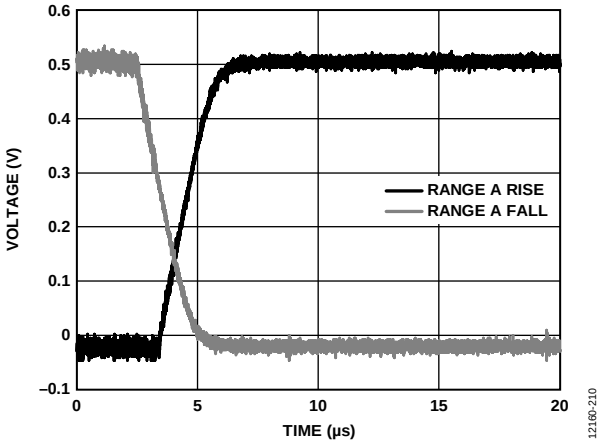


Figure 110. PPMU Force Voltage Transient Response, Range A, 0.0 V to 0.5 V, Uncalibrated, C_{LOAD} = 200 pF

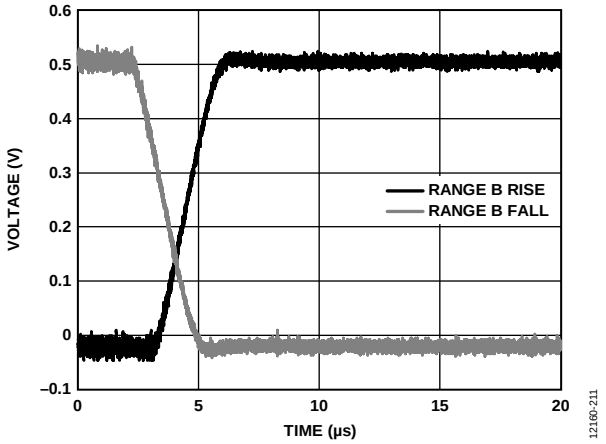


Figure 111. PPMU Force Voltage Transient Response, Range B, 0.0 V to 0.5 V, Uncalibrated, C_{LOAD} = 200 pF

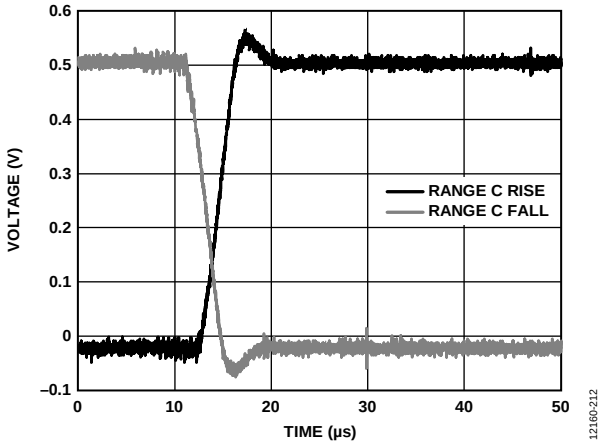


Figure 112. PPMU Force Voltage Transient Response, Range C, 0.0 V to 0.5 V, Uncalibrated, C_{LOAD} = 200 pF

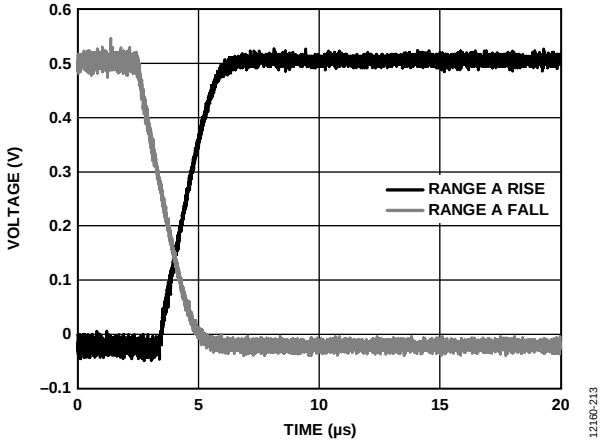


Figure 113. PPMU Force Voltage Transient Response, Range A, 0.0 V to 0.5 V, Uncalibrated, C_{LOAD} = 2000 pF

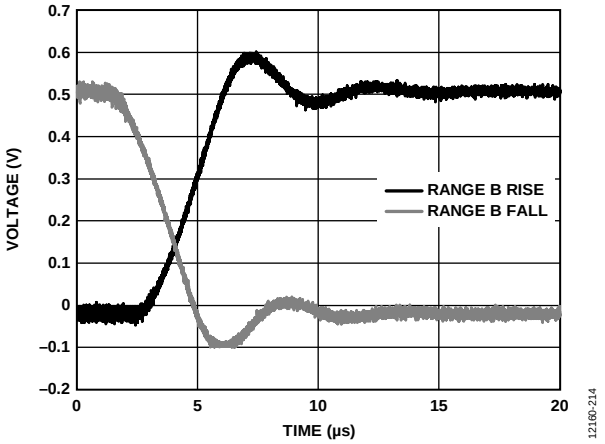


Figure 114. PPMU Force Voltage Transient Response, Range B, 0.0 V to 0.5 V, Uncalibrated, C_{LOAD} = 2000 pF

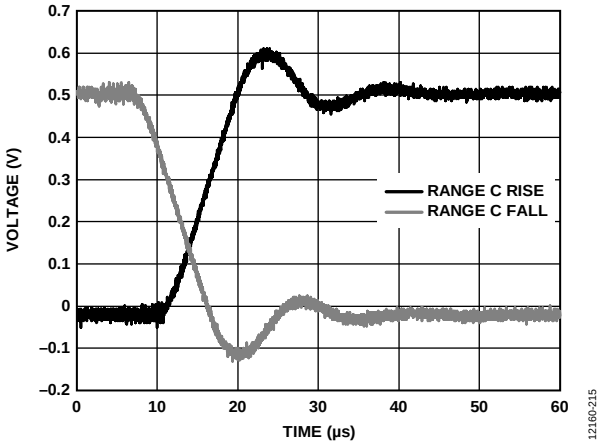


Figure 115. PPMU Force Voltage Transient Response, Range C, 0.0 V to 0.5 V, Uncalibrated, C_{LOAD} = 2000 pF

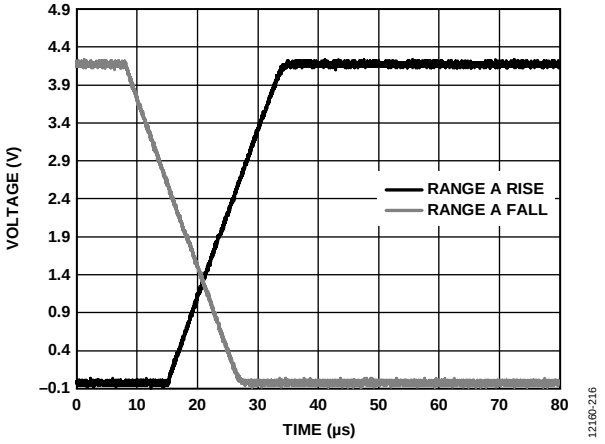


Figure 116. PPMU Force Voltage Transient Response, Range A, 0.0 V to 4.0 V, Uncalibrated, C_{LOAD} = 200 pF

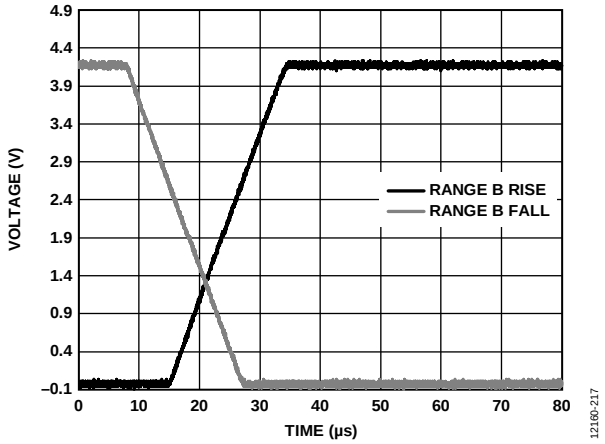


Figure 117. PPMU Force Voltage Transient Response, Range B, 0.0 V to 4.0 V, Uncalibrated, C_{LOAD} = 200 pF

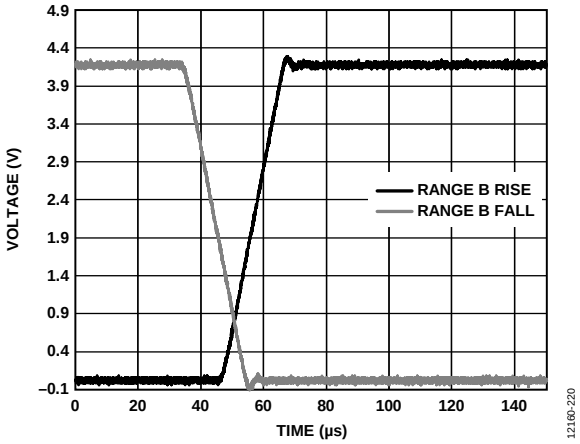


Figure 120. PPMU Force Voltage Transient Response, Range B, 0.0 V to 4.0 V, Uncalibrated, C_{LOAD} = 2000 pF

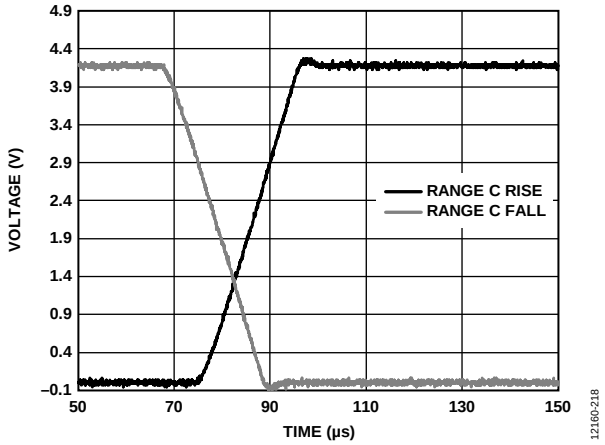


Figure 118. PPMU Force Voltage Transient Response, Range C, 0.0 V to 4.0 V, Uncalibrated, C_{LOAD} = 200 pF

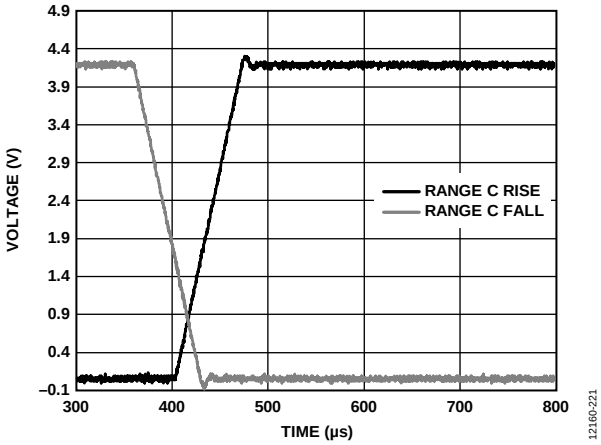


Figure 121. PPMU Force Voltage Transient Response, Range C, 0.0 V to 4.0 V, Uncalibrated, C_{LOAD} = 2000 pF

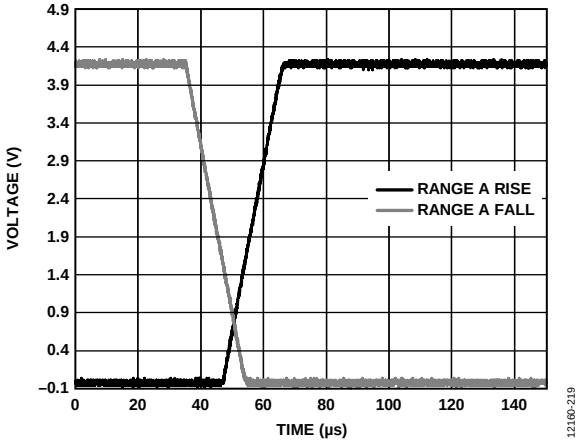


Figure 119. PPMU Force Voltage Transient Response, Range A, 0.0 V to 4.0 V, Uncalibrated, C_{LOAD} = 2000 pF

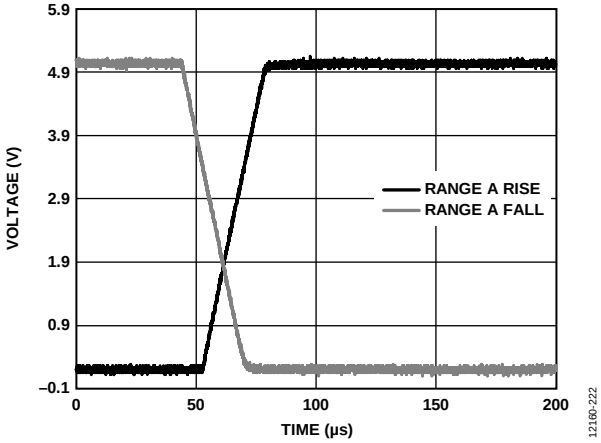


Figure 122. PPMU Force Current Transient Response, Range A, Full-Scale Transition, Uncalibrated, C_{LOAD} = 200 pF, R_{LOAD} = 127 Ω

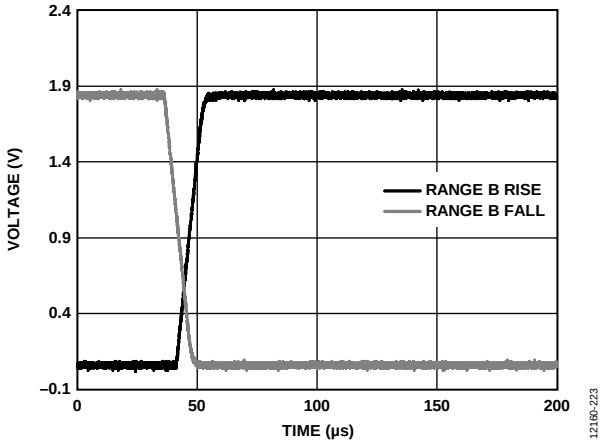


Figure 123. PPMU Force Current Transient Response, Range B, Full-Scale Transition, Uncalibrated, C_{LOAD} = 200 pF, R_{LOAD} = 1.8 kΩ

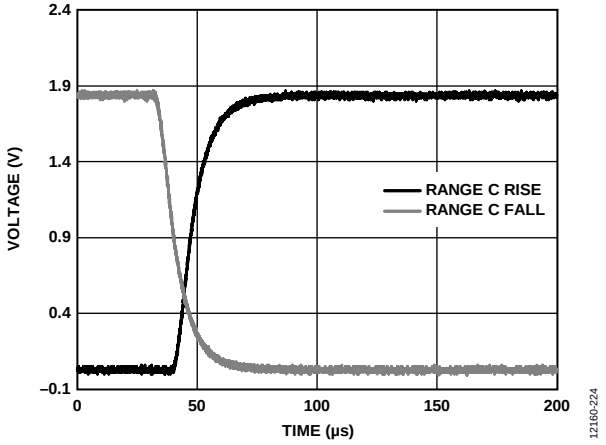


Figure 124. PPMU Force Current Transient Response, Range C, Full-Scale Transition, Uncalibrated, C_{LOAD} = 200 pF, R_{LOAD} = 18.5 kΩ

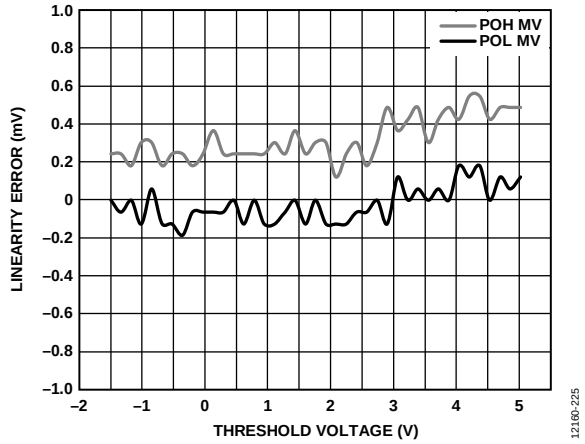


Figure 125. PPMU Go/No-Go Comparator Threshold INL

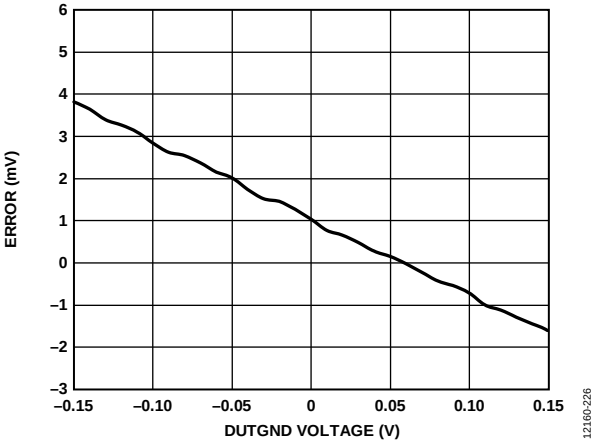


Figure 126. Typical DUTGND Transfer Function Voltage Error, Drive Low, VIL = 0.0 V

THEORY OF OPERATION

SERIAL PROGRAMMABLE INTERFACE (SPI)

SPI Hardware Interconnect Details

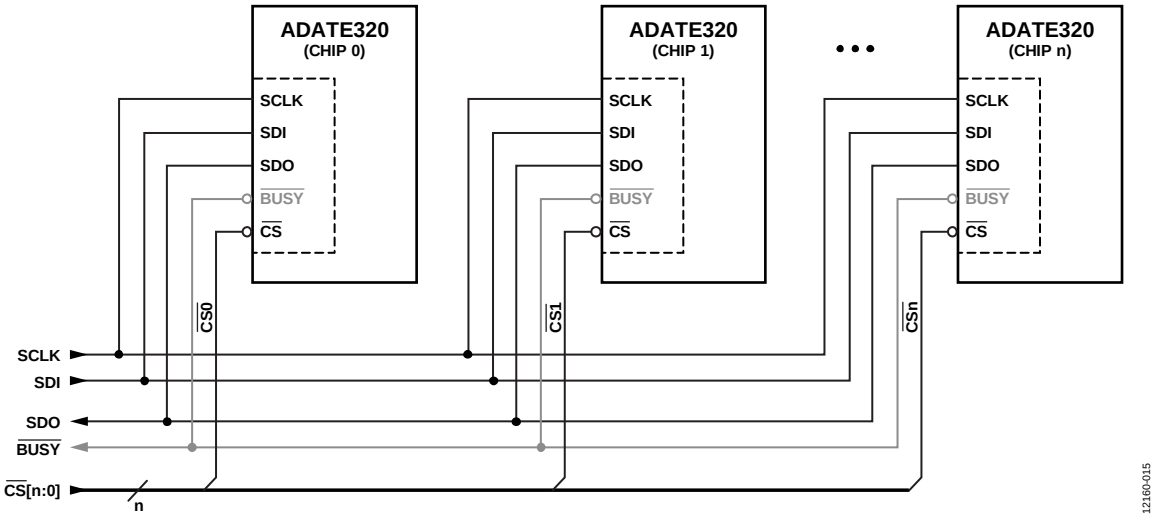


Figure 127. Multiple SPI with a Shared SDO Line

SPI Reset Sequence and the $\overline{RST}$ Pin

The internal state of the ADATE320 is indeterminate following power-up. For this reason, it is necessary to perform a valid hardware reset sequence as soon as the power supplies are stabilized. The ADATE320 provides an active low reset pin ($\overline{RST}$) for this purpose. Asserting $\overline{RST}$ asynchronously initiates a reset sequence. Furthermore, the $\overline{RST}$ pin must be asserted before and during the power-up cycling sequence, and released only after all power supplies are guaranteed to be stable.

A soft reset sequence can also be initiated under SPI software control by writing to the SPI_RESET bit (see Figure 147). In the case of a soft reset, the sequence begins on the first rising edge of SCLK following the release of $\overline{CS}$, subject to the normal setup and hold times. Certain actions occur immediately upon the initiation of the reset request, whereas other actions require several cycles of SCLK.

The following asynchronous actions occur immediately following the detection of the reset request, whether it was hardware ($\overline{RST}$) or software (SPI) initiated:

- Assert open-drain $\overline{BUSY}$ pin
- Force all control registers to their default reset states as defined in Table 29
- Clear all calibration registers to their default reset states as defined in Table 29
- Override all DAC analog outputs and force dc levels to V_{DUTGND}, disable the driver and PPMU functions
- Enable active loads with IOHx = IOLx = 100 µA (uncalibrated and expected to vary with offset from device to device); soft connect DUTx pins to VCOM = V_{DUTGND}

The device remains in this static reset state indefinitely until the clocked portion of the sequence begins with either the first rising edge of SCLK following the release of $\overline{RST}$ in the case of an asynchronous hardware reset, or the second rising edge of SCLK following the release of $\overline{CS}$ in the case of a software SPI reset. Regardless of how the reset sequence was initiated, the clocked portion of the sequence requires 744 SCLK cycles to run through to completion, and the open-drain $\overline{BUSY}$ pin (if available) remains asserted until all clock cycles are received. The following actions occur during the clocked portion of the reset sequence:

- Complete initialization of internal SPI controller
- Write default values to appropriate DAC X_2 registers
- Enable the thermal alarm with a 100°C threshold
- Disable the PPMU clamp and overvoltage detect (OVD) alarms

The 744 rising edges of SCLK release $\overline{BUSY}$ and start a self timed DAC deglitch period of approximately 3 µs. DAC voltages begin to change as soon as the deglitch circuits time out. An additional 10 µs is required to settle to the final values. A full reset sequence thus requires approximately 30 µs, comprising 16 µs (744 cycles × 20 ns) for post reset initialization, 3 µs for DAC deglitch, and another 10 µs for DAC analog level settling.

SPI Clock Cycles and the $\overline{\text{BUSY}}$ Pin

The ADATE320 offers a digital $\overline{\text{BUSY}}$ output pin to indicate that the SPI controller requires more SCLK cycles to be input on the SCLK pin. The device may be operated without this pin, but care must be exercised to ensure that the required number of SCLK cycles are provided in each case to complete each SPI instruction.

After any valid SPI instruction is written to the ADATE320, the $\overline{\text{BUSY}}$ pin is asserted to indicate a busy status of the DAC update and calibration routines. The $\overline{\text{BUSY}}$ pin is an open-drain output capable of sinking a minimum of 2 mA from the VDD supply. It is recommended to tie the $\overline{\text{BUSY}}$ pin to VDD with an external 1 kΩ pull-up resistor.

It is not a requirement to wait for release of $\overline{\text{BUSY}}$ prior to a subsequent assertion of the $\overline{\text{CS}}$ pin. As long as the minimum number of SCLK cycles following the previous release of $\overline{\text{CS}}$ is met according to the t_{CSAM} parameter, the $\overline{\text{CS}}$ pin can again be asserted for another SPI operation. With the one exception of recovery from a reset request (either by hardware assertion of $\overline{\text{RST}}$ pin or software setting of the internal SPI_RESET control bit), there is no scenario in normal operation of the ADATE320 in which the user must wait for release of $\overline{\text{BUSY}}$ before asserting the $\overline{\text{CS}}$ pin for a subsequent SPI operation. The only requirement on the assertion of $\overline{\text{CS}}$ is that the t_{CSAM} parameter has been met as defined in Figure 2 and Table 14.

It is very important, however, that the SCLK pin continue to operate for as long as the $\overline{\text{BUSY}}$ pin state remains active. This period of time is defined by the parameter t_{BUSW} and is defined in Figure 2, Table 14, and Table 23. If the SCLK pin does not remain active for at least the number of cycles specified, operations pending to the internal processor may not fully complete. In such a case, a temporary malfunction of the ADATE320 may occur, or unexpected results may be obtained. After the device releases the $\overline{\text{BUSY}}$ pin (or the required minimum number of clock cycles is satisfied), SCLK may again be stopped to prevent any unwanted digital noise from coupling into the analog functions. In every case (with no exception for reset recovery), it is the purpose of the $\overline{\text{BUSY}}$ pin to notify the supervisory ASIC or FGPA that it is again safe to stop the SCLK signal. Running SCLK for extra periods when $\overline{\text{BUSY}}$ is not active is never a problem except for the possibility of adding unwanted digital switching noise into analog functions.

The required length of the $\overline{\text{BUSY}}$ period (t_{BUSW}) is variable depending on the particular preceding SPI instruction, but it is always deterministic. It depends only on factors such as whether the previous instruction involved a write to one or more DAC addresses, and, if so, how many channels were involved and whether calibration was enabled. Table 23 details the length of the t_{BUSW} requirement in units of rising edge SCLK cycles for each possible SPI instruction scenario, including recovery from a hardware $\overline{\text{RST}}$ reset.

Because t_{BUSW} is deterministic, it is therefore possible to predict in advance the minimum number of rising edge SCLK cycles that are required to complete any given SPI instruction, which makes it possible to operate the device without a need to monitor the $\overline{\text{BUSY}}$ pin. For applications in which it is neither possible nor desirable to monitor the pin, it is acceptable to use the deterministic information provided in Table 23 to guarantee the minimum number of cycles is provided. Either way, it is necessary to honor the minimum number of required rising edge SCLK cycles, as defined by t_{BUSW}, following the release of $\overline{\text{CS}}$ for each of the SPI instruction scenarios listed.

Table 23. $\overline{\text{BUSY}}$ Minimum SCLK Cycle Requirements

SPI Instruction Type (Single- or Dual-Channel Operation)	Minimum t_{BUSW} (SCLK Cycles)
Following Release of Asynchronous $\overline{\text{RST}}$ Reset Pin (Hardware Reset)	744
Following Assertion of the SPI_RESET Control Bit (Software Reset)	744
Write to No Operation (NOP) (Address 0x00, Address 0x20, Address 0x50, Address 0x60)	3
Write to a Valid Address That Is Not a DAC (Address > 0x10)	3
Write to Any DAC Except VILx or VIHx (Address 0x01 to Address 0x0F, Except Address 0x01 and Address 0x03)	18
Write to VILx or VIHx DAC (Address 0x01 or Address 0x03)	21

SPI Read/Write Register Definition

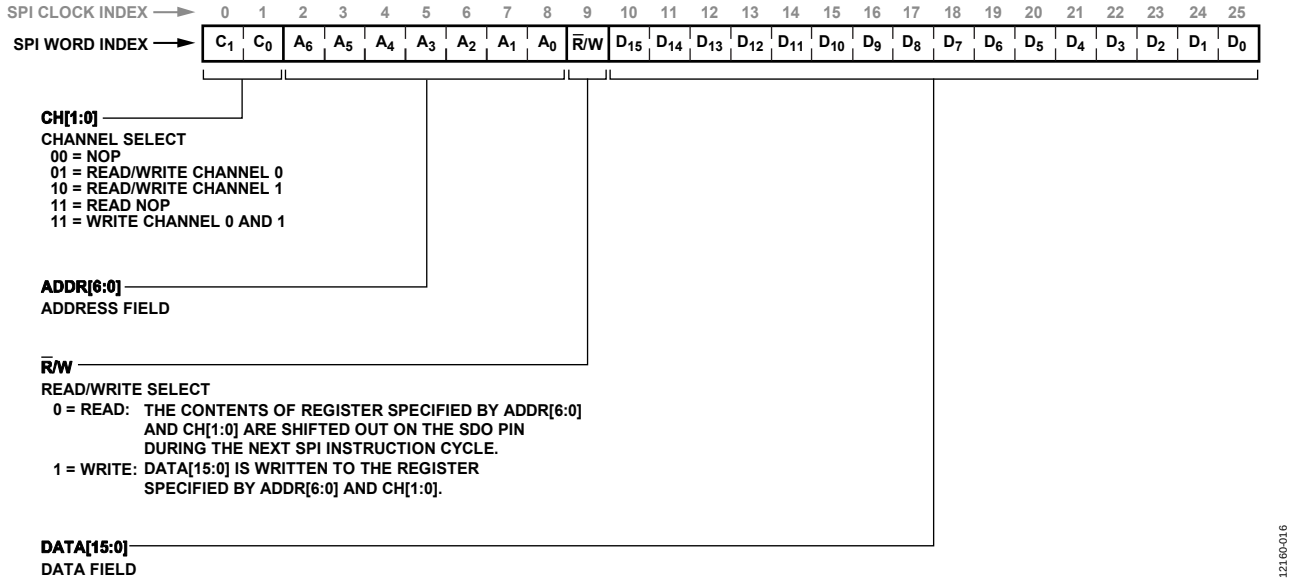


Figure 128. SPI Word Definition

The ADATE320 is configured through a collection of 16-bit registers as defined in Table 29. Mode configuration, DAC level settings, calibration constants, and alarm flags status can all be controlled and monitored by accessing the respective registers.

Specific access to any 16-bit register is made through a serial programmable interface (SPI). A single SPI control register is exposed to the user by this hardware SPI interface. The format of the SPI Control Register is illustrated in Figure 128. The SPI control register includes address and channel information, read/write direction, and a 16-bit data field. Any valid SPI write instruction cycle populates all these fields, and the ADATE320 subsequently operates on the addressed channel and register using the data provided. Any valid SPI read instruction cycle populates only the address and channel fields, and the ADATE320 makes the addressed register contents in the 16-bit data field available for subsequent readout at the SDO pin.

Detailed SPI timing diagrams for each read/write operation type are provided in Figure 2 through Figure 7. Respective dc and ac timing parameters are provided in Table 13 and Table 14, respectively.

A typical hardware wiring diagram for the SPI is illustrated in Figure 127.

LEVEL SETTING DACS

DAC Update Modes

The ADATE320 provides 32 16-bit integrated level setting DACs organized as two channel banks of 16 DACs each. The detailed mapping of each DAC register to each pin electronics function is shown in Table 29. Each DAC can be individually programmed by writing data to the respective SPI register address and channel.

The ADATE320 provides two methods for updating analog DAC levels: DAC immediate update mode and DAC deferred update mode. At the release of the $\overline{CS}$ pin associated with any valid SPI write to a DAC address, the update of the analog levels can start immediately or can be deferred, depending on the state of the DAC_LOAD_MODE control bit in the DAC control register (see Figure 146). Initiation of the analog level update sequence (and triggering of the on-chip deglitch circuit) begins four SCLK cycles following the associated release of $\overline{CS}$ pin. For the purpose of this data sheet, the analog level update sequence is assumed to start coincident with the release of $\overline{CS}$. The DAC update mode can be selected independently for each channel bank.

If the DAC_LOAD_MODE control bit for a given channel bank is cleared, the DACs assigned to that channel bank are placed in the DAC immediate update mode. Writing to any DAC within that channel causes the corresponding analog levels to be updated immediately following the associated release of $\overline{CS}$. Because all analog levels are updated on a per channel basis, any previously pending DAC writes queued to that channel (while in an earlier deferred update mode) are also updated at this time. This situation can arise if DAC writes are queued to the channel while in deferred update mode, and then the DAC_LOAD_MODE bit is subsequently changed to immediate update mode before writing to the respective DAC_LOAD control bit (see Figure 146). The queued data is not lost. Note that writing to the DAC_LOAD control bit has no effect while in immediate update mode.

If the DAC_LOAD_MODE control bit for a given channel is set, then the DACs assigned to that channel bank is in the deferred update mode. Writing to any DAC of that channel only queues the DAC data into that channel. The analog update of queued DAC levels is deferred until the respective DAC_LOAD control bit is set (see Figure 146). The DAC deferred update mode, in conjunction with the respective DAC_LOAD control bit, provides the means to queue all DAC level writes to a given channel bank before synchronously updating the analog levels with a single SPI command.

The OVDH and OVDL DAC levels do not fit neatly within a particular channel bank. However, they must be updated as a part of the channel bank to which they are assigned, as shown in Table 29.

The ADATE320 provides a feature in which a single SPI write operation can address two channels at one time. With this feature, a single SPI write operation can address corresponding DACs on both channels at the same time, even though the channels may be configured with different DAC update modes. In such a case, the device behaves as expected. For example, if both channels are in immediate update mode, the update of analog levels of both channel banks begins following the associated release of the $\overline{CS}$ pin. If both channels are in deferred update mode, the update of analog levels is deferred for both channels until the corresponding DAC_LOAD control bit is set. If one channel is in deferred update mode and the other is in immediate update mode, the deferred channel defers analog updates until the corresponding DAC_LOAD bit is written, and the immediate channel begins analog updates immediately following release of the $\overline{CS}$ pin.

An on-chip deglitch circuit with a period of approximately 3 µs is provided to prevent DAC-to-DAC crosstalk within a channel whenever an analog update is processed. Each DAC channel bank has its own dedicated deglitch circuitry, and each channel may therefore operate independently.

A deglitch circuit can be retriggered if an analog level update is initiated before a previous update operation on that channel completes. Analog transitions at the DAC outputs do not begin until after the deglitch circuit times out. Final settling to full precision requires an additional 7 µs beyond the end of the 3 µs deglitch interval. The total DAC settling time following the release of the associated $\overline{CS}$ pin is approximately 10 µs maximum. Note that an extended retriggering sequence of the deglitch circuit on one channel may cause the apparent settling time of analog levels on that channel to appear delayed longer than the specified 10 µs.

A typical DAC update sequence is illustrated in Figure 129. In this example, consecutive immediate mode DAC updates are written in direct succession. This example was chosen to illustrate what happens when a DAC update command is written before the previous update command finishes its deglitch and settling sequence.

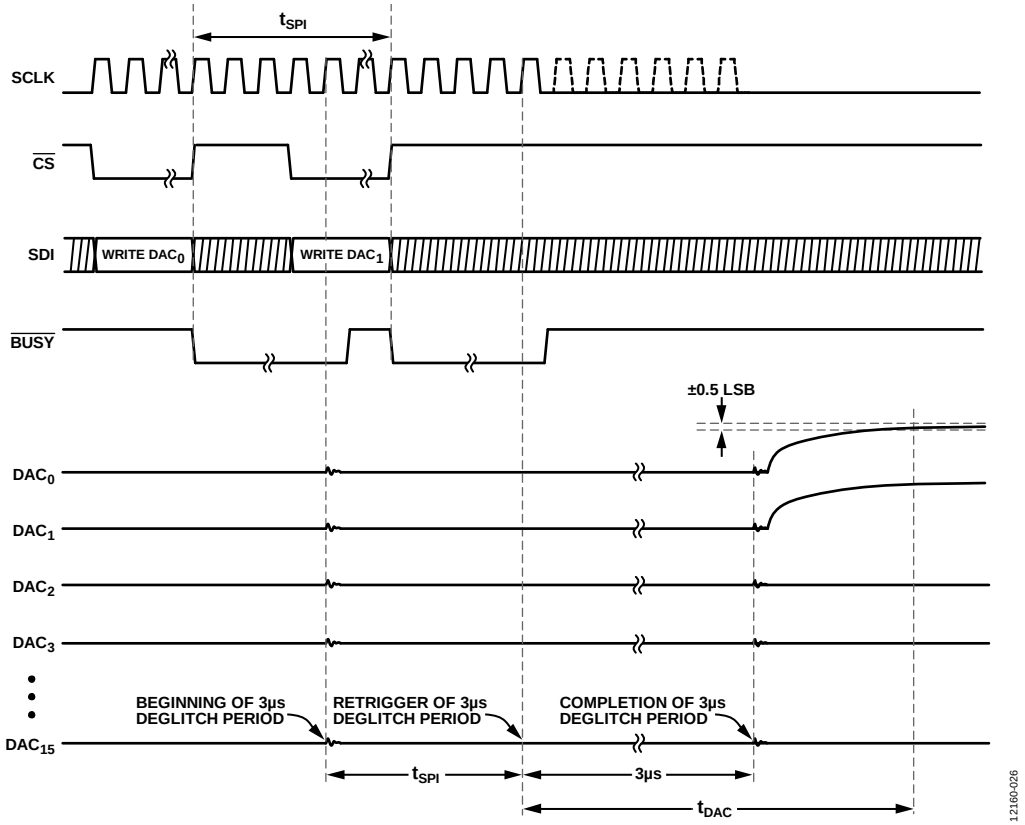


Figure 129. SPI DAC Write Timing Diagram and Settling of DC Levels

DAC Levels and VTHERM Pin Transfer Function

Table 24. Detailed DAC Code to/from Voltage Level Transfer Functions

Level	Programmable Range (0x0000 to 0xFFFF)	DAC-to-Level and Level-to-DAC Transfer Functions
VILx, VIHx, VITx/VCOMx, VOLx, VOHx, POLx, POHx, VCHx, VCLx, PCHx, PCLx, OVDHx, OVDLx, PPMUx (FV), PCHx (FI), PCLx (FI)	−2.5 V to +7.5 V	$V_{DUTx} = (4 \times (DAC/2^{16}) - 1) \times (V_{REF} - V_{REFGND}) + V_{DUTGND}$ $DAC = ((V_{DUTx} - V_{DUTGND}) + (V_{REF} - V_{REFGND}))/(4 \times (V_{REF} - V_{REFGND})) \times 2^{16}$
IOHx, IOLx	−12.5 mA to +37.5 mA	$I_{DUTx} = (4 \times (DAC/2^{16}) - 1) \times (V_{REF} - V_{REFGND}) \times (25\ mA/5)$ $DAC = ((I_{DUTx} \times (5/25\ mA)) + (V_{REF} - V_{REFGND}))/(4 \times (V_{REF} - V_{REFGND})) \times 2^{16}$
PPMUx (FI, Range A), PCHx and PCLx (FV, Range A)	−80 mA to +80 mA	$I_{DUTx} = (4 \times (DAC/2^{16}) - 2) \times (V_{REF} - V_{REFGND}) \times (80\ mA/5)$ $DAC = ((I_{DUTx}/80\ mA \times 5) + 2 \times (V_{REF} - V_{REFGND}))/(4 \times (V_{REF} - V_{REFGND})) \times 2^{16}$
PPMUx (FI, Range B), PCHx and PCLx (FV, Range B)	−2 mA to +2 mA	$I_{DUTx} = (4 \times (DAC/2^{16}) - 2) \times (V_{REF} - V_{REFGND}) \times (2\ mA/5)$ $DAC = ((I_{DUTx}/2\ mA \times 5) + 2 \times (V_{REF} - V_{REFGND}))/(4 \times (V_{REF} - V_{REFGND})) \times 2^{16}$
PPMUx (FI, Range C), PCHx and PCLx (FV, Range C)	−200 µA to +200 µA	$I_{DUTx} = (4 \times (DAC/2^{16}) - 2) \times (V_{REF} - V_{REFGND}) \times (200\ \mu A/5)$ $DAC = ((I_{DUTx}/200\ \mu A \times 5) + 2 \times (V_{REF} - V_{REFGND}))/(4 \times (V_{REF} - V_{REFGND})) \times 2^{16}$
PPMUx (FI, Range D) PCHx and PCLx (FV, Range D)	−20 µA to +20 µA	$I_{DUTx} = (4 \times (DAC/2^{16}) - 2) \times (V_{REF} - V_{REFGND}) \times (20\ \mu A/5)$ $DAC = ((I_{DUTx}/20\ \mu A \times 5) + 2 \times (V_{REF} - V_{REFGND}))/(4 \times (V_{REF} - V_{REFGND})) \times 2^{16}$
PPMUx (FI, Range E) PCHx and PCLx (FV, Range E)	−4 µA to +4 µA	$I_{DUTx} = (4 \times (DAC/2^{16}) - 2) \times (V_{REF} - V_{REFGND}) \times (4\ \mu A/5)$ $DAC = ((I_{DUTx}/4\ \mu A \times 5) + 2 \times (V_{REF} - V_{REFGND}))/(4 \times (V_{REF} - V_{REFGND})) \times 2^{16}$

Table 25. Load Transfer Functions

Load Level	Transfer Functions	Notes
IOLx	$VIOLx/(2 \times (V_{REF} - V_{REFGND})) \times 25\ mA$	VIOLx DAC levels are not referenced to V_{DUTGND}
IOHx	$VIOHx/(2 \times (V_{REF} - V_{REFGND})) \times 25\ mA$	VIOHx DAC levels are not referenced to V_{DUTGND}

Table 26. PPMU Transfer Functions

PPMU Mode	Transfer Functions[1]	Uncalibrated PPMU DAC Settings to Achieve Specified PPMU Range
FV	$V_{DUTx} = PPMUx$	−1.5 V < PPMUx < +4.5 V
FI	$I_{DUTx} = (PPMUx - (V_{REF} - V_{REFGND}))/(5 \times R_{PPMU})$	0.0 V < PPMUx < 5.0 V
MV	$VPPMU\_Mx = V_{DUTx}$ (internal sense path)	Not applicable
MV	$VPPMU\_Mx = V_{PPMU\_Sx}$ (external sense path)	Not applicable
MI	$VPPMU\_Mx = (V_{REF} - V_{REFGND}) + (5 \times I_{DUTx} \times R_{PPMU}) + V_{DUTGND}$	Not applicable

[1] R_{PPMU} = 12.5 Ω for Range A, 500 Ω for Range B, 5.0 kΩ for Range C, 50 kΩ for Range D, and 250 kΩ for Range E.

Table 27. Temperature Sensor Transfer Function

Temperature	Output
0 K	0.00 V
300 K	3.00 V
T_{KELVIN}	$0.00\ V + (T_{KELVIN}) \times 10\ mV/K$

DAC Gain and Offset Correction

Each analog function within the ADATE320 has independent gain (m) and offset (c) calibration registers that allow digital trim of first-order errors in the analog signal chain. These registers correct errors in the pin electronics transfer functions as well as errors intrinsic to the DAC itself.

The m and c registers are volatile and must be reloaded after each power-on cycle as part of a calibration routine if values other than the defaults are required. The registers are not cleared by any reset operation (although the DAC_CAL_ENABLE bit is cleared following reset).

The gain and offset calibration function can be bypassed by clearing the DAC_CAL_ENABLE bit in the DAC control register (see Figure 146). This bypass mode is available only on a per chip basis. In other words, it is not possible to bypass the calibration function for a specific subset of the DACs.

The calibration function, when enabled, adjusts the numerical data sent to each DAC according to the following equation:

$$X_2 = \left(\left(\frac{m+1}{2^{16}}\right) \times X_1\right) + \left(c - 2^{15}\right) \quad (1)$$

where:
X_2 is the 16-bit data-word gated into the physical DAC, and returned by subsequent SPI read from that same DAC.
m is the code in the respective DAC gain calibration register (the default code is 0xFFFF = $2^{16} - 1$).
X_1 is the 16-bit data-word written by the user to the DAC via the SPI.
c is the code in the respective DAC offset calibration register (the default code is 0x8000 = 2^{15}).

From Equation 1, it can be seen that the gain applied to any written X_1 data is always ≤1.0, with the effect that the effective output of a DAC can only be made smaller in magnitude by the calibration mechanism. To compensate for this imposed limitation, each of the analog signal paths in the pin electronics functions are guaranteed by designed to have a gain ≥1.0 when the default m register values are applied. A signal path gain ≥1.0 guarantees that proper gain calibration can always be achieved by multiplying down.

DAC X_2 Registers and SPI Readback

When data is written via the SPI to a particular DAC, that data is operated on in accordance with Equation 1. The results are stored in an X_2 register associated with that DAC (see Figure 130).

There is only a single physical X_2 register per DAC, and it is the value of this X_2 register that is eventually gated into the physical DAC at the time of analog update, which can be either in immediate or deferred mode. It is also this register value that is returned to the user during an SPI read operation addressed to that DAC channel. In the special case of a dual channel write to a DAC, both of the associated X_2 registers are sequentially updated using the appropriate m register and c register for each channel.

When enabled, the calibration function applies this operation to the X_2 registers only after a SPI write to the respective X_1 registers. The X_2 registers are not updated after write operations to either m register or c register or following any changes to functional modes or range settings of the device. For this reason, to ensure that calibration data is recalculated for any particular DAC, it is necessary to write fresh data to that DAC after changes are first made to the associated m register and c register, and any associated functional modes and ranges for that DAC function.

For each DAC, there is only a single X_2 register, and generally there is one dedicated and unique set of m calibration register and c calibration register assigned. In several special cases (for example, the PPMU DAC) there is still only one X_2 register per DAC, but there are several different choices for m register and c register depending on the particular configuration of mode and range control settings for the function. For those DACs, a choice of calibration register is made automatically based on the respective mode and range control settings in place for that function when the DAC is written.

Table 28 describes detailed m register and c register selection as a function of mode and range control settings. For all DAC functions, it is necessary to ensure that the respective m register and c register values are put in place first, and that the desired mode and range settings are updated prior to sending data to the DAC. It is only during the DAC write sequence that the calibration constants are selected and applied.

Table 28. m and c Calibration Register Selection[1]

SPI Address [Channel]	DAC Name	Functional (DAC Usage) Description	m Register	c Register	DMC_ ENABLE (Address 0x1A[0])	LOAD_ ENABLE_x (Address 0x1B[0])	PPMU_ MEAS_VI_x (Address 0x1C[6])	PPMU_ FORCE_VI_x (Address 0x1C[5])	PPMU_ RANGE_x (Address 0x1C[4:2])
0x01[0]	VIH0	Driver high level, Channel 0	0x21[0]	0x31[0]	X	X	X	X	XXX
0x01[1]	VIH1	Driver high level, Channel 1	0x21[1]	0x31[1]	X	X	X	X	XXX
0x02[0]	VIT0/ VCOM0	Driver term level, Channel 0	0x22[0]	0x32[0]	X	0	X	X	XXX
		Load commutation voltage, Channel 0	0x42[0]	0x52[0]	X	1	X	X	XXX
0x02[1]	VIT1/ VCOM0	Driver termination level, Channel 1	0x22[1]	0x32[1]	X	0	X	X	XXX
		Load commutation voltage, Channel 1	0x42[1]	0x52[1]	X	1	X	X	XXX
0x03[0]	VIL0	Driver low level, Channel 0	0x23[0]	0x33[0]	X	X	X	X	XXX
0x03[1]	VIL1	Driver low level, Channel 1	0x23[1]	0x33[1]	X	X	X	X	XXX
0x04[0]	VCH0	Reflection clamp high level, Channel 0	0x24[0]	0x34[0]	X	X	X	X	XXX
0x04[1]	VCH1	Reflection clamp high level, Channel 1	0x24[1]	0x34[1]	X	X	X	X	XXX
0x05[0]	VCL0	Reflection clamp low level, Channel 0	0x25[0]	0x35[0]	X	X	X	X	XXX
0x05[1]	VCL1	Reflection clamp low level, Channel 1	0x25[1]	0x35[1]	X	X	X	X	XXX
0x06[0]	VOH0	Normal window comparator high level, Channel 0	0x26[0]	0x36[0]	0	X	X	X	XXX
		Differential mode comparator high level, Channel 0	0x46[0]	0x56[0]	1	X	X	X	XXX
0x06[1]	VOH1	Normal window comparator high level, Channel 1	0x26[1]	0x36[1]	X	X	X	X	XXX
0x07[0]	VOL0	Normal window comparator low level, Channel 0	0x27[0]	0x37[0]	0	X	X	X	XXX
		Differential mode comparator low level, Channel 0	0x47[0]	0x57[0]	1	X	X	X	XXX
0x07[1]	VOL1	Normal window comparator low level, Channel 1	0x27[1]	0x37[1]	X	X	X	X	XXX
0x08[0]	VIOH0	Load IOHx level, Channel 0	0x28[0]	0x38[0]	X	X	X	X	XXX
0x08[1]	VIOH1	Load IOHx level, Channel 1	0x28[1]	0x38[1]	X	X	X	X	XXX
0x09[0]	VIOL0	Load IOL level, Channel 0	0x29[0]	0x39[0]	X	X	X	X	XXX
0x09[1]	VIOL1	Load IOL level, Channel 1	0x29[1]	0x39[1]	X	X	X	X	XXX
0x0A[0]	PPMU0	PPMU VIN FV level, Channel 0	0x2A[0]	0x3A[0]	X	X	X	0	XXX
		PPMU VIN FI level Range A, Channel 0	0x4A[0]	0x5A[0]	X	X	X	1	111
		PPMU VIN FI level Range B, Channel 0	0x4B[0]	0x5A[0]	X	X	X	1	110
		PPMU VIN FI level Range C, Channel 0	0x4C[0]	0x5A[0]	X	X	X	1	101
		PPMU VIN FI level Range D, Channel 0	0x4D[0]	0x5A[0]	X	X	X	1	100
		PPMU VIN FI level Range E, Channel 0	0x4E[0]	0x5A[0]	X	X	X	1	0XX
0x0A[1]	PPMU1	PPMU VIN FV level, Channel 1	0x2A[1]	0x3A[1]	X	X	X	0	XXX
		PPMU VIN FI level Range A, Channel 1	0x4A[1]	0x5A[1]	X	X	X	1	111
		PPMU VIN FI level Range B, Channel 1	0x4B[1]	0x5A[1]	X	X	X	1	110
		PPMU VIN FI level Range C, Channel 1	0x4C[1]	0x5A[1]	X	X	X	1	101
		PPMU VIN FI level Range D, Channel 1	0x4D[1]	0x5A[1]	X	X	X	1	100
		PPMU VIN FI level Range E, Channel 1	0x4E[1]	0x5A[1]	X	X	X	1	0XX

SPI Address [Channel]	DAC Name	Functional (DAC Usage) Description	m Register	c Register	DMC_ ENABLE (Address 0x1A[0])	LOAD_ ENABLE_x (Address 0x1B[0])	PPMU_ MEAS_VI_x (Address 0x1C[6])	PPMU_ FORCE_VI_x (Address 0x1C[5])	PPMU_ RANGE_x (Address 0x1C[4:2])
0x0B[0]	PCH0	PPMU current clamp (FV) high level, Channel 0	0x44[0]	0x54[0]	X	X	X	0	XXX
		PPMU voltage clamp (FI) high level, Channel 0	0x2B[0]	0x3B[0]				1	
0x0B[1]	PCH1	PPMU current clamp (FV) high level, Channel 1	0x44[1]	0x54[1]	X	X	X	0	XXX
		PPMU voltage clamp (FI) high level, Channel 1	0x2B[1]	0x3B[1]				1	
0x0C[0]	PCL0	PPMU current clamp (FV) low level, Channel 0	0x45[0]	0x55[0]	X	X	X	0	XXX
		PPMU voltage clamp (FI) low level, Channel 0	0x2C[0]	0x3C[0]				1	
0x0C[1]	PCL1	PPMU current clamp (FV) low level, Channel 1	0x45[1]	0x55[1]	X	X	X	0	XXX
		PPMU voltage clamp (FI) low level, Channel 1	0x2C[1]	0x3C[1]	X	X	X	1	
0x0D[0]	POH0	PPMU go/no-go MV high level, Channel 0	0x2D[0]	0x3D[0]	X	X	0	X	XXX
		PPMU go/no-go MI Range A high level, Channel 0	0x61[0]	0x5D[0]	X	X	1	X	111
		PPMU go/no-go MI Range B high level, Channel 0	0x62[0]	0x5D[0]	X	X	1	X	110
		PPMU go/no-go MI Range C high level, Channel 0	0x63[0]	0x5D[0]	X	X	1	X	101
		PPMU go/no-go MI Range D high level, Channel 0	0x64[0]	0x5D[0]	X	X	1	X	100
		PPMU go/no-go MI Range E high level, Channel 0	0x65[0]	0x5D[0]	X	X	1	X	0XX
0x0D[1]	POH1	PPMU go/no-go MV high level, Channel 1	0x2D[1]	0x3D[1]	X	X	0	X	XXX
		PPMU go/no-go MI Range A high level, Channel 1	0x61[1]	0x5D[1]	X	X	1	X	111
		PPMU go/no-go MI Range B high level, Channel 1	0x62[1]	0x5D[1]	X	X	1	X	110
		PPMU go/no-go MI Range C high level, Channel 1	0x63[1]	0x5D[1]	X	X	1	X	101
		PPMU go/no-go MI Range D high level, Channel 1	0x641[]	0x5D[1]	X	X	1	X	100
		PPMU go/no-go MI Range E high level, Channel 1	0x65[1]	0x5D[1	X	X	1	X	0XX
0x0E[0]	POL0	PPMU go/no-go MV low level, Channel 0	0x2E[0]	0x3E[0]	X	X	0	X	XXX
		PPMU go/no-go MI Range A low level, Channel 0	0x66[0]	0x5E[0]	X	X	1	X	111
		PPMU go/no-go MI Range B low level, Channel 0	0x67[0]	0x5E[0]	X	X	1	X	110
		PPMU go/no-go MI Range C low level, Channel 0	0x68[0]	0x5E[0]	X	X	1	X	101
		PPMU go/no-go MI Range D low level, Channel 0	0x69[0]	0x5E[0]	X	X	1	X	100
		PPMU go/no-go MI Range E low level, Channel 0	0x6A[0]	0x5E[0]	X	X	1	X	0XX

SPI Address [Channel]	DAC Name	Functional (DAC Usage) Description	m Register	c Register	DMC_ ENABLE (Address 0x1A[0])	LOAD_ ENABLE_x (Address 0x1B[0])	PPMU_ MEAS_VI_x (Address 0x1C[6])	PPMU_ FORCE_VI_x (Address 0x1C[5])	PPMU_ RANGE_x (Address 0x1C[4:2])
0x0E[1]	POL1	PPMU go/no-go MV low level, Channel 1	0x2E[1]	0x3E[1]	X	X	0	X	XXX
		PPMU go/no-go MI Range A low level, Channel 1	0x66[1]	0x5E[1]	X	X	1	X	111
		PPMU go/no-go MI Range B low level, Channel 1	0x67[1]	0x5E[1]	X	X	1	X	110
		PPMU go/no-go MI Range C low level, Channel 1	0x68[1]	0x5E[1]	X	X	1	X	101
		PPMU go/no-go MI Range D low level, Channel 1	0x69[1]	0x5E[1]	X	X	1	X	100
		PPMU go/no-go MI Range E low level, Channel 1	0x6A[1]	0x5E[1]	X	X	1	X	0XX
0x0F[0]	OVDL	Overvoltage detect low level	0x2F[0]	0x3F[0]	X	X	X	X	XXX
0x0F[1]	OVDH	Overvoltage detect high level	0x2F[1]	0x3F[1]	X	X	X	X	XXX

[1] X means don't care.

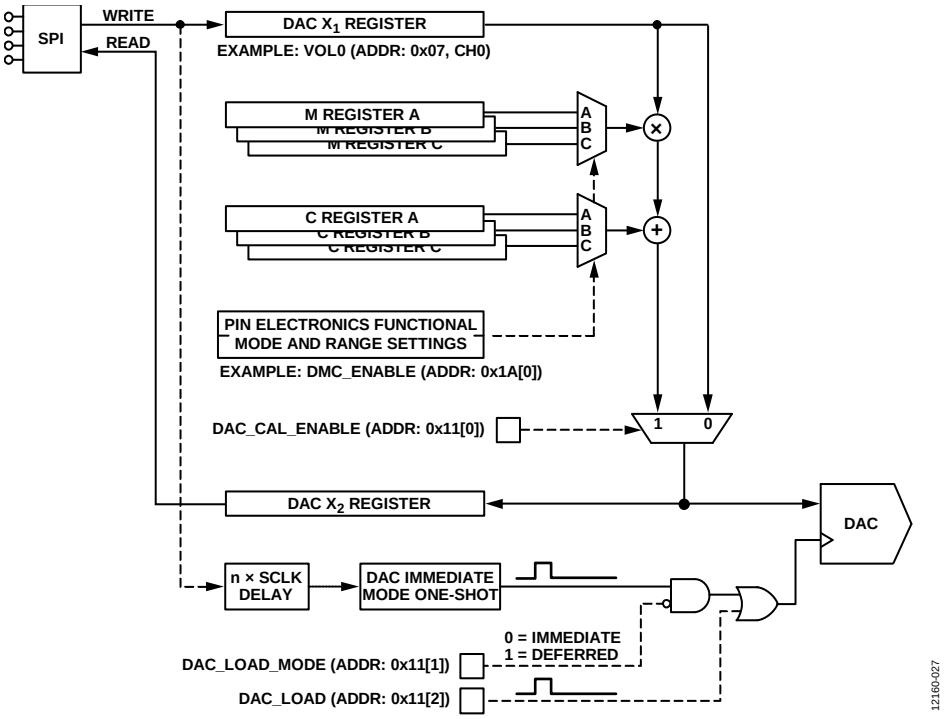


Figure 130. DAC X_2 Registers and Calibration Diagram

ALARM FUNCTIONS

The ADATE320 contains per channel overvoltage detectors (OVDL/OVDH), per channel PPMU voltage/current clamps (PCLx/PCHx), and a thermal alarm to detect and signal these respective fault conditions. Any of these functions may flag an alarm independently in the alarm state register (see Figure 153). The status of the alarms may be determined at any time by reading the SPI alarm state register. This register is read only, and its contents are cleared by the read operation. The alarm flag bits can then become set by any of the respective alarm functions. The individual fault condition flags are logically OR'ed together to drive the open-drain $\overline{\text{ALARM}}$ output pin to indicate that a fault condition has occurred (see Figure 134).

The various alarm flags can be either enabled or disabled (masked) using the alarm mask register (see Figure 152). The thermal alarm is enabled by default (mask bit clear), and the overvoltage and PPMU clamp alarms are all disabled by default (mask bits set).

The PPMU clamp alarm behavior depends on the mode of the PPMU. When in FI mode, the PPMU clamps behave as programmable voltage clamps. The high and low voltage clamp levels are set by the respective PCHx and PCLx level setting DACs. If the voltage on the DUTx pin reaches either the PCHx or PCLx setting, a PPMU clamp alarm is generated, but only if the clamps are enabled with the PPMU_CLAMP_ENABLE_x control bit in the PPMU control register (see Figure 151). Note that if the PPMU clamps are enabled and a PPMU clamp alarm is generated, the alarm can still be masked with the alarm mask register. However, if the voltage clamps are disabled, no PPMU clamp alarm is generated.

When the PPMU is in FV mode, the PPMU clamps behave as programmable current clamps. The source and sink current clamp levels are set with the respective PCHx and PCLx level setting DACs. The current clamps cannot be disabled by setting or clearing the PPMU_CLAMP_ENABLE_x control bit—the clamps are always active when in PPMU FV mode. If the PCHx and PCLx levels are set outside their functional range, a ±140% static current limit is left in effect. If the current on a DUTx pin reaches either the PCHx or PCLx clamp setting, or, alternatively, one of the static current limits, a PPMU clamp alarm results. The PPMU clamp alarm can be masked separately in the alarm mask register.

Refer to Figure 131 through Figure 134 for more information about PPMU clamp functions.

The only purpose of the various alarm circuits is to detect and indicate the presence of a fault condition of interest to the user. The only action the ADATE320 takes upon detection of a fault is to set the appropriate alarm state register flag bits in the alarm state register and then activate the open-drain $\overline{\text{ALARM}}$ pin. No other action is taken.

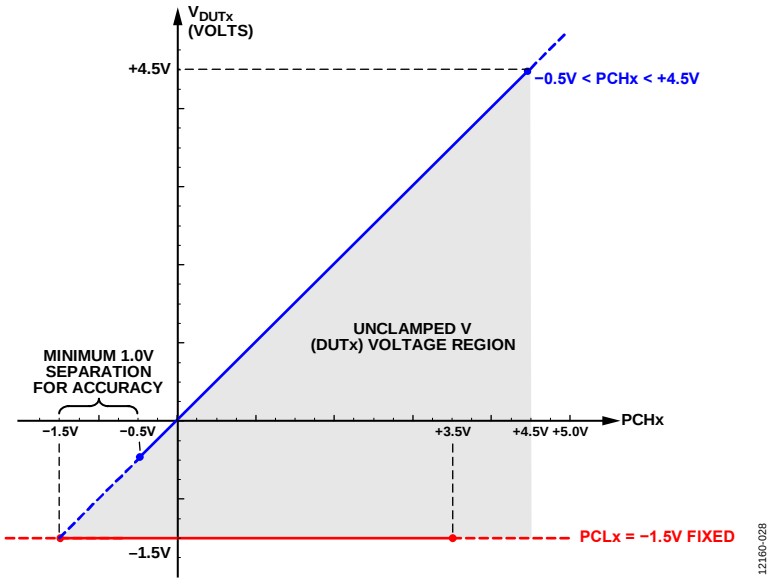


Figure 131. PPMU Voltage Clamp High, Functional Diagram (Voltage Clamp Low Fixed at −1.5 V)

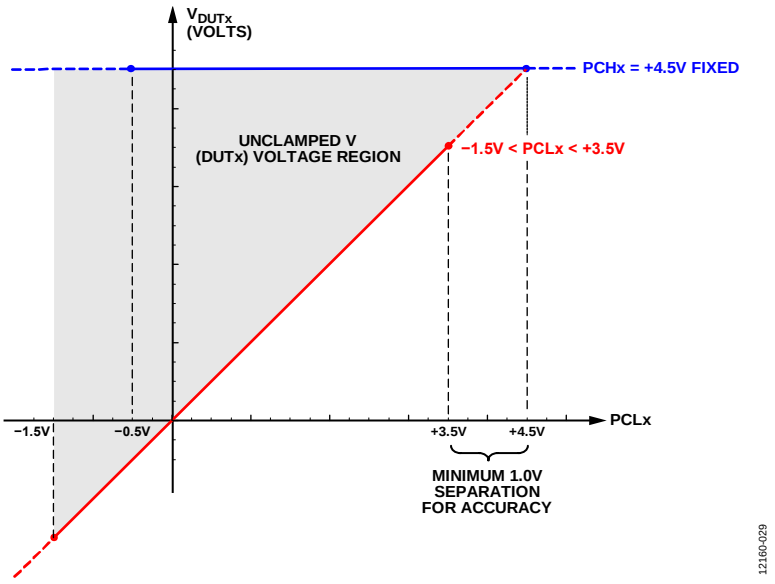


Figure 132. PPMU Voltage Clamp Low, Functional Diagram (Voltage Clamp High Fixed at 4.5 V)

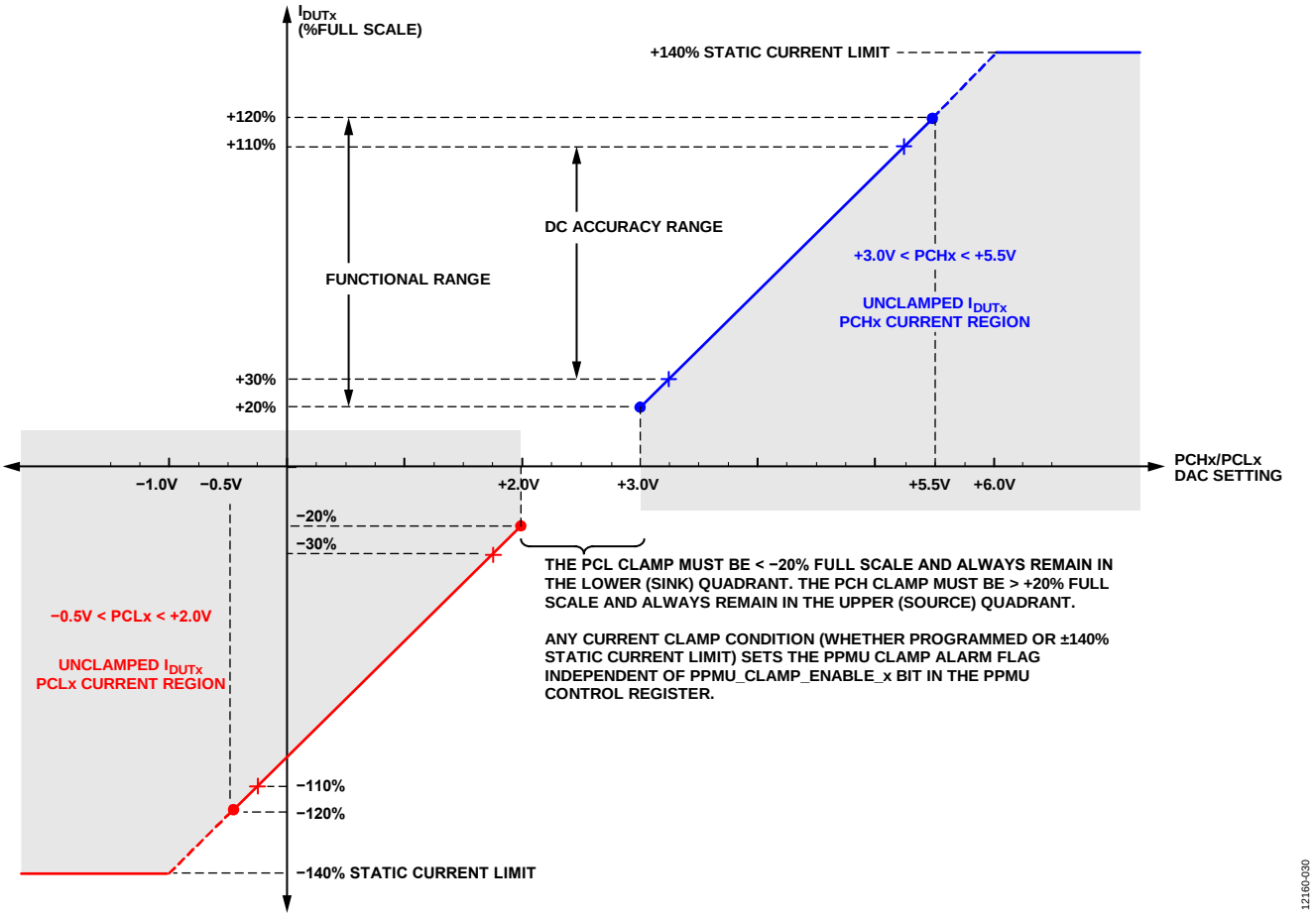


Figure 133. PPMU Current Clamp High and Low, Functional Diagram

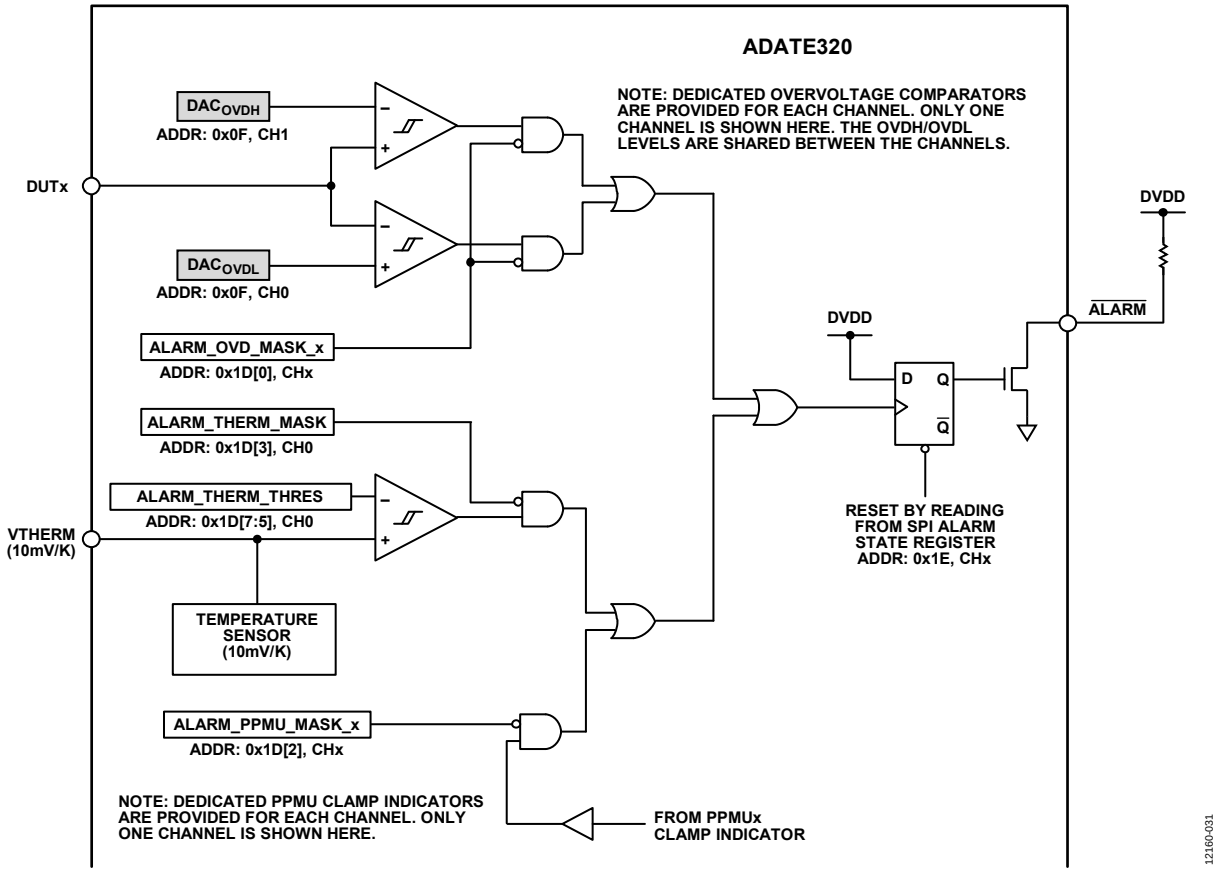


Figure 134. Fault Alarm Functional Block Diagram

APPLICATIONS INFORMATION

POWER SUPPLY, GROUNDING, AND TYPICAL DECOUPLING STRATEGY

The ADATE320 is internally divided into a digital core and an analog core.

The VDD and DGND pins provide power and ground for the digital core that includes the SPI, certain logic functions, and the digital calibration functions. DGND is the logic ground reference for the VDD supply. Therefore, bypass VDD adequately to DGND with good quality, low effective series resistance (ESR) bypass capacitors. To reduce transient digital switching noise coupling to the analog core, connect DGND to a dedicated external ground plane that is separated from the analog ground domains. If the application permits, the DGND pins can share a digital ground domain with the supervisory FPGA or ASIC that interfaces with the ADATE320 SPI. All CMOS inputs and outputs are referenced between VDD and DGND, and their valid levels must be guaranteed relative to these power supply pins.

The analog core of the device includes all analog ATE functional blocks such as the DACs, the driver, the comparator, the load, and the PPMU. The VCC and VEE supplies provide power to the analog core. AGND and PGND are analog ground and power ground references, respectively. PGND is generally noisier with analog switching transients, and it may also have large static dc currents. AGND is generally quieter and has relatively smaller static dc currents. These two grounds can be connected together outside the chip to a single shared analog ground plane. Regardless, keep PGND and AGND (whether separated or shared) separated from the DGND ground plane if system design constraints permit.

The transient frequencies generated by the analog core can be a full order of magnitude greater than those generated by the SPI and on-chip digital circuitry. Therefore, pay close attention to the decoupling of the VCC and VEE supplies. Each supply must be adequately bypassed to the PGND ground domain using the highest quality bypass capacitors available. Locate the decoupling capacitors as close to the device as practically possible. The decoupling capacitors must have very low ESR and effective series inductance (ESL). Commonly available ceramic capacitors may provide only a marginally low impedance path to ground at the frequencies encountered in the ADATE320. Therefore, consider only the highest performance decoupling capacitors if possible. In accordance with generally accepted practices, a typical 10 μF tantalum capacitor must also be shared across each power supply domain.

Pay particularly close attention to decoupling the VCC and VEE supplies in proximity to the transmission line at the DUTx pins of the device. To avoid undesired waveform aberrations and degradation of performance, it is important that all return currents to and from the transmission line have a direct and low impedance path back to the VCCDx and VEEDx pins adjacent to the respective DUTx pins. See Figure 135 for a typical transmission line decoupling strategy.

The ADATE320 has a DUTGND reference input pin that senses the remote low frequency ground potential at the target device under test (DUT). With the exception of the VIOH and VIOL active load currents and VPMU when in PPMU FI mode, all DAC levels are adjusted on-chip relative to this DUTGND input. Furthermore, the PPMU measure output pins (PPMU_Mx) are also referenced to DUTGND. The off-chip system analog-to-digital converter (ADC) that measures the PPMU_Mx pins must therefore be referenced to DUTGND as well. Referencing the system ADC to AGND results in errors unless DUTGND is tied directly to AGND as close as possible to the ADATE320. For applications that do not distinguish between DUT ground reference and system analog ground reference, the DUTGND pin may be connected to the same ground plane as AGND.

Avoid routing digital lines under the device, because these lines can couple noise into the device. Generous use of an analog ground plane under the device shields noise coupling that can otherwise enter the device. The power supply distribution lines must provide very wide and low inductance paths to the respective supply planes. This is especially true for VCC and VEE. Attention to via inductance is extremely important in these supplies—it cannot be neglected. Fast switching signals routed in proximity to the ADATE320 must be adequately shielded, preferably with their proper ground returns to avoid radiating noise to other parts of the board. Route such lines as far away as possible from the analog inputs to the device, such as the AGND, DUTGND, VREF, and VREFGND reference inputs.

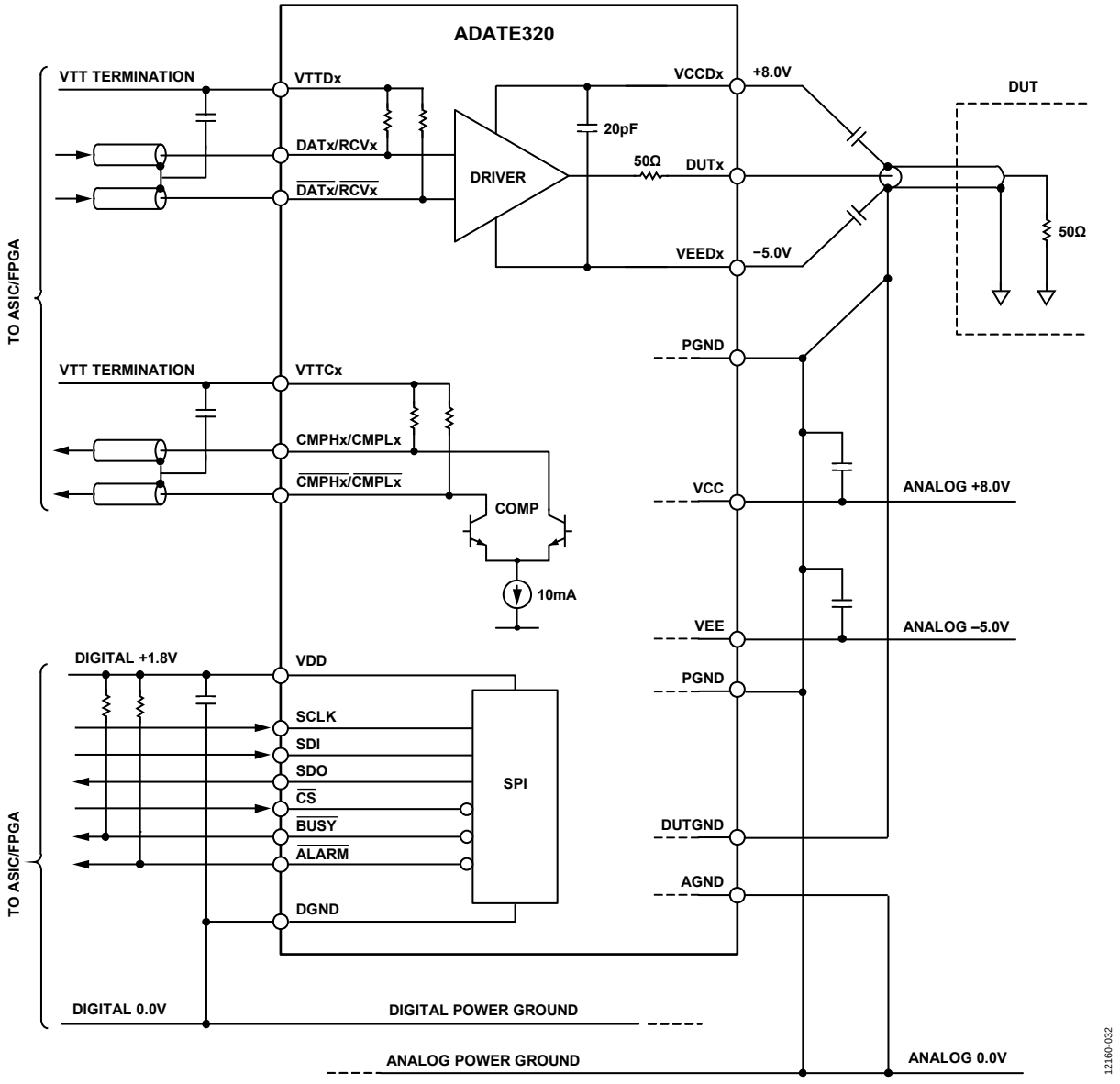


Figure 135. Power Supply and Transmission Path Decoupling Detail

POWER SUPPLY SEQUENCING

The ADATE320 is designed to tolerate sequencing of power supplies in any order. It is therefore not critical that the power supplies be sequenced in any particular order; however, there are recommended best practices.

The ADATE320 has two analog power supplies (VCC, VEE) and one digital power supply (VDD). The analog supplies service all of the analog functions on the chip such as level setting DACs, driver, comparator, load, and PPMU. The digital supply services the SPI and all digital CMOS control circuitry.

There is careful separation between the analog and digital partitions of the chip, and significant effort has been made to decouple these two partitions both functionally and electrically. The analog partition remains in the default configuration in the absence of V_{DD}, and similarly, the digital partition remains in the default configuration in the absence of either (or both) V_{CC} and V_{EE}.

It is not possible to guarantee predictable behavior of the analog partition if either the V_{EE} or V_{CC} supply is poorly conditioned or absent. It is therefore recommended that any externally connected device be disconnected from the DUTx pin to prevent potential damage to that device while either of the V_{EE} or V_{CC} supplies is out of specification.

Assuming the V_{EE} and V_{CC} analog supplies are both applied and within specification, the analog partition ensures that all functions remain in the default configuration. This is true even when the V_{DD} supply is absent and digital CMOS control circuitry is not yet functioning. In such a case (or whenever the $\overline{RST}$ pin is asserted), all of the level setting DACs takes the voltage present at the DUTGND input pin, and all SPI control bits assume their reset default values. The analog functions remain in this safe condition as long as V_{DD} remains absent or as long as the $\overline{RST}$ pin remains asserted.

It is recommended that the $\overline{RST}$ pin always be asserted during the time that the V_{DD} supply is being brought up. If this condition is met, the level setting DACs continue to hold the DUTGND potential after V_{DD} stabilizes and after the $\overline{RST}$ pin is released. A fully clocked reset sequence then initializes the level setting DACs to the reset default conditions as specified in Table 29.

The reset sequence is described in more detail in the SPI Reset Sequence and the Pin section.

In light of these considerations, it is recommended that the two analog supplies be applied first. It is preferable that the smaller valued supply (V_{EE}) be applied before the larger valued supply (V_{CC}). Bring up the digital V_{DD} supply next while the $\overline{RST}$ pin is asserted. After V_{DD} is stable and the $\overline{RST}$ pin is subsequently released, a fully clocked reset sequence must follow. This power supply sequence ensures that analog functions and all level setting DACs receive the proper configuration information during the digital partition reset sequence.

The power supplies must be removed in the reverse order.

Note that VREF and the high speed transmission line termination pins (VTTDx, VTTCx) are all part of the analog partition, but they are not treated as supplies. VREF can be managed independent of V_{CC} and V_{EE}, provided its potential never goes outside those of the V_{EE} and V_{CC} supply buses to prevent ESD protection diodes from becoming forward biased. The VTTDx and VTTCx pins do not have this restriction relative to V_{CC} and V_{EE}, but they must never go outside the absolute maximum ratings as measured with respect to PGND.

DETAILED FUNCTIONAL BLOCK DIAGRAMS

Figure 142 through Figure 145 illustrate the top-level functionality of the capabilities of the ADATE320 for the driver, comparator, active load, and PPMU.

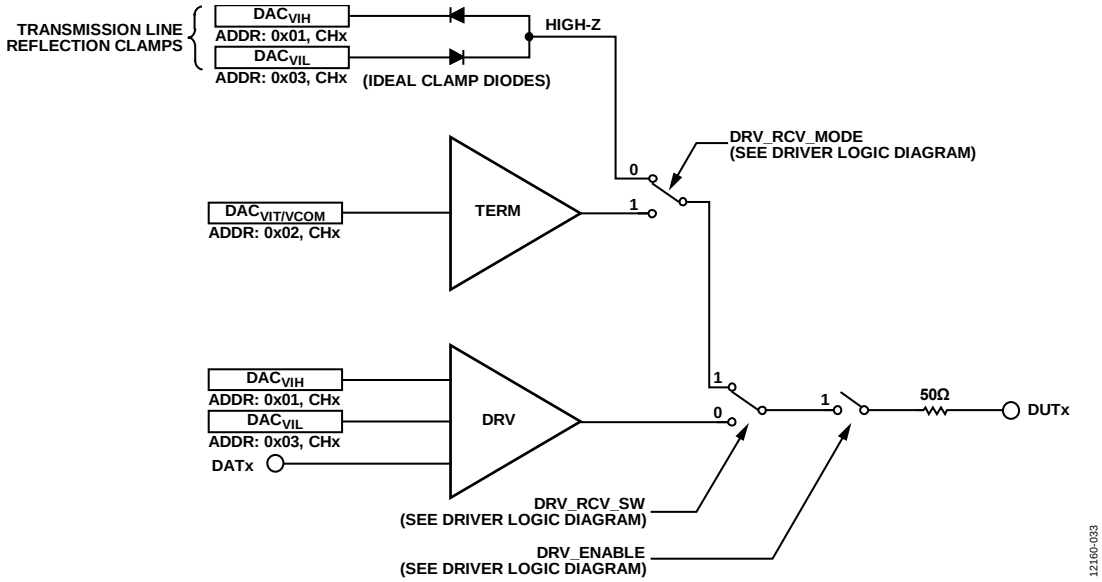


Figure 136. Driver Functional Block Diagram

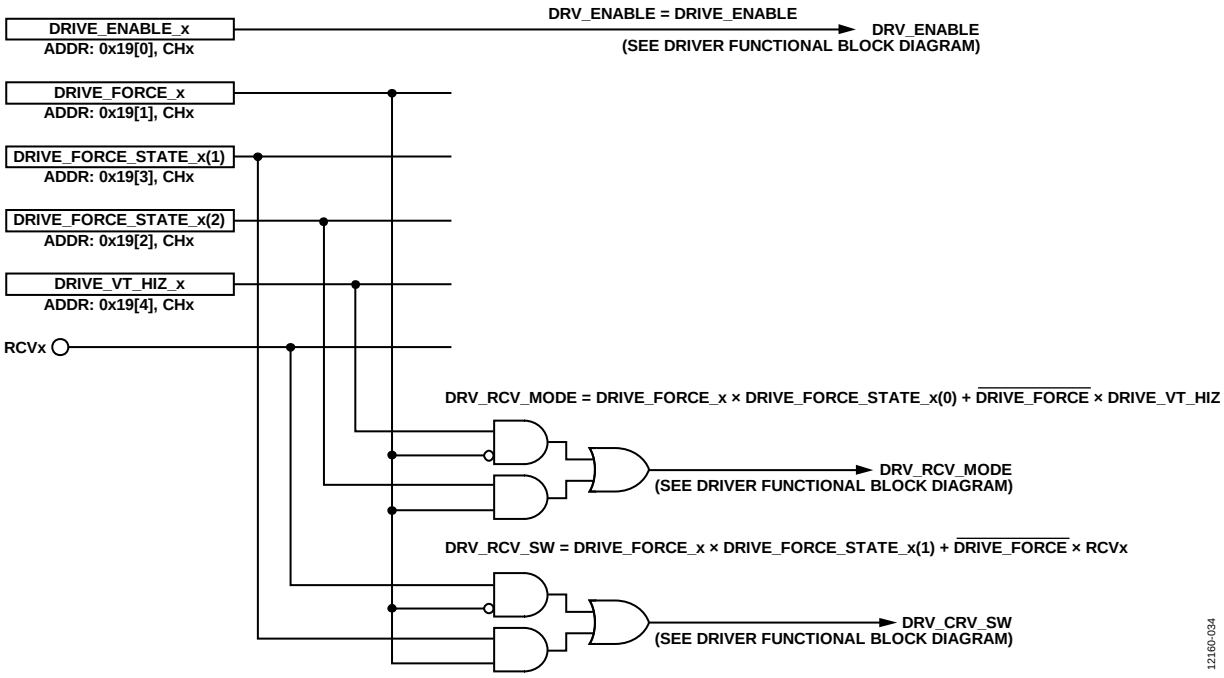


Figure 137. Driver Logic Diagram

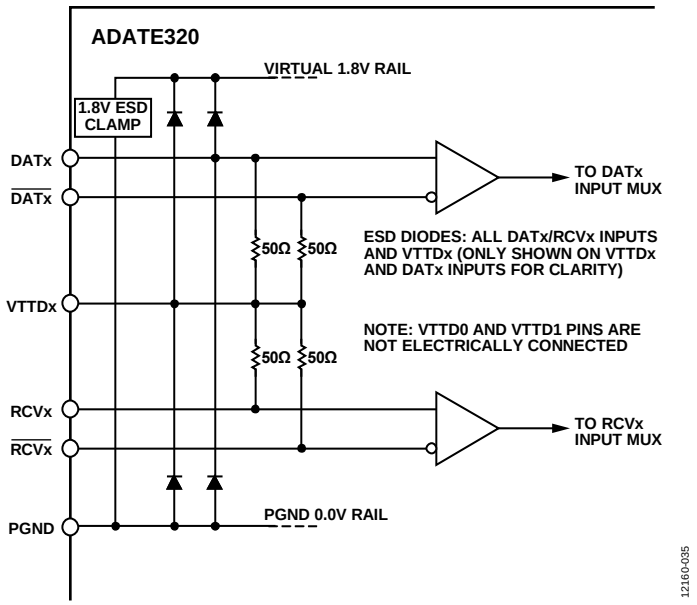


Figure 138. Driver Equivalent Input Stage Diagram

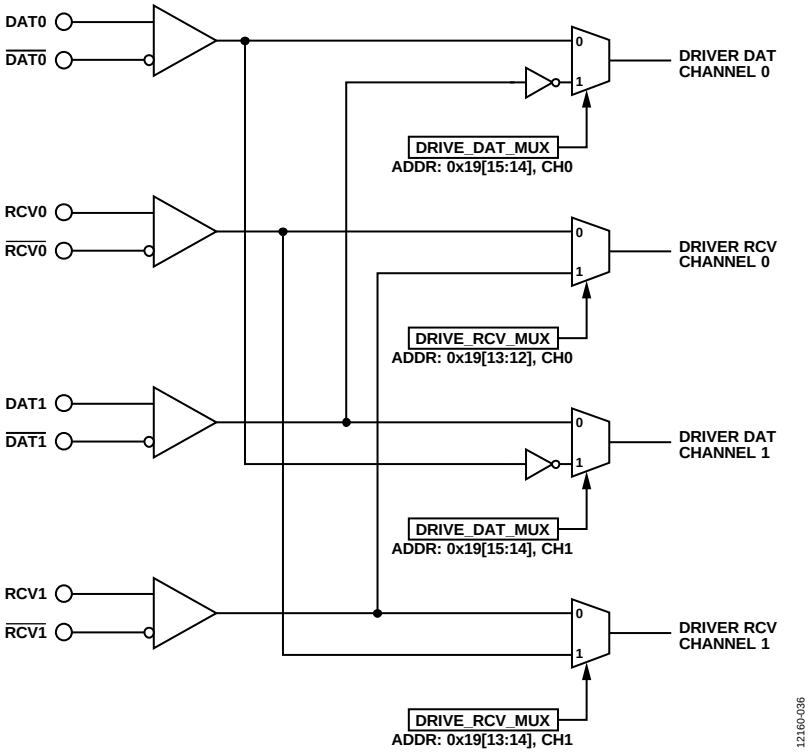


Figure 139. Driver Input Multiplex Diagram

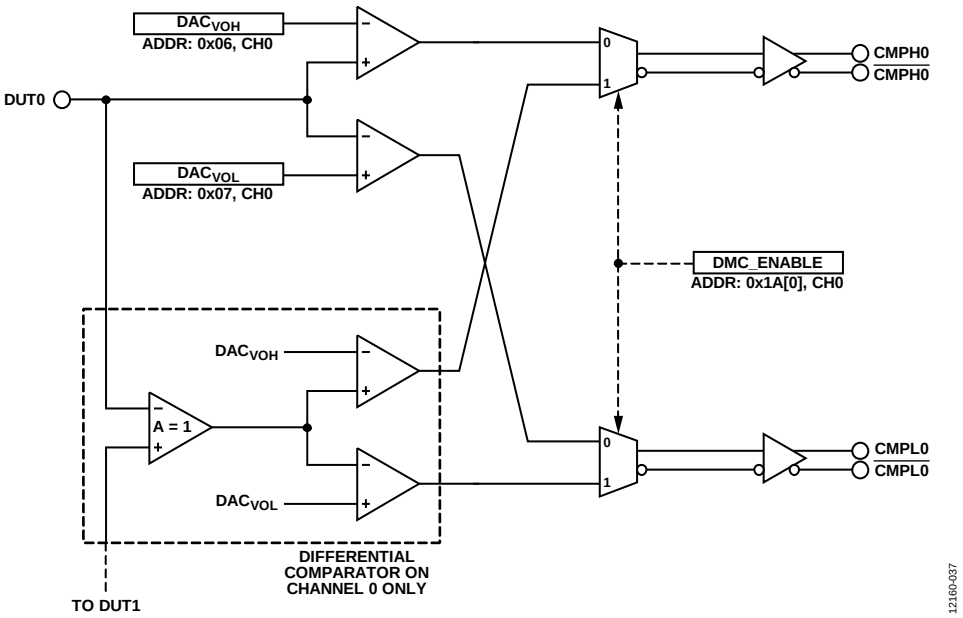


Figure 140. Comparator Functional Block Diagram

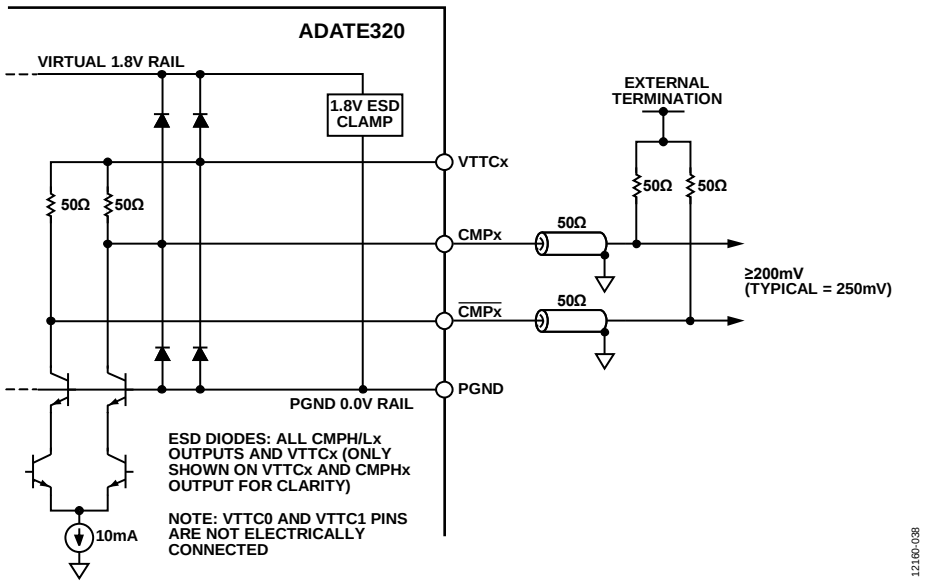


Figure 141. Comparator Equivalent Output Stage Diagram

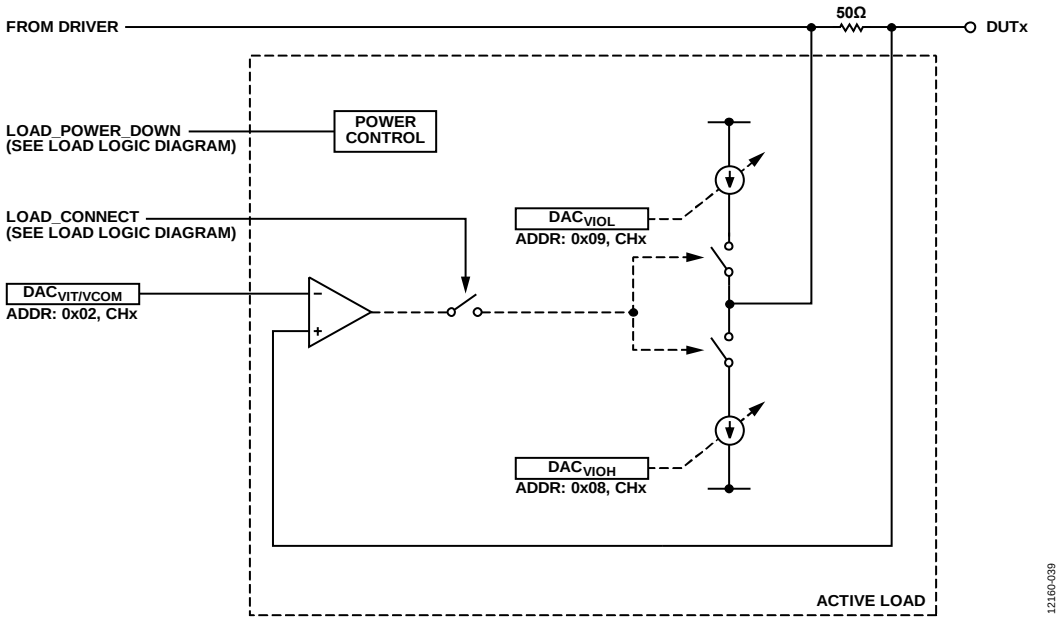


Figure 142. Active Load Functional Block Diagram

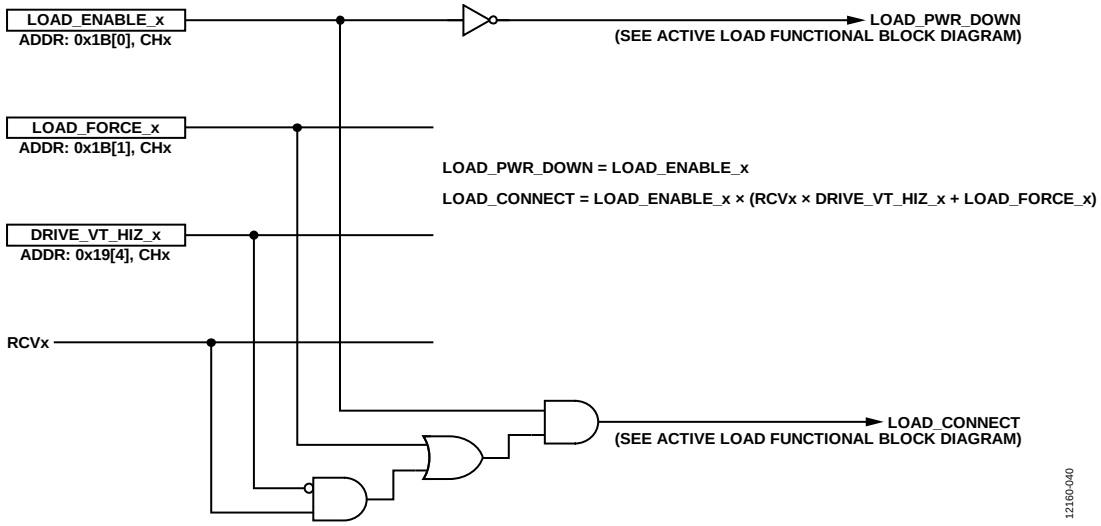
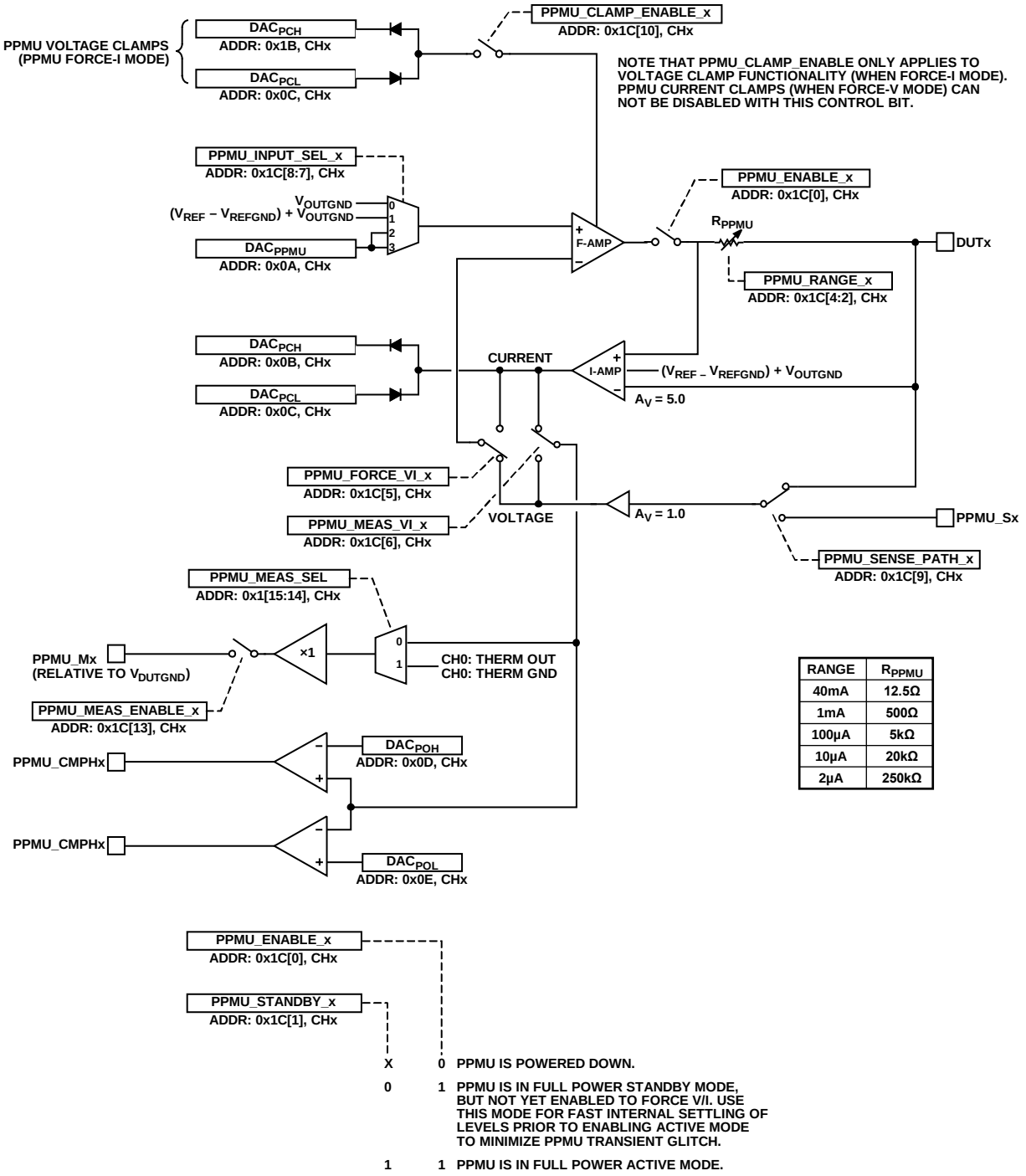
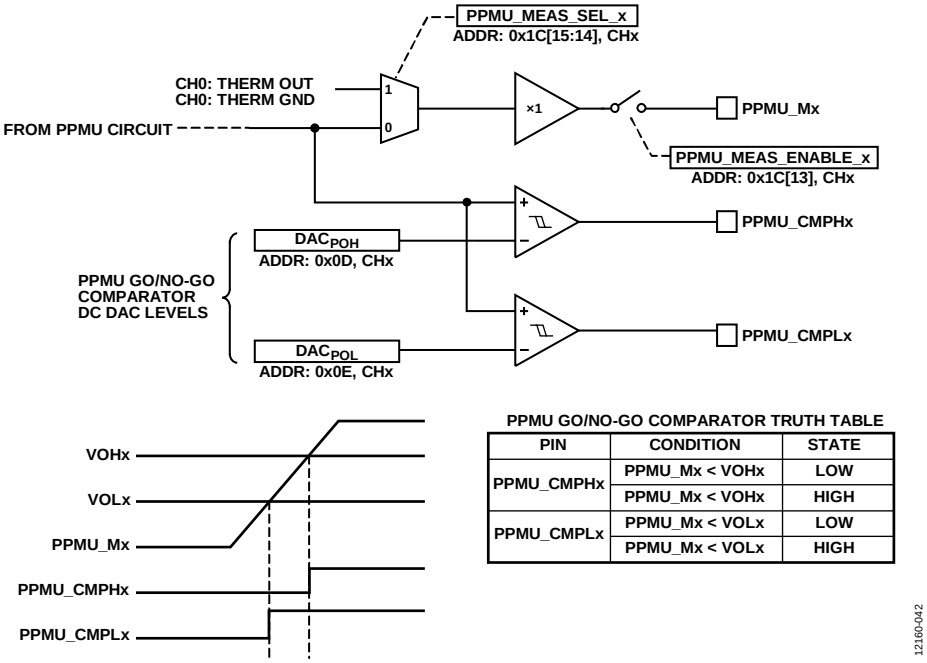


Figure 143. Active Load Functional Logic Diagram



RANGE	R_{PPMU}
40mA	12.5Ω
1mA	500Ω
100µA	5kΩ
10µA	20kΩ
2µA	250kΩ

Figure 144. PPMU Functional Block Diagram



PPMU GO/NO-GO COMPARATOR TRUTH TABLE

PIN	CONDITION	STATE
PPMU_CMPHx	PPMU_Mx < VOHx	LOW
	PPMU_Mx < VOHx	HIGH
PPMU_CMPLx	PPMU_Mx < VOLx	LOW
	PPMU_Mx < VOLx	HIGH

Figure 145. PPMU Go/No-Go Comparator Functional Block Diagram

SPI REGISTER MEMORY MAP AND DETAILS

MEMORY MAP

Table 29. SPI Register Memory Map[1]

CH[1:0][2]	Address (ADDR[6:0])	R/W	DATA[15:0][3]	Register Description	Reset Value
XX	0x00	X	XXXX	NOP	
CC	0x01	R/W	DDDD	VIH DAC level (reset value = 0.0 V)	0x4000
CC	0x02	R/W	DDDD	VIT/VCOM DAC level (reset value = 0.0 V)	0x4000
CC	0x03	R/W	DDDD	VIL DAC level (reset value = 0.0 V)	0x4000
CC	0x04	R/W	DDDD	VCHx DAC level (reset value = V_{MAX})	0xFFFF
CC	0x05	R/W	DDDD	VCLx DAC level (reset value = V_{MIN})	0x0000
CC	0x06	R/W	DDDD	VOHx DAC level (reset value = 4.0 V)	0xA666
CC	0x07	R/W	DDDD	VOLx DAC level (reset value = −1.0 V)	0x2666
CC	0x08	R/W	DDDD	VIOH DAC level (reset value ≥ 0 µA)[4]	0x4000
CC	0x09	R/W	DDDD	VIOL DAC level (reset value ≥ 0 µA)[4]	0x4000
CC	0x0A	R/W	DDDD	PPMU DAC level (reset value = 0.0 V)	0x4000
CC	0x0B	R/W	DDDD	PCHx DAC level (reset value = V_{MAX})	0xFFFF
CC	0x0C	R/W	DDDD	PCLx DAC level (reset value = V_{MIN})	0x0000
CC	0x0D	R/W	DDDD	POHx DAC level (reset value = 4.0 V)	0xA666
CC	0x0E	R/W	DDDD	POLx DAC level (reset value = −1.0 V)	0x2666
01	0x0F	R/W	DDDD	OVDL DAC level (reset value = V_{MIN})	0x0000
10	0x0F	R/W	DDDD	OVDH DAC level (reset value = V_{MAX})	0xFFFF
XX	0x10	X	XXXX	Reserved	
CC	0x11	R/W	DDDD	DAC control register	0x0000
01	0x12	R/W	DDDD	SPI control register	0x0000
XX	0x13 to 0x18	X	XXXX	Reserved	
CC	0x19	R/W	DDDD	DRV control register	0x0000
CC	0x1A	R/W	DDDD	CMP control register	0xFF00
CC	0x1B	R/W	DDDD	Load control register	0x0003
CC	0x1C	R/W	DDDD	PPMU control register	0x0000
01	0x1D	R/W	DDDD	Alarm mask register	0x0085
10	0x1D	R/W	DDDD	Alarm mask register	0x0005
CC	0x1E	R	DDDD	Alarm state register	0x0000
CC	0x1F	R/W	DDDD	Product serialization code register	Unique
XX	0x20	X	XXXX	NOP	
CC	0x21	R/W	DDDD	VIH (driver high level) m coefficient	0xFFFF
CC	0x22	R/W	DDDD	VIT (driver term level) m coefficient	0xFFFF
CC	0x23	R/W	DDDD	VIL (driver low level) m coefficient	0xFFFF
CC	0x24	R/W	DDDD	VCHx (driver reflection clamp) m coefficient	0xFFFF
CC	0x25	R/W	DDDD	VCLx (driver reflection clamp) m coefficient	0xFFFF
CC	0x26	R/W	DDDD	VOHx (normal window comparator) m coefficient	0xFFFF
CC	0x27	R/W	DDDD	VOLx (normal window comparator) m coefficient	0xFFFF
CC	0x28	R/W	DDDD	VIOH (active load IOHx) m coefficient	0xFFFF
CC	0x29	R/W	DDDD	VIOL (active load IOL) m coefficient	0xFFFF
CC	0x2A	R/W	DDDD	PPMU (PPMU FV) m coefficient	0xFFFF
CC	0x2B	R/W	DDDD	PCHx (PPMU voltage clamp, FI) m coefficient	0xFFFF
CC	0x2C	R/W	DDDD	PCLx (PPMU voltage clamp, FI) m coefficient	0xFFFF
CC	0x2D	R/W	DDDD	POHx (PPMU comparator MV) m coefficient	0xFFFF
CC	0x2E	R/W	DDDD	POLx (PPMU comparator MV) m coefficient	0xFFFF
01	0x2F	R/W	DDDD	OVDL m coefficient	0xFFFF
10	0x2F	R/W	DDDD	OVDH m coefficient	0xFFFF

CH[1:0][2]	Address (ADDR[6:0])	R/W	DATA[15:0][3]	Register Description	Reset Value
XX	0x30	X	XXXX	Reserved	
CC	0x31	R/W	DDDD	VIH (driver high level) c coefficient	0x8000
CC	0x32	R/W	DDDD	VIT (driver term level) c coefficient	0x8000
CC	0x33	R/W	DDDD	VIL (driver low level) c coefficient	0x8000
CC	0x34	R/W	DDDD	VCHx (driver reflection clamp) c coefficient	0x8000
CC	0x35	R/W	DDDD	VCLx (driver reflection clamp) c coefficient	0x8000
CC	0x36	R/W	DDDD	VOHx (normal window comparator) c coefficient	0x8000
CC	0x37	R/W	DDDD	VOLx (normal window comparator) c coefficient	0x8000
CC	0x38	R/W	DDDD	VIOH (active load IOHx) c coefficient	0x8000
CC	0x39	R/W	DDDD	VIOL (active load IOL) c coefficient	0x8000
CC	0x3A	R/W	DDDD	PPMU (PPMU FV) c coefficient	0x8000
CC	0x3B	R/W	DDDD	PCHx (PPMU voltage clamp, FI) c coefficient	0x8000
CC	0x3C	R/W	DDDD	PCLx (PPMU voltage clamp, FI) c coefficient	0x8000
CC	0x3D	R/W	DDDD	POHx (PPMU comparator MV) c coefficient	0x8000
CC	0x3E	R/W	DDDD	POLx (PPMU comparator MV) c coefficient	0x8000
01	0x3F	R/W	DDDD	OVDL c coefficient	0x8000
10	0x3F	R/W	DDDD	OVDH c coefficient	0x8000
XX	0x40 to 0x41	X	XXXX	Reserved	
CC	0x42	R/W	DDDD	VCOM (active load) m coefficient	0xFFFF
XX	0x43	X	XXXX	Reserved	
CC	0x44	R/W	DDDD	PCHx (PPMU current clamp, FV) m coefficient	0xFFFF
CC	0x45	R/W	DDDD	PCLx (PPMU current clamp, FV) m coefficient	0xFFFF
01	0x46	R/W	DDDD	VOHx (differential comparator) m coefficient	0xFFFF
01	0x47	R/W	DDDD	VOLx (differential comparator) m coefficient	0xFFFF
XX	0x48 to 0x49	X	XXXX	Reserved	
CC	0x4A	R/W	DDDD	PPMU FI Range A m coefficient	0xFFFF
CC	0x4B	R/W	DDDD	PPMU FI Range B m coefficient	0xFFFF
CC	0x4C	R/W	DDDD	PPMU FI Range C m coefficient	0xFFFF
CC	0x4D	R/W	DDDD	PPMU FI Range D m coefficient	0xFFFF
CC	0x4E	R/W	DDDD	PPMU FI Range E m coefficient	0xFFFF
XX	0x4F	X	XXXX	Reserved	
XX	0x50 to 0x51	X	XXXX	Reserved	
CC	0x52	R/W	DDDD	VCOM (active load) c coefficient	0x8000
XX	0x53	X	XXXX	Reserved	
CC	0x54	R/W	DDDD	PCHx (PPMU current clamp, FV) c coefficient	0x8000
CC	0x55	R/W	DDDD	PCLx (PPMU current clamp, FV) c coefficient	0x8000
01	0x56	R/W	DDDD	VOHx (differential comparator) c coefficient	0x8000
01	0x57	R/W	DDDD	VOLx (differential comparator) c coefficient	0x8000
XX	0x58 to 0x59	X	XXXX	Reserved	
CC	0x5A	R/W	DDDD	PPMU FI c coefficient	0x8000
XX	0x5B to 0x5C	X	XXXX	Reserved	
CC	0x5D	R/W	DDDD	POHx (PPMU comparator MI) c coefficient	0x8000
CC	0x5E	R/W	DDDD	POLx (PPMU comparator MI) c coefficient	0x8000
XX	0x5F	X	XXXX	Reserved	
XX	0x60	X	XXXX	Reserved	
CC	0x61	R/W	DDDD	POHx (PPMU comparator MI Range A) m coefficient	0xFFFF
CC	0x62	R/W	DDDD	POHx (PPMU comparator MI Range B) m coefficient	0xFFFF
CC	0x63	R/W	DDDD	POHx (PPMU comparator MI Range C) m coefficient	0xFFFF
CC	0x64	R/W	DDDD	POHx (PPMU comparator MI Range D) m coefficient	0xFFFF
CC	0x65	R/W	DDDD	POHx (PPMU comparator MI Range E) m coefficient	0xFFFF
CC	0x66	R/W	DDDD	POLx (PPMU comparator MI Range A) m coefficient	0xFFFF

CH[1:0][2]	Address (ADDR[6:0])	R/W	DATA[15:0][3]	Register Description	Reset Value
CC	0x67	R/W	DDDD	POLx (PPMU comparator MI Range B) m coefficient	0xFFFF
CC	0x68	R/W	DDDD	POLx (PPMU comparator MI Range C) m coefficient	0xFFFF
CC	0x69	R/W	DDDD	POLx (PPMU comparator MI Range D) m coefficient	0xFFFF
CC	0x6A	R/W	DDDD	POLx (PPMU comparator MI Range E) m coefficient	0xFFFF
XX	0x6B to 0x7F	X	XXXX	Reserved	

[1] X means don't care for the respective field.
[2] CC represents two contiguous binary channel bits.
[3] DDDD represents four-digit hexadecimal data.
[4] The active load VIOHx and VIOLx voltage offsets are guaranteed to be nonzero and positive. These offsets result in a nonzero current for each IOHx and IOLx level following valid reset sequence and prior to calibration. Furthermore, the active load is forced into the active on state following a reset, which facilitates a soft connect of the DUTx pin to VCOMx = 0.0 V following a valid reset sequence (with small but nonzero IOHx and IOLx currents).

REGISTER DETAILS

Reserved bits in any register are undefined. In some cases, a physical but unused memory bit may be present.

Any SPI read operation from a reserved bit or register results in an unknown but deterministic readback value. Any SPI write operation to a reserved bit or register results in no action.

A write to a control bit or control register defined only on Channel 0 must be addressed to Channel 0. Any such write that is addressed to only Channel 1 is ignored if no register or control bit is defined on Channel 1.

Furthermore, any such write that is addressed to both Channel 0 and Channel 1 (as a multichannel write) proceeds as if the write is addressed to both Channel 0 and Channel 1. If no register or control bit is defined at Channel 1, data addressed to the undefined Channel 1 is ignored. If a register or control bit is defined at Channel 1, it is filled as part of the multichannel write.

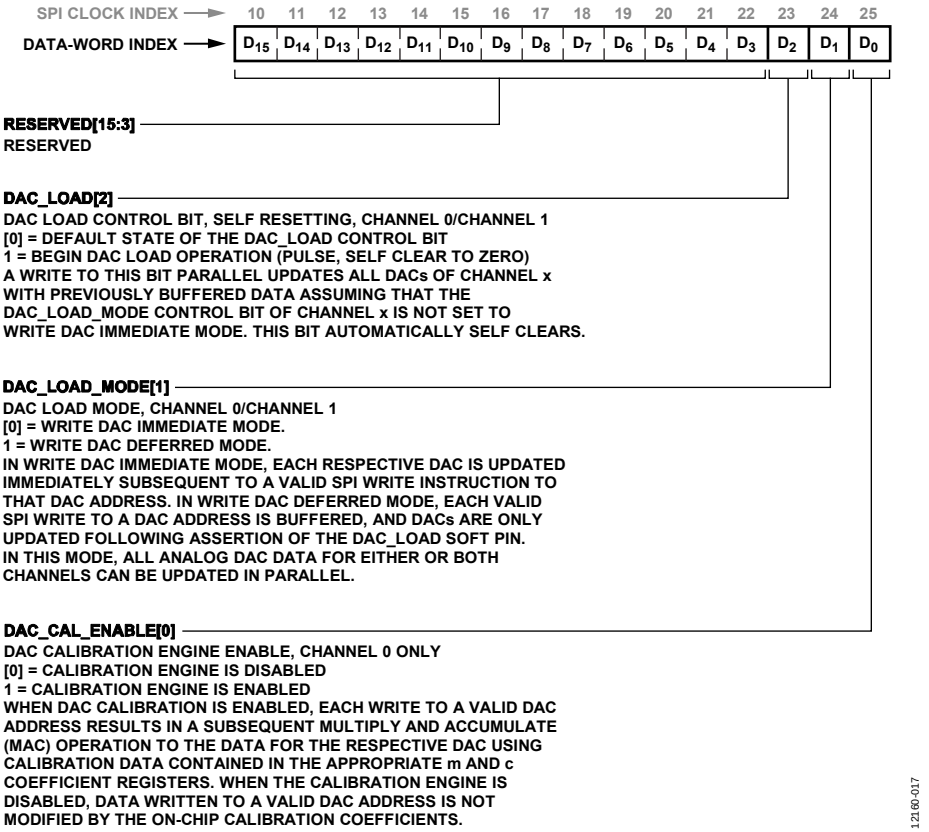


Figure 146. DAC Control Register (Address 0x11)

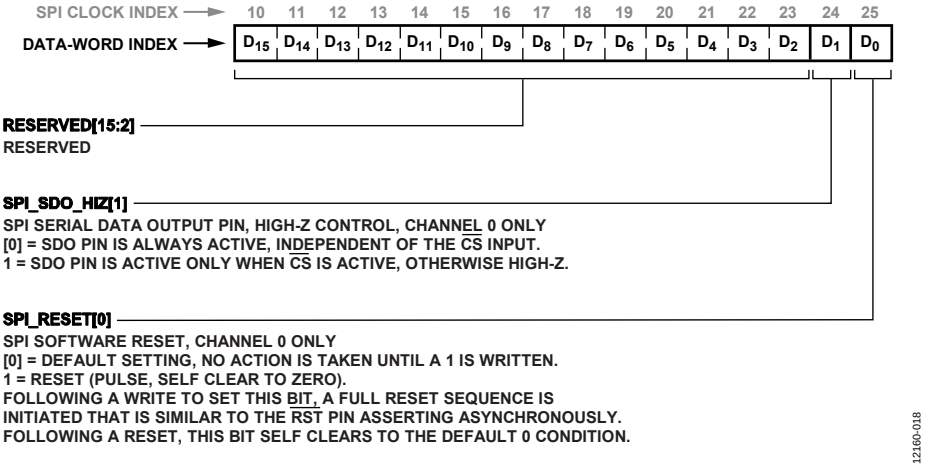


Figure 147. SPI Control Register (Address 0x12)

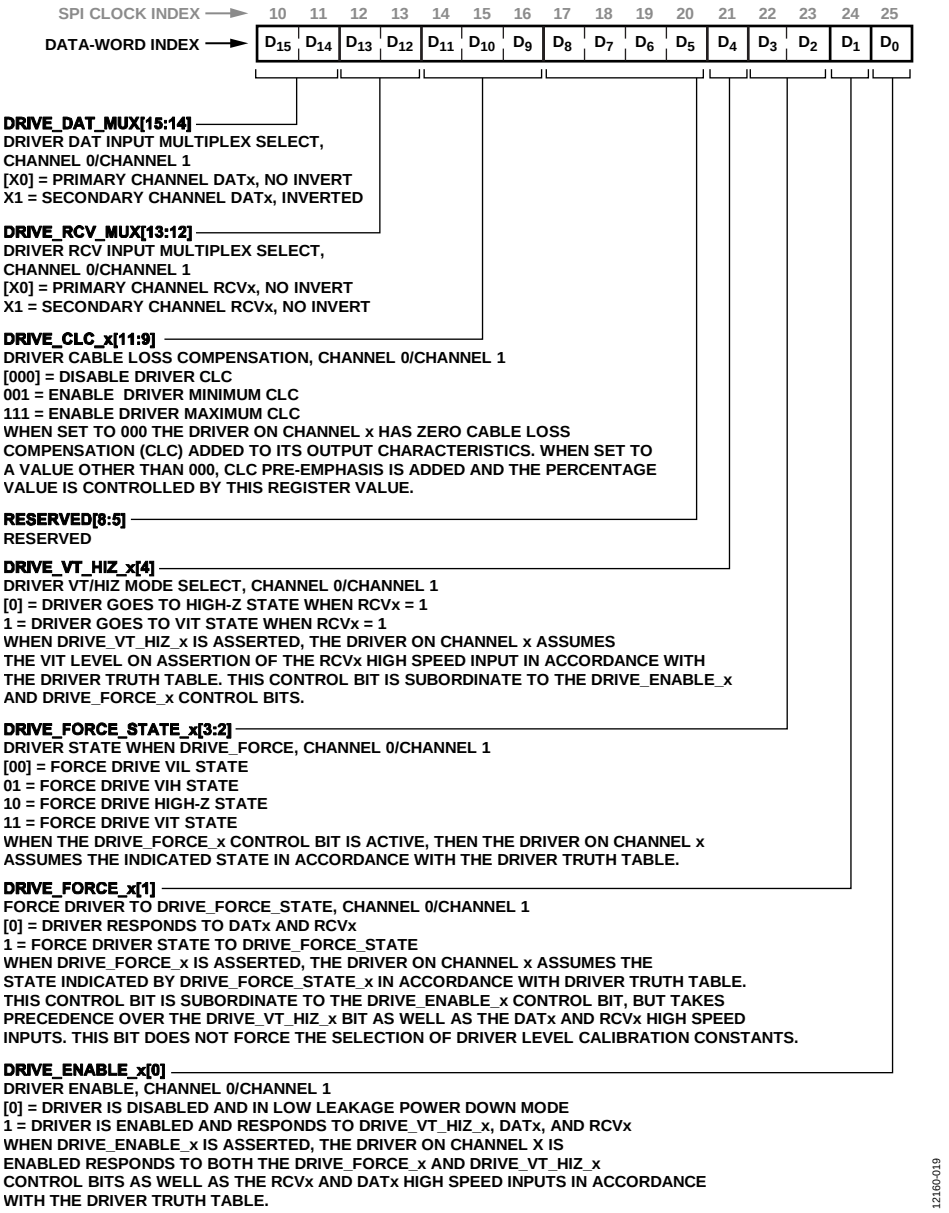


Figure 148. DRV Control Register (Address 0x19)

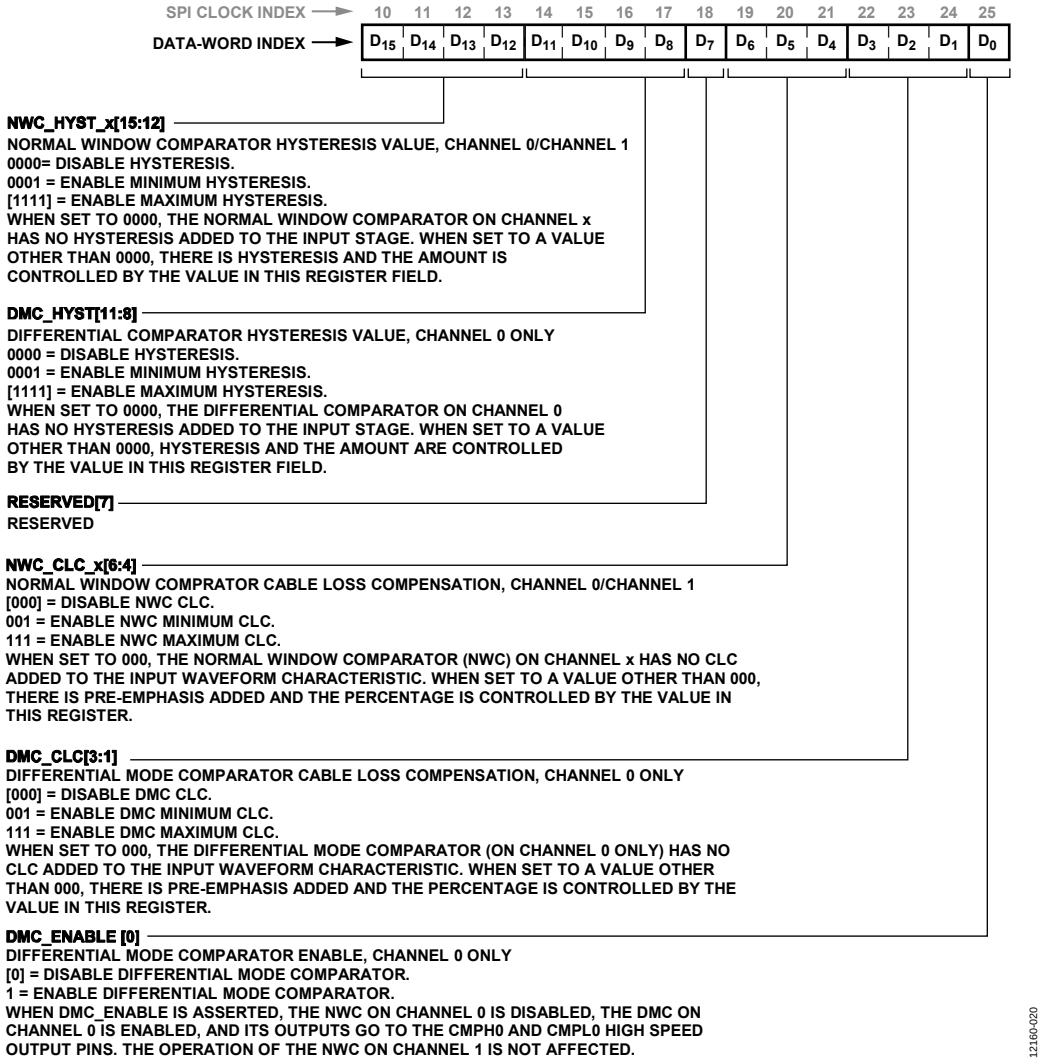


Figure 149. CMP Control Register (Address 0x1A)

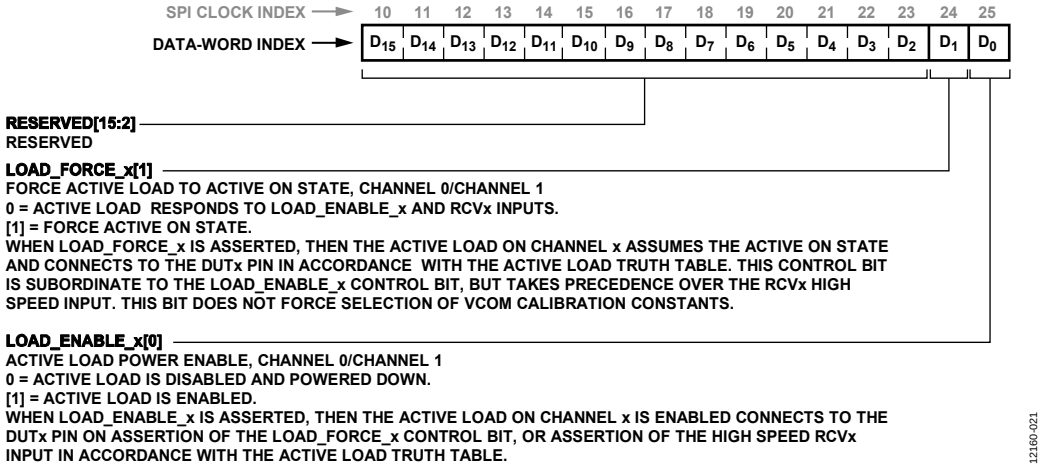


Figure 150. Load Control Register (Address 0x1B)

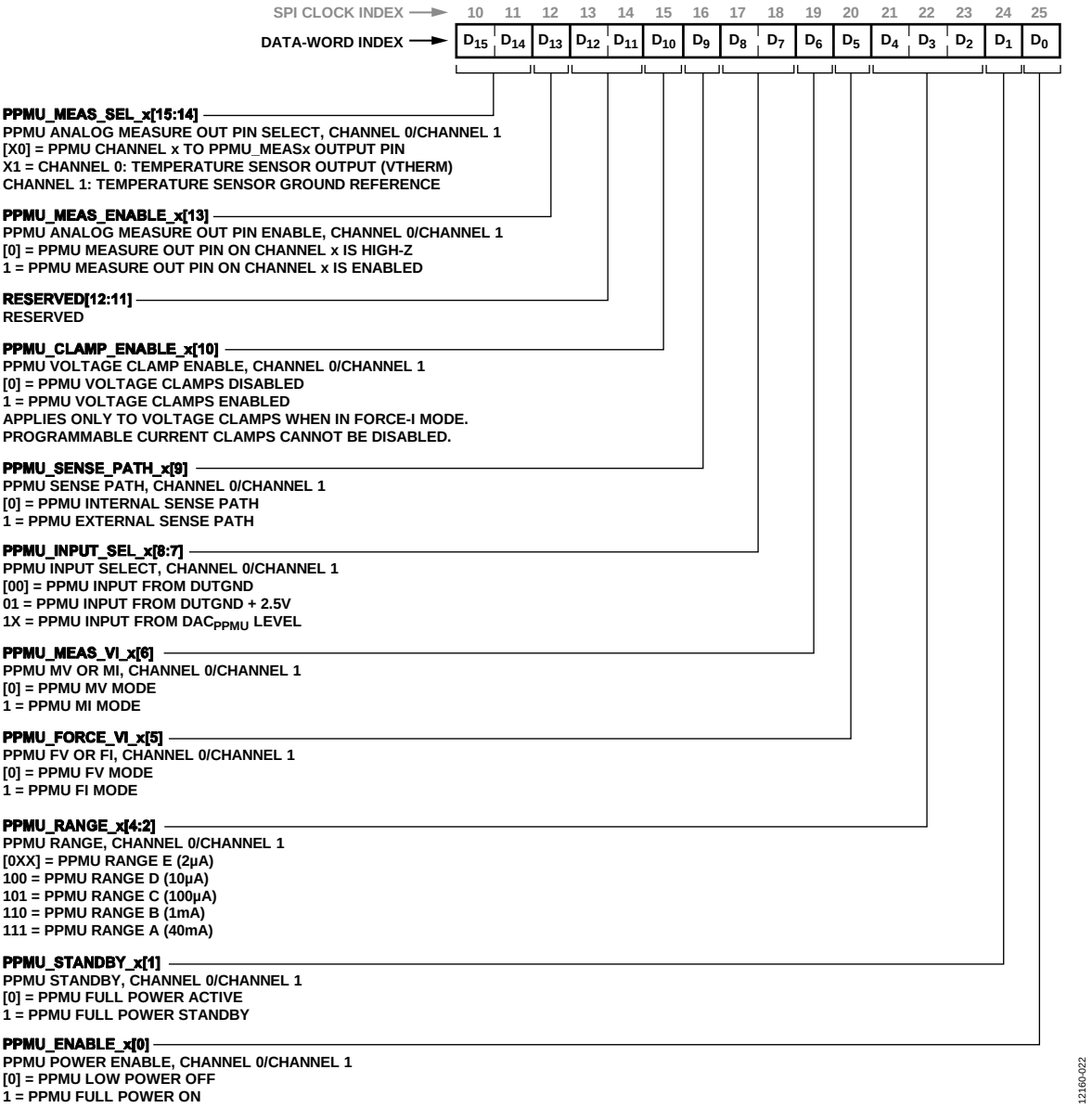


Figure 151. PPMU Control Register (Address 0x1C)

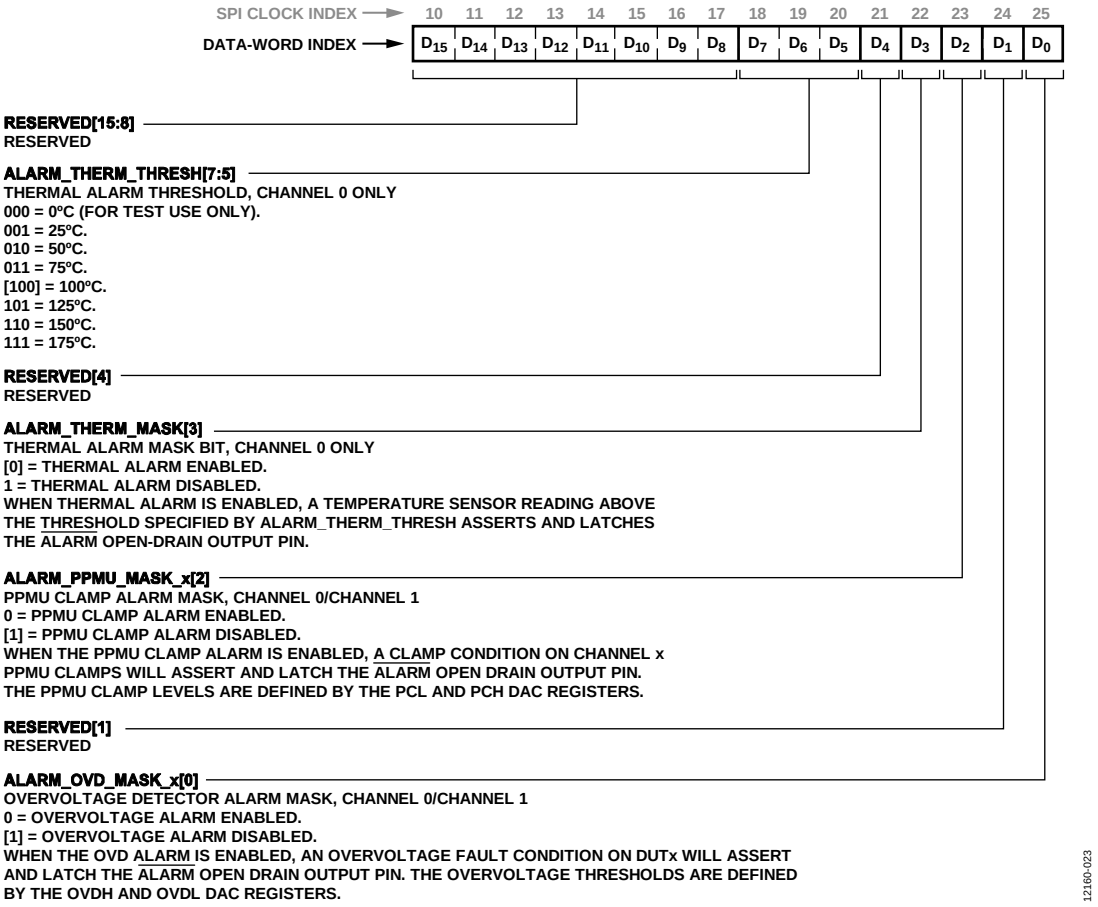


Figure 152. Alarm Mask Register (Address 0x1D)

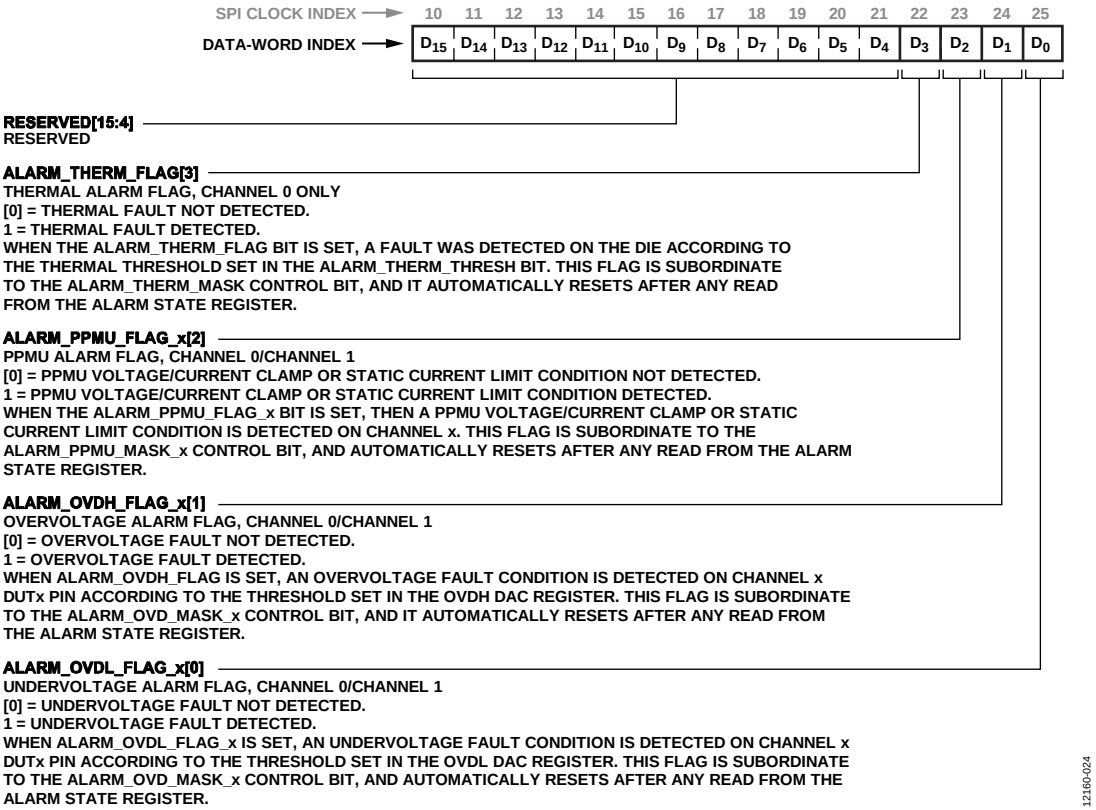


Figure 153. Alarm State Register (Address 0x1E) (Read Only)

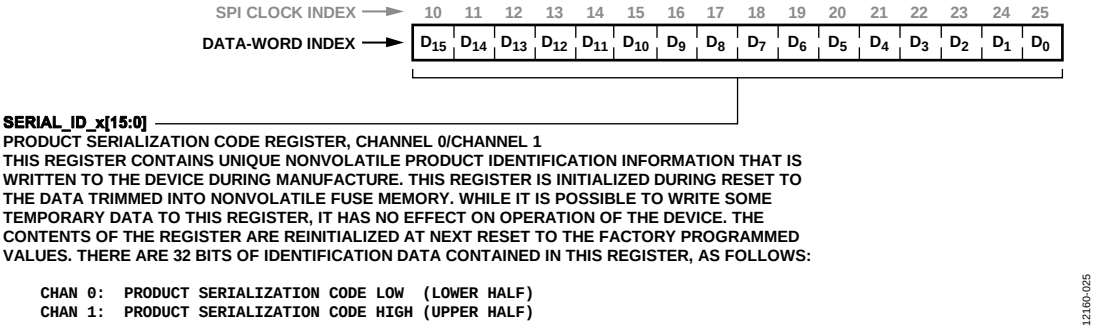


Figure 154. Product Serialization Code Register (Address 0x1F)

DEFAULT TEST CONDITIONS

Table 30. Default Test Conditions

Name	SPI Address	Default Test Condition	Description
VIHx DAC Levels	Address 0x01[x]	2.0 V	
VITx/VCOMx DAC Levels	Address 0x02[x]	1.0 V	
VILx DAC Levels	Address 0x03[x]	0.0 V	
VOHx DAC Levels	Address 0x06[x]	5.0 V	
VOLx DAC Levels	Address 0x07[x]	−2.0 V	
POHx DAC Levels	Address 0x0D[x	5.5 V	
POLx DAC Levels	Address 0x0E[x]	−2.0 V	
VCHx DAC Levels	Address 0x04[x]	5.0 V	
VCLx DAC Levels	Address 0x05[x]	−2.0 V	
PCHx DAC Levels	Address 0x0B[x]	7.0 V	
PCLx DAC Levels	Address 0x0C[x]	−2.0 V	
VIOHx DAC Levels	Address 0x08[x]	0.0 mA	
VIOLx DAC Levels	Address 0x09[x]	0.0 mA	
PPMUx DAC Levels	Address 0x0A[x]	0.0 V	
OVDH DAC Level	Address 0x0F[1]	5.0 V	
OVDL DAC Level	Address 0x0F[0]	−2.0 V	
DAC Control Register	Address 0x11[0]	0x0000	DAC calibration disabled, DAC load mode is immediate
SPI Control Register	Address 0x12[1]	0x0000	SDO pin is always active, independent of $\overline{CS}$ state
DRV Control Registers	Address 0x19[x]	0x0000	Driver disabled in low leakage mode, DATx/RCVx inputs are multiplexed to primary channels, CLC is off, driver responds high-Z to RCVx inputs when enabled
CMP Control Registers	Address 0x1A[x]	0x0000	Normal window comparator mode, CLC is off, hysteresis is off
LOAD Control Registers	Address 0x1B[x]	0x0000	Active load is disabled and in power-down mode
PPMU Control Registers	Address 0x1C[x]	0x0000	PPMU disabled and in power-down mode, mode set FVMV Range E, input select V_{DUTGND} internal sense path to V_{DUTx}, PPMU_Mx pins high-Z, clamps disabled
ALARM Mask Registers	Address 0x1D[x]	0x0085	Disable PPMU and overvoltage detector alarm functions
Calibration m Coefficients	Not applicable	1.0 (0xFFFF)	
Calibration c Coefficients	Not applicable	0.0 (0x8000)	
DATx, RCVx Inputs	Not applicable	Static low	
SCLK Input	Not applicable	Static low	
DUTx Pins	Not applicable	Unterminated	
CMPHx, CMPLx Outputs	Not applicable	Unterminated	
V_{DUTGND}	Not applicable	0.0 V	

EXTERNAL COMPONENTS

In addition to the external components identified in Table 31 and Table 32, see the Power Supply, Grounding, and Typical Decoupling Strategy section for further information about recommended power supply decoupling capacitors.

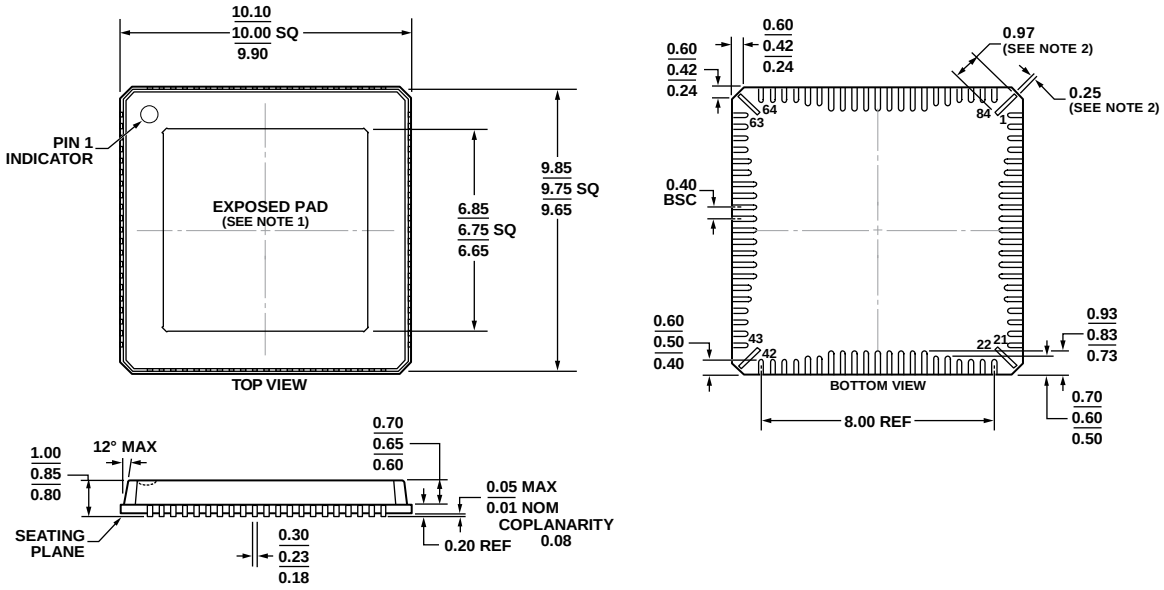
Table 31. PPMU External Compensation Capacitors

External Components Value (pF)	Location
1000 pF	Between the CFFB0 and CFFA0 pins
1000 pF	Between the CFFB1 and CFFA1 pins

Table 32. Other External Components

External Components Value (kΩ)	Location
10 kΩ	$\overline{\text{ALARM}}$ pull-up resistor to VDD
1 kΩ	$\overline{\text{BUSY}}$ pull-up resistor to VDD

OUTLINE DIMENSIONS



NOTES:
1. FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET.
2. TIEBARS MAY OR MAY NOT BE SOLDERED TO THE BOARD.

07-02-2012-B

Figure 155. 84-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
10 mm × 10 mm Body, Very Thin Quad
(CP-84-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADATE320KCPZ	25°C to 75°C	84-Lead LFCSP_VQ with Exposed Pad (Tray)	CP-84-2
ADATE320-1KCPZ	25°C to 75°C	84-Lead LFCSP_VQ with Exposed Pad (Tray)	CP-84-2

[1] Z = RoHS Compliant Part.

D12160-0-9/16(B)