

SN74AHC174 Hex D-Type Flip-Flops With Clear

1 Features

1. Operating range 2V to 5.5V V_{CC}
2. Contain six flip-flops with single-rail outputs
3. Latch-up performance exceeds 250mA per JESD 17

2 Applications

- Buffer/Storage Registers
- Shift Registers
- Pattern Generators

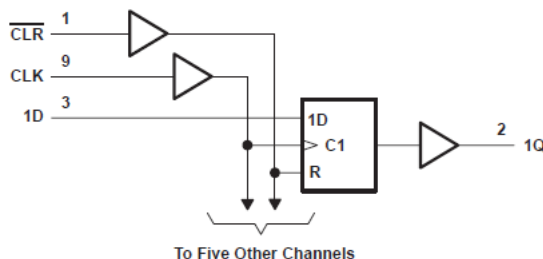
3 Description

The 'AHC174 devices are positive-edge-triggered D-type flip-flops with a direct clear ($\overline{CLR}$) input and are designed for 2V to 5.5V V_{CC} operation.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SN74AHC174	D (SOIC, 16)	9.9mm × 6mm	9.9mm × 3.9mm
	DB (SSOP, 16)	6.2mm × 7.8mm	6.2mm × 5.3mm
	N (PDIP, 16)	19.3mm × 9.4mm	19.3mm × 6.35mm
	PW (TSSOP, 16)	5mm × 6.4mm	5mm × 4.4mm

- (1) For more information, see [Mechanical, Packaging, and Orderable Information](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)



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4 Pin Configuration and Functions

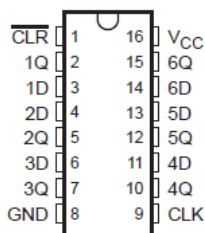


Figure 4-1. D, DB, DGV, N, NS, or PW Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
CLR	1	I	Clear Pin
1Q	2	O	1Q Output
1D	3	I	1D Input
2D	4	I	2D Input
2Q	5	O	2Q Output
3D	6	I	3D Input
3Q	7	O	3Q Output
GND	8	—	Ground Pin
CLK	9	I	Clock Pin
4Q	10	O	4Q Output
4D	11	I	4D Input
5Q	12	O	5Q Output
5D	13	I	5D Input
6D	14	I	6D Input
6Q	15	O	6Q Output
V _{CC}	16	P	Power Pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	–0.5	7	V
V _I ⁽²⁾	Input voltage	–0.5	7	V
V _O ⁽²⁾	Output voltage	–0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	(V _I < 0)	–20	mA
I _{OK}	Output clamp current	(V _O < 0)	±20	mA
I _O	Continuous output current	(V _O = 0 to V _{CC})	±25	mA
	Continuous current through V _{CC} or GND		±50	mA
T _{stg}	Storage temperature range	–65	150	°CW

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output damp current ratings are observed.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	V
		V _{CC} = 3 V	2.1	
		V _{CC} = 5.5 V	3.85	
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	V
		V _{CC} = 3 V	0.9	
		V _{CC} = 5.5 V	1.65	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	–50	μA
		V _{CC} = 3.3 V ± 0.3 V	–4	mA
		V _{CC} = 5 V ± 0.5 V	–8	
I _{OL}	Low-level output current	V _{CC} = 2 V	50	μA
		V _{CC} = 3.3 V ± 0.3 V	4	mA
		V _{CC} = 5 V ± 0.5 V	8	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V	100	ns/V
		V _{CC} = 5 V ± 0.5 V	20	
T _A	Operating free-air temperature	–40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, [Implications of Slow or Floating CMOS Inputs](#).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AHC174						UNIT
		D	DB	DGV	N	NS	PW	
		16 PINS						
R _{θJA}	Junction-to-ambient thermal resistance	73	82	120	67	64	135.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN74AHC174		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = –50 μA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I _{OH} = –4 mA	3 V	2.58			2.48		
	I _{OH} = –8 mA	4.5 V	3.94			3.8		
V _{OL}	I _{OL} = 50 μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I _{OL} = 4 mA	3 V			0.36		0.44	
	I _{OL} = 8 mA	4.5			0.36		0.44	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			± 0.1		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40	μA
C _i	V _I = V _{CC} or GND	5 V		1.7	10		10	pF

5.6 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted)

			T _A = 25°C		SN74AHC174		UNIT
			MIN	MAX	MIN	MAX	
t _w	Pulse duration	CLR low	5		5		ns
		CLK high or low	5		5		
t _{su}	Setup time before CLK↑	Data	5		6		ns
		CLR inactive	3		3		
t _h	Hold time, data after CLK↑		0		0		ns

5.7 Timing Requirements, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted)

			T _A = 25°C		SN74AHC174		UNIT
			MIN	MAX	MIN	MAX	
t _w	Pulse duration	CLR low	5		5		ns
		CLK high or low	5		5		
t _{su}	Setup time before CLK↑	Data	4.5		4.5		ns
		CLR inactive	2.5		2.5		
t _h	Hold time, data after CLK↑		0.5		0.5		ns

5.8 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74AHC174		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	95 ¹	170 ¹		80		MHz
			$C_L = 50\text{ pF}$	55	130		50		
t_{PHL}	$\overline{\text{CLR}}$	Any Q	$C_L = 15\text{ pF}$		4.5 ¹	11.4 ¹	1	13.5	ns
t_{PLH}	CLK	Any Q	$C_L = 15\text{ pF}$		5.8 ¹	11 ¹	1	13	ns
t_{PHL}					5.8 ¹	11 ¹	1	13	
t_{PHL}	$\overline{\text{CLR}}$	Any Q	$C_L = 50\text{ pF}$		6	14.9	1	17	ns
t_{PLH}	CLK	Any Q	$C_L = 50\text{ pF}$		7.5	14.5	1	16.5	ns
t_{PHL}					7.5	14.5	1	16.5	
$t_{\text{sk(o)}}$			$C_L = 50\text{ pF}$			1.5 ²		1.5	ns

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.
2. On products compliant to MIL-PRF-38535, this parameter does not apply.

5.9 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74AHC174		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	130 ¹	240 ¹		110		MHz
			$C_L = 50\text{ pF}$	90	180		80		
t_{PHL}	$\overline{\text{CLR}}$	Any Q	$C_L = 15\text{ pF}$		3 ¹	7.6 ¹	1	9	ns
t_{PLH}	CLK	Any Q	$C_L = 15\text{ pF}$		4.1 ¹	7.2 ¹	1	8.5	ns
t_{PHL}					4.1 ¹	7.2 ¹	1	8.5	
t_{PHL}	$\overline{\text{CLR}}$	Any Q	$C_L = 50\text{ pF}$		4.2	9.6	1	11	ns
t_{PLH}	CLK	Any Q	$C_L = 50\text{ pF}$		5.5	9.2	1	10.5	ns
t_{PHL}					5.5	9.2	1	10.5	
$t_{\text{sk(o)}}$			$C_L = 50\text{ pF}$			1 ²		1	ns

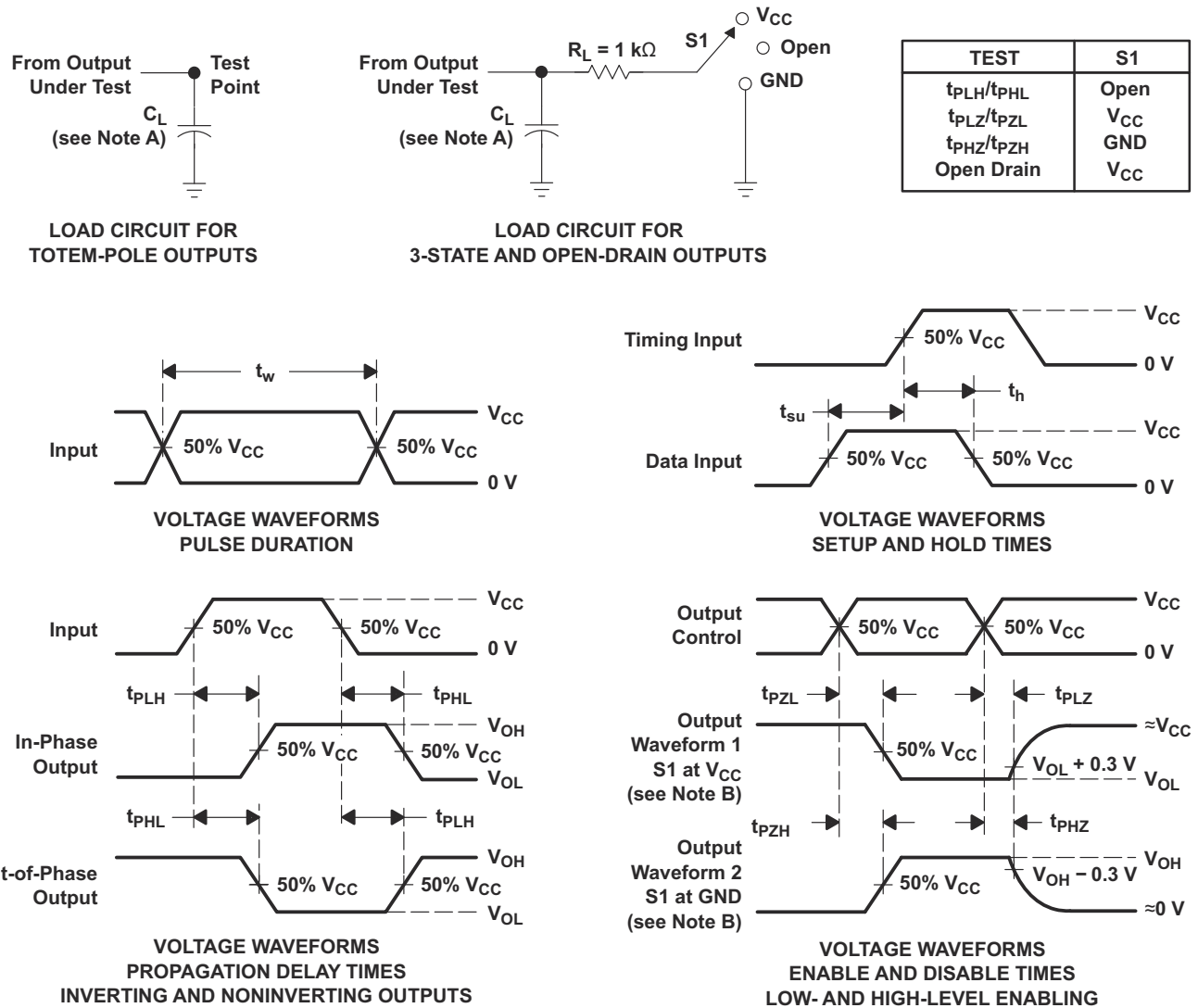
1. On products compliant to MIL-PRF-38535, this parameter is not production tested.
2. On products compliant to MIL-PRF-38535, this parameter does not apply.

5.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	$f = 10\text{ MHz}$	15.2	pF

6 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

Information at the data (D) inputs that meets the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

7.2 Functional Block Diagram

Figure 7-1. Logic Diagram (Positive Logic)

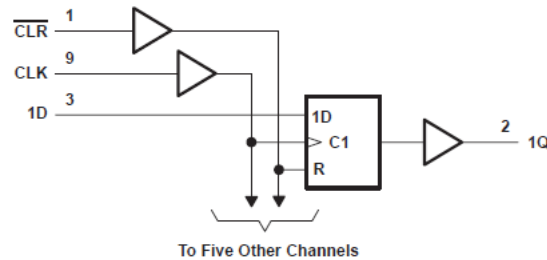


Figure 7-2.

7.3 Device Functional Modes

Table 7-1. Function Table

INPUTS ⁽¹⁾			OUTPUT
CLR	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Qo

(1) H = High Voltage Level, L = Low Voltage Level, X = Do not Care, Z = High Impedance

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

8.2 Layout

8.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

8.2.2 Layout Example

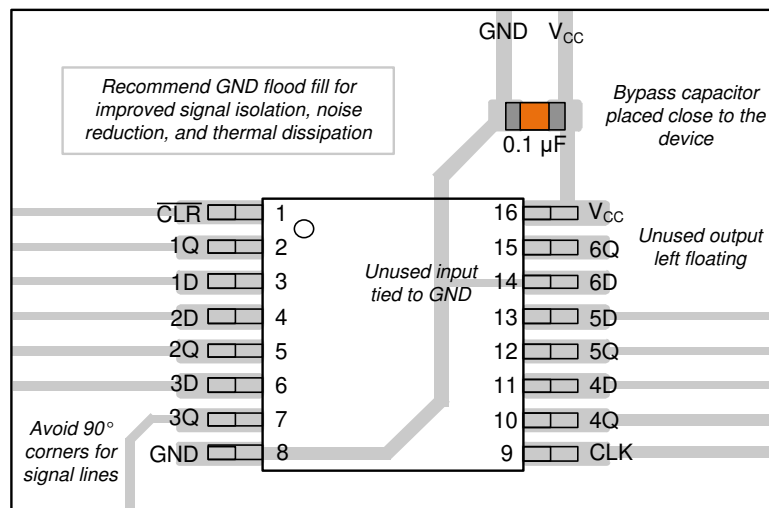


Figure 8-1. Layout Example of the

9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHC1G04-Q1	Click here	Click here	Click here	Click here	Click here

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (November 2023) to Revision H (July 2024)	Page
• Updated RθJA value: PW = 108 to 135.9, all values in °C/W	5

Changes from Revision F (June 1998) to Revision G (November 2023)	Page
• Added <i>Applications</i> section, <i>Package Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Device Functional Modes</i> , <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHC174D	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 85	AHC174
SN74AHC174DBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA174
SN74AHC174DBR.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA174
SN74AHC174DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC174
SN74AHC174DR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC174
SN74AHC174N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AHC174N
SN74AHC174N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AHC174N
SN74AHC174PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA174
SN74AHC174PWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA174

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC174DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC174DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHC174PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC174DBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74AHC174DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74AHC174PWR	TSSOP	PW	16	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AHC174N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC174N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC174N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC174N.A	N	PDIP	16	25	506	13.97	11230	4.32

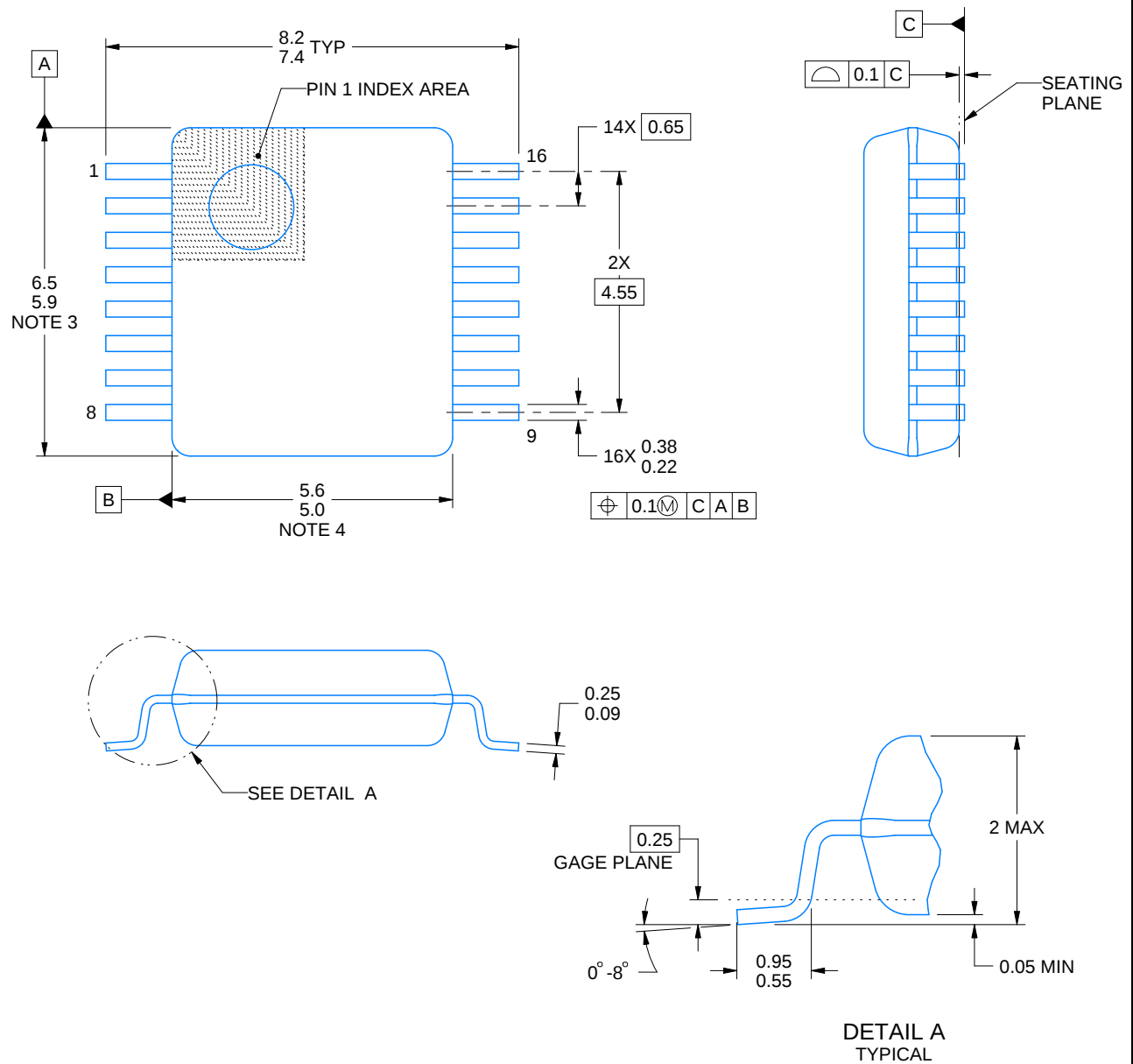
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



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NOTES:

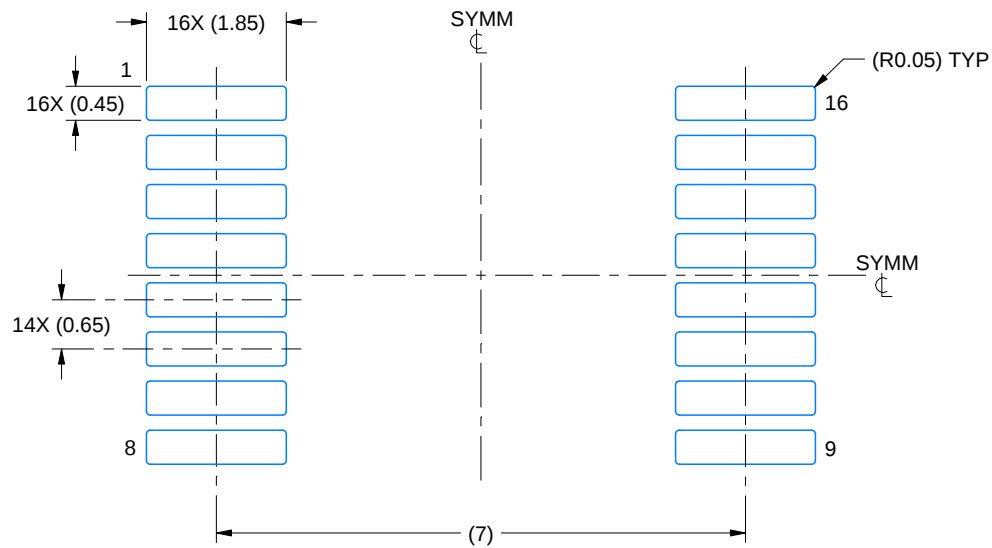
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

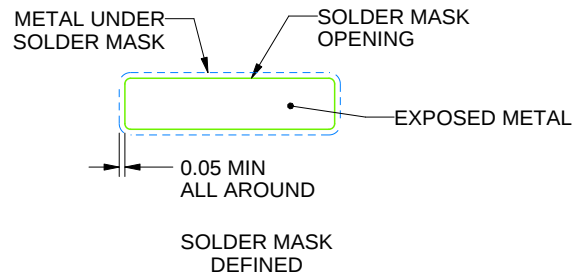
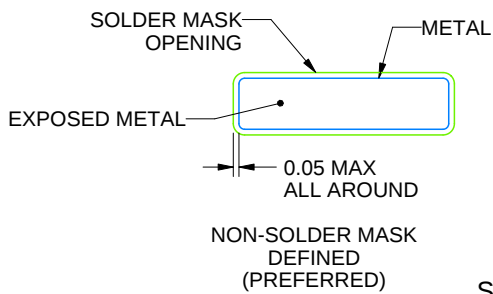
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

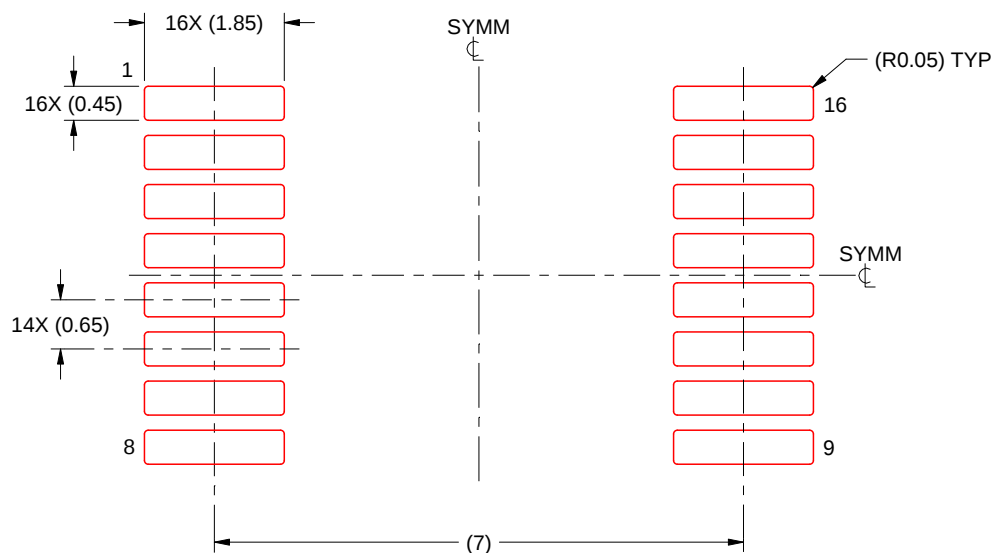
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

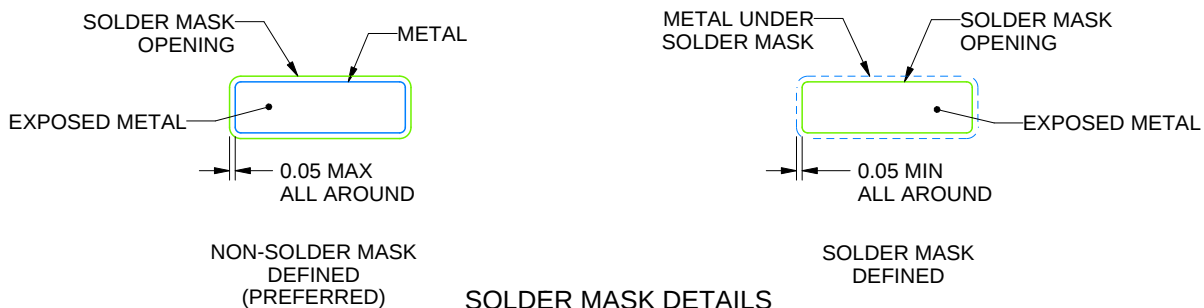
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

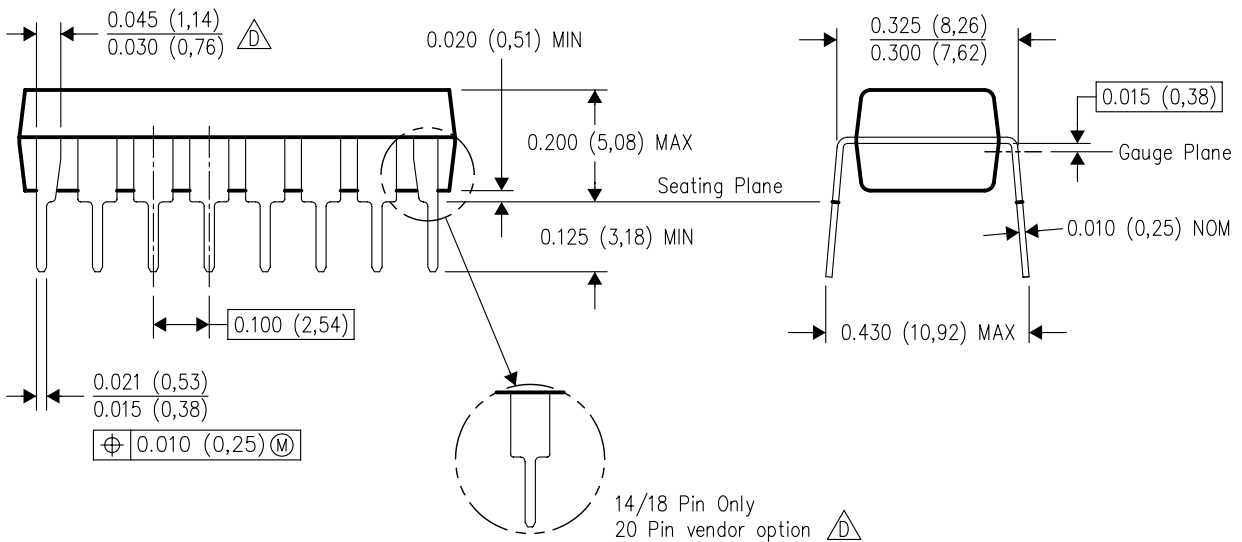
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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