

Electronic tuning PLL frequency synthesizer

BH2615S

The BH2615S is a PLL frequency synthesizer, featuring low radiation and low power consumption. It includes high sensitive RF amplifier and supports IF count function.

●Features

- 1) Low voltage operation (2.7V~)
- 2) High speed prescaler capable of direct dividing VCO (130MHz) frequency.
- 3) Low radiation (Xtal OSC 75kHz)
- 4) Low supply current (PLL ON:5mA, PLL OFF:300μA, Typ. V_{DD}=3.0V).
- 5) Reference frequency : 25, 12.5, 6.25, 3.125, 5, 3, 1kHz
- 6) On chip IF frequency counter.
- 7) Unlock detector
- 8) Output port : 7 ports (open drain output)
- 9) Data input : serial input (CE. CK. DA)

●Absolute maximum ratings (Ta = 25°C)

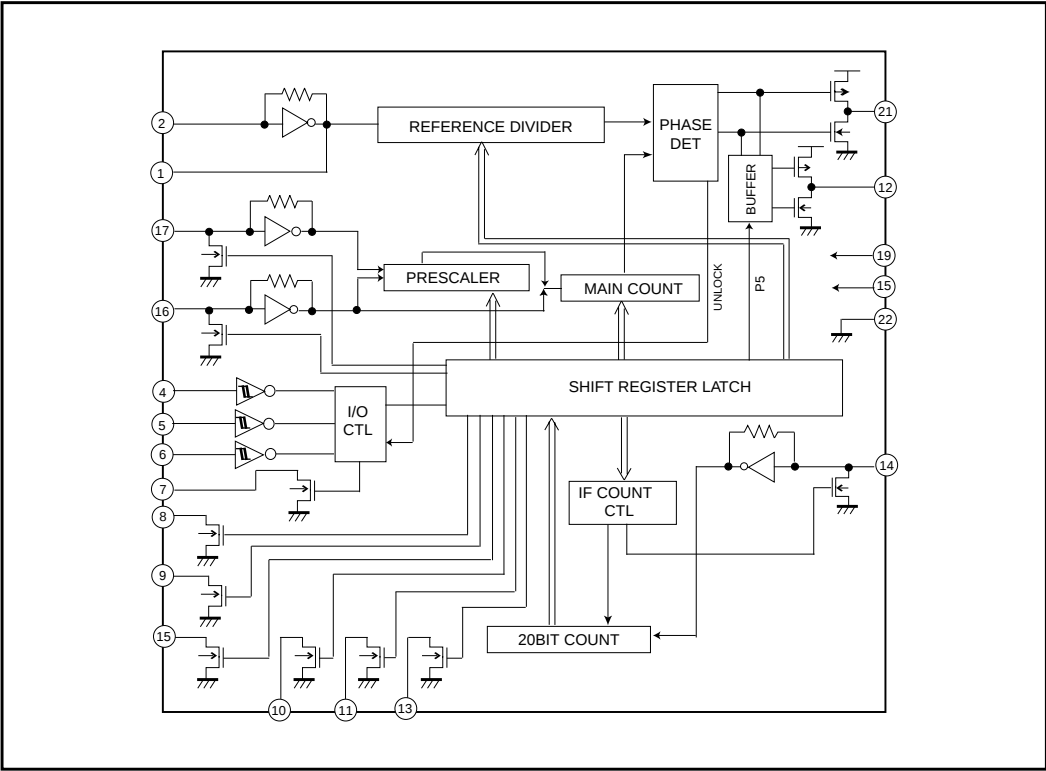
Parameter	Symbol	Limits	Unit	Condition
Maximum supply voltage	V _{DD}	-0.3~+7.0	V	V _{DD1} , V _{DD2}
Maximum input voltage 1	V _{IN1}	-0.3~+7.0	V	CE, CK, DA
Maximum input voltage 2	V _{IN2}	-0.3~V _{DD} +0.3	V	XIN, F _{MIN} , A _{MIN} , I _{FIN}
Maximum output voltage 1	V _{OUT1}	-0.3~10.0	V	P ₀ , P ₁ , P ₂ , P ₃ , P ₄ , P ₅ , CD
Maximum output voltage 2	V _{OUT2}	-0.3~V _{DD} +0.3	V	PD ₁ , PD ₂ , P ₅ , XOUT
Maximum output current	I _{OUT}	0~3.0	mA	P ₀ , P ₁ , P ₂ , P ₃ , P ₄ , P ₅ , CD
Allowable power dissipation	P _D	600 *	mW	
Operating temperature	T _{opr}	-10~+75	°C	
Storage temperature	T _{stg}	-55~+125	°C	

* Derating is done at 6.0mW /°C for operating above Ta=25°C.

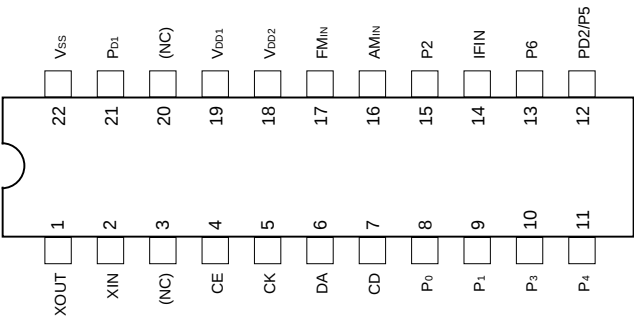
●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating supply voltage	V _{DD1} =V _{DD2}	2.7	—	3.6	V

●Block diagram



●Pin assigment



Audio ICs

●Pin descriptions

Pin No.	Pin Name	Symbol	Functions	I / O
1	Xtal OSC	XOUT	Crystal resonator (75kHz) is connected.	OUT
2		XIN		IN
3	Non contact	NC		
4	Chip enable	CE	"H" level are input during DA and CK. Data is synchronized this clock. Serial data transfered from controller.	IN
5	Clock	CK		
6	Serial data	DA		
7	Count data	CD	IF count data , unlock data output.	Nch open drain
8	Output port	P ₀	Controlled by input serial data.	
9		P ₁		
10		P ₃		
11		P ₄		
12		P ₅ / P _{D2}	*Selected input controlled data.	
13		P ₆		Nch open drain
14	IF input	IF _{IN}	IF frequency input.	IN
15	Output port	P ₂	Controlled by input serial data.	Nch open drain
16	AM input	AM _{IN}	Input AM local OSC.	IN
17	FM input	FM _{IN}	Input FM local OSC.	IN
18	Power supply2	V _{DD2}	Supply voltage 2.7~3.6V	
19	Power supply1	V _{DD1}	Supply voltage 2.7~3.6V	
20	Non contact	NC		
21	Charge pump	P _{D1}	If local OSC freq, divided by N is higher than reference freq, "H". lower, "L" and same, (Floating).	3-State
22	GROUND	V _{SS}		

Audio ICs

●Electrical characteristics (Unless otherwise specified, Ta = 25°C, V_{DD1} = V_{DD2} = 3.0V, V_{SS} = 0.0V)

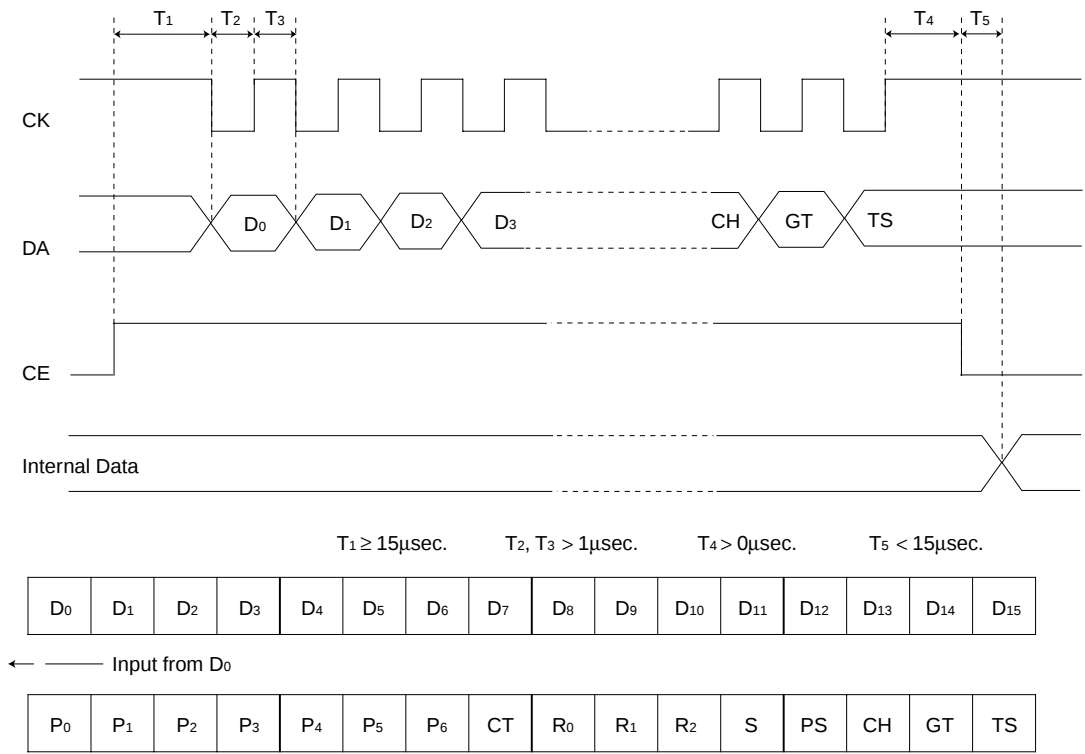
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply current 1	I _{DD1}	—	2.8	5.0	mA	F _{MIN} =130MHz, 50mVrms, V _{DD1} +V _{DD2} Current
Supply current 2	I _{DD2}	—	0.7	1.5	mA	A _{MIN} =1.0MHz, 50mVrms, V _{DD1} +V _{DD2} Current
Supply current 3	I _{DD3}	—	0.3	1.0	mA	PLL=OFF
Input "H" level voltage	V _{IH}	0.8V _{DD1}	—	—	—	CE,CK,DA Pins
Input "L" level voltage	V _{IL}	—	—	0.2V _{DD1}	—	CE,CK,DA Pins
Input "H" level current 1	I _{IH1}	—	—	1.0	μA	CE,CK,DA Pins, V _{IN} =V _{DD1}
Input "H" level current 2	I _{IH2}	—	0.3	0.7	μA	XIN Pin, V _{IN} =V _{DD1}
Input "H" level current 3	I _{IH3}	5	10	15	μA	F _{MIN} ,A _{MIN} Pins, V _{IN} =V _{DD2}
Input "H" level current 4	I _{IH4}	3	6	12	μA	I _{FIN} Pin, V _{IN} =V _{DD1}
Input "L" level current 1	I _{IL1}	−1.0	—	—	μA	CE,CK,DA Pins, V _{IN} =V _{SS}
Input "L" level current 2	I _{IL2}	−0.7	−0.3	—	μA	XIN Pin, V _{IN} =V _{SS}
Input "L" level current 3	I _{IL3}	−5	−10	−15	μA	F _{MIN} ,A _{MIN} ,I _{FIN} Pins, V _{IN} =V _{SS}
Output "L" level voltage 1	V _{OL1}	—	0.2	0.5	V	P ₀ ,P ₁ ,P ₂ ,P ₃ ,P ₄ ,P ₆ ,CD, I _O =1.0mA
Output "OFF" leak current 1	I _{OFF1}	—	—	1.0	μA	P ₀ ,P ₁ ,P ₂ ,P ₃ ,P ₄ ,P ₆ ,CD, V _O =10V
Output "L" level voltage 2	V _{OL2}	—	0.1	0.5	V	F _{MIN} ,A _{MIN} ,I _{FIN} , I _{OUT} =0.1mA
Output "H" level voltage	V _{OH}	V _{DD1} −1.0	V _{DD1} −0.3	—	V	P _{D1} ,P _{D2} ,P ₅ , I _{OUT} =−1.0mA
Output "L" level voltage	V _{OL}	—	0.2	1.0	V	P _{D1} ,P _{D2} ,P ₅ , I _{OUT} =1.0mA
Output "OFF" leak current 2	I _{OFF2}	—	—	100	nA	P _{D1} ,P _{D2} , V _{OUT} =V _{DD1}
Output "OFF" leak current 3	I _{OFF3}	−100	—	—	nA	P _{D1} ,P _{D2} , V _{OUT} =V _{SS}
On chip feedback resistance 1	R _{F1}	3.8	10	16	MΩ	XIN
On chip feedback resistance 2	R _{F2}	300	500	1000	kΩ	F _{MIN} ,A _{MIN} ,I _{FIN}
Input frequency input level 1	F _{IN1}	10 100	75	160 900	kHz mVrms	XIN,Sine Wave, C-Coupling
Input frequency input level 2	F _{IN2}	20 20	—	130 900	MHz mVrms	F _{MIN} ,Sine Wave, C-Coupling
Input frequency input level 3	F _{IN3}	0.4 20	—	5.0 900	MHz mVrms	A _{MIN} ,Sine Wave, C-Coupling
Input frequency input level 4	F _{IN4}	5.0 40	—	30 900	MHz mVrms	A _{MIN} ,Sine Wave, C-Coupling
Input frequency input level 5	F _{IN5}	0.4 20	—	16 900	MHz mVrms	I _{FIN} ,Sine Wave, C-Coupling
Minimum pulse width	TW	—	1.0	—	μs	CK,DA
Input rase time	TR	—	—	500	ns	CE,CK,DA
Input fall time	TF	—	—	500	ns	CE,CK,DA

© Not designed for radiation resistance.

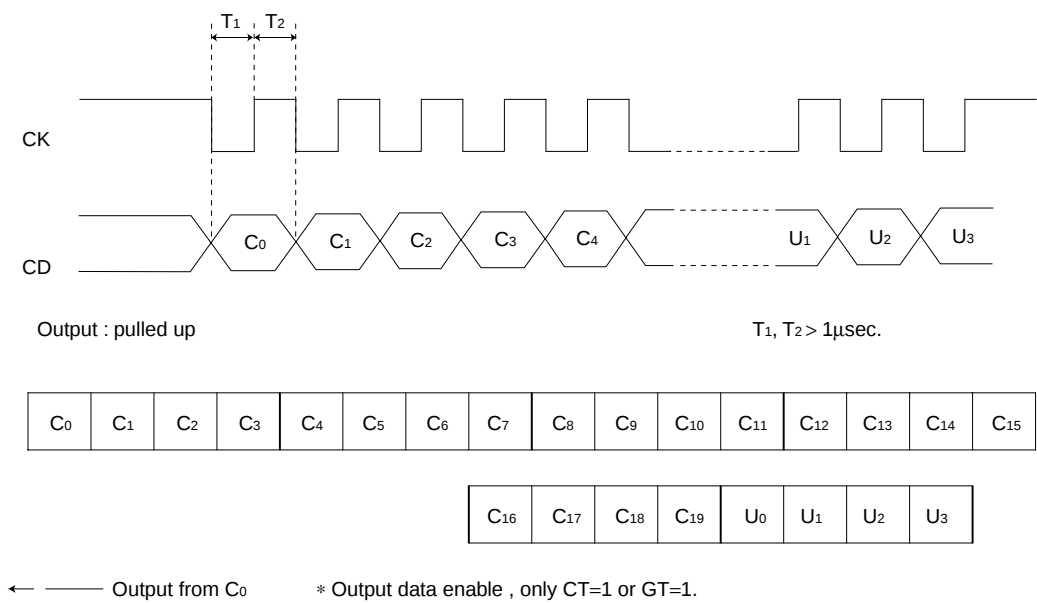
Audio ICs

●Circuit operation

Input data format



Output data format CE="L0" level



Audio ICs

Structure of control data

1) Division ratio data : D₀~D₁₅

D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D ₉	D ₁₀	D ₁₁	D ₁₂	D ₁₃	D ₁₄	D ₁₅
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Example :

Division = 1100 (D) = $1100 \div 2 = 550$ (D) = 226 (H)

S=0,PS=0

Division is twice the set point

0	1	1	0	0	1	0	0	0	1	0	0	0	0	0	0
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Division = 1107 (D) = 453 (H)

S=1,PS=1

1	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0
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Division = 926 (D) = 39E (H)

S=1,PS=0

x	x	x	x	0	1	1	1	1	0	0	1	1	1	0	0
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2) CT : IF counter on OFF

1 : START

0 : Counter is reset, IF_{IN} pulldown.3) Output port control data : P₀, P₁, P₂, P₃, P₄, P₅, P₆1 : Nch open drain output ON (P₅=L0)0 : Nch open drain output OFF (P₅=H1)4) R₀, R₁, R₂, Reference frequency data.

Data			
R ₀	R ₁	R ₂	Reference frequency
0	0	0	25kHz
0	0	1	12.5kHz
0	1	0	6.25kHz
0	1	1	5kHz
1	0	0	3.125kHz
1	0	1	3kHz
1	1	0	1kHz
1	1	1	* PLL OFF

*FM_{IN}=Pull down, AM_{IN}=Pull down, PD=Floating5) S : FM_{IN}, AM_{IN} select data0 : FM_{IN}1 : AM_{IN}

6) PS : Pre scaler ON with S=1

7) GT : IF count or unlock ON / OFF

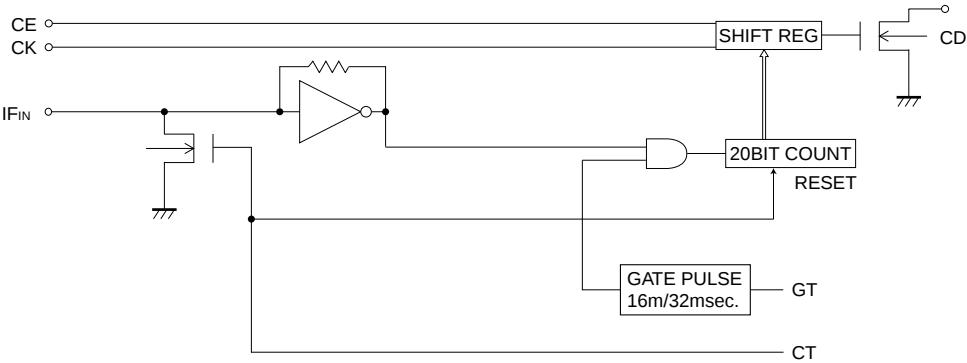
CT	GT	IF counter	Unlock detector	Output data
0	0	OFF	OFF	NG
0	1	OFF	ON	OK
1	0	ON Gate time=16msec.	ON	
1	1	ON Gate time=32msec.	ON	

8) TS : Test data input "0".

Audio ICs

IF counter

1) Composition



2) Operation of IF detection circuit

CT=1, IF counter start. CT = 0, IF count circuit reset.

GT=0, gate time=16msec. GT=1, gate time=32msec.

3) Output data

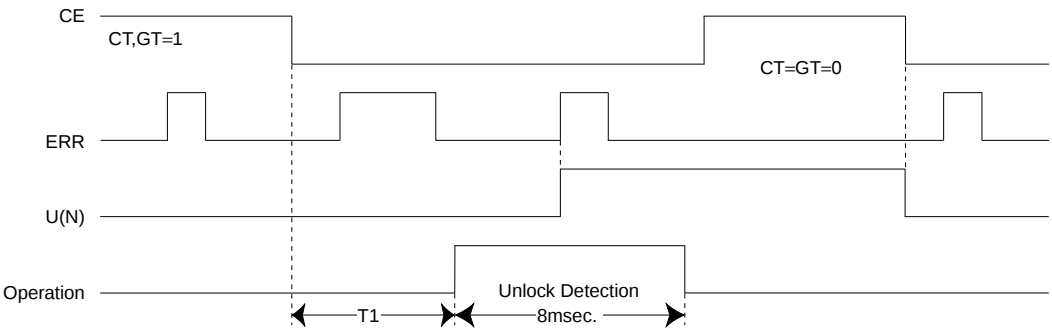
C₀ : LSB C₁₉ : MSB

Operation of unlock detector

GT=1 or CT=1, unlock detector start during 8msec.

CT=1, unlock detector start before gate pulse of IF counter.

CT=0 GT=0, IF counter and unlock detector.



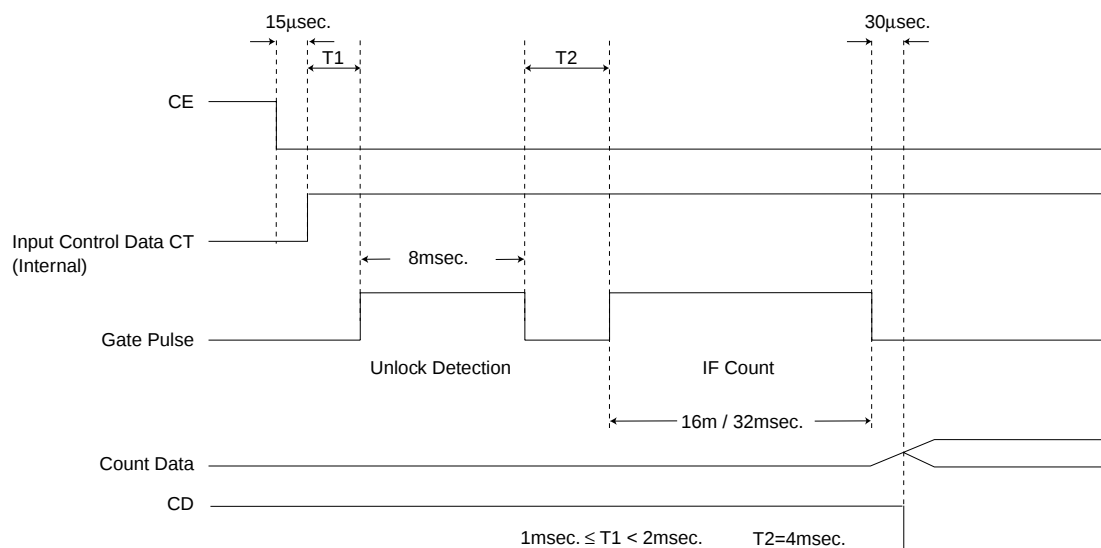
Structure output

U0	U1	U2	U3		ERR	
0	0	0	0			7μsec.
1	0	0	0	7μsec.	< ERR	< 13μsec.
1	1	0	0	13μsec.	< ERR	< 26μsec.
1	1	1	0	26μsec.	< ERR	< 54μsec.
1	1	1	1	54μsec.	< ERR	

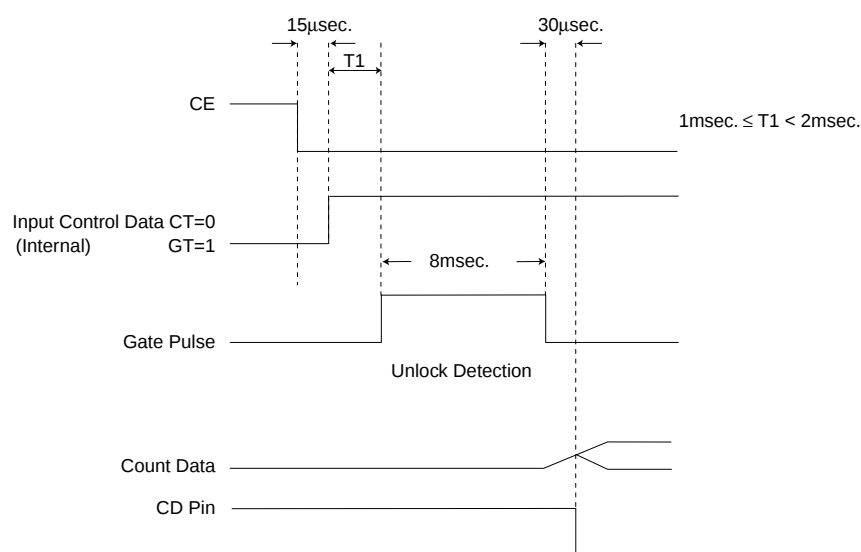
Audio ICs

Operation of IF counter and unlock detector.

1) CT=1 : IF count and unlock detector.



2) CT=0 GT=1 : unlock detection only.

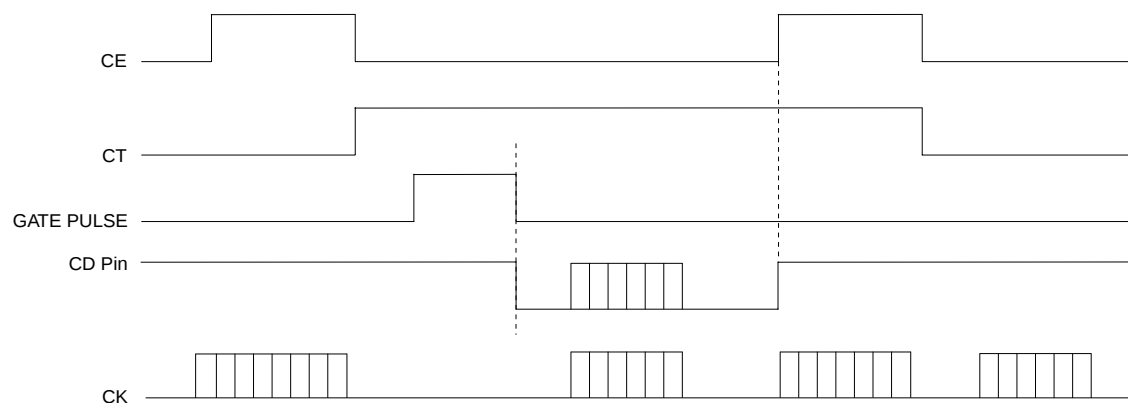


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Structure CD Pin

CD Pin becomes "L0" after finishing IF count or unlock detection operation.

Output data synchronized CK.



●External dimensions (Units : mm)

