BCM® Bus Converter

BCM48Bx120y120B00

Isolated Fixed Ratio DC-DC Converter

Features & Benefits

- $48V_{DC}$ – $12V_{DC}$ 120W Bus Converter
- High efficiency (>95%) reduces system power consumption
- High power density (801W/in³) reduces power system footprint by >50%
- "Half Chip" VI Chip® package enables surface mount, low impedance interconnect to system board
- Contains built-in protection features against:
  - Undervoltage
  - Overvoltage
  - Overcurrent
  - Short Circuit
  - Overtemperature
- Provides enable/disable control, internal temperature monitoring
- ZVS/ZCS Resonant Sine Amplitude Converter topology
- Less than 50°C temperature rise at full load in typical applications

Typical Application

- High End Computing Systems
- Automated Test Equipment
- Telecom Base Stations
- High Density Power Supplies
- Communication Systems

Product Ratings	
V_{IN} = 48V (38 – 55V)	P_{OUT} = up to 120W
V_{OUT} = 12V (9.5 – 13.75V) (NO LOAD)	K = 1/4

Description

The VI Chip® Bus Converter is a high efficiency (>95%) Sine Amplitude ConverterTM (SAC™) operating from a 38 to $55V_{DC}$ primary bus to deliver an isolated ratiometric output voltage from 9.5 to $13.75V_{DC}$. The SAC offers a low AC impedance beyond the bandwidth of most downstream regulators, meaning that input capacitance normally located at the input of a 12V regulator can be located at the input to the SAC. Since the K factor of the BCM48Bx120y120B00 is 1/4, that capacitance value can be reduced by a factor of 16x, resulting in savings of board area, materials and total system cost.

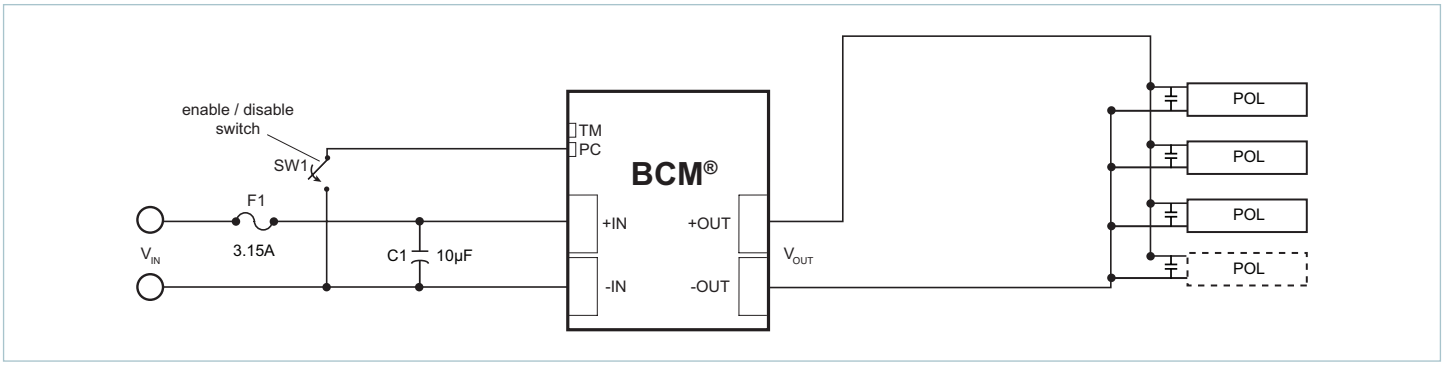
The BCM48BH120y120B00 is provided in a VI Chip package compatible with standard pick-and-place and surface mount assembly processes. The VI Chip package provides flexible thermal management through its low junction-to-case and junction-to-board thermal resistance. With high conversion efficiency the BCM48Bx120y120B00 increases overall system efficiency and lowers operating costs compared to conventional approaches.

Part Numbering

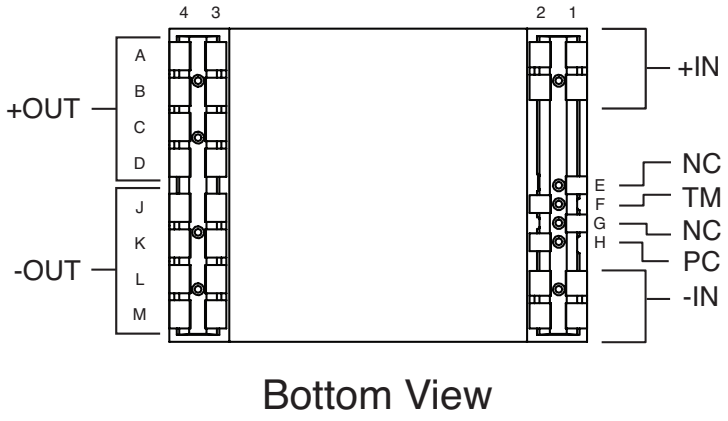
Product Number	Package Style (x)	Product Grade (y)
BCM48Bx120y120B00	**H** = J-Lead	**T** = -40° to 125°C
		M = -55° to 125°C

For Storage and Operating Temperatures see Section 6.0 General Characteristics

Typical Application



Pin Configuration



Pin Descriptions

Pin Number	Signal Name	Type	Function
A1-B1, A2-B2	+IN	INPUT POWER	Positive input power terminal
L1-M1, L2-M2	–IN	INPUT POWER RETURN	Negative input power terminal
E1	NC	NC	No connect
F2	TM	OUTPUT	Temperature monitor, input side referenced signal
G1	NC	NC	No connect
H2	PC	OUTPUT/INPUT	Enable and disable control, input side referenced signal
A3-D3, A4-D4	+OUT	OUTPUT POWER	Positive output power terminal
J3-M3, J4-M4	–OUT	OUTPUT POWER RETURN	Negative output power terminal

Control Pin Specifications

See Using the Control Signals PC, TM for more information.

PC (BCM Primary Control)

The PC pin can enable and disable the BCM module. When held below V_{PC_DIS} the BCM shall be disabled. When allowed to float with an impedance to –IN of greater than 60kΩ the module will start. When connected to another BCM PC pin (either directly, or isolated through a diode), the BCM modules will start simultaneously when enabled. The PC pin is capable of being either driven high by an external logic signal or internal pull up to 5V (operating).

TM (BCM Temperature Monitor)

The TM pin monitors the internal temperature of the BCM module within an accuracy of ±5°C. It has a room temperature setpoint of ~3.0V and an approximate gain of 10mV/°C. It can source up to 100µA and may also be used as a "Power Good" flag to verify that the BCM module is operating.

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
+IN to –IN		-1	60	V
V_{IN} slew rate	Operational	-1	1	V/µs
Isolation voltage, input to ouput			2250	V
+OUT to –OUT		-1	16	V
Output current transient	≤ 10ms, ≤ 10% DC	-3	14.2	A
Output current average		-2	10	A
PC to –IN		-0.3	20	V
TM to –IN		-0.3	7	V

Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_J ≤ 125°C (T-Grade); all other specifications are at T_J = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain						
Voltage range	V_{IN_DC}		**38**	**48**	**55**	V
dV / dt	dV_{IN} / dt				**1**	V/µs
Quiescent power	P_Q	PC connected to –IN		68	**150**	mW
No load power dissipation	P_{NL}	V_{IN} = 48V		2.1	**4.1**	W
		V_{IN} = 38V to 55V			**5**	
Inrush current peak	I_{INR_P}	V_{IN} = 48V, C_{OUT} = 500µF, I_{OUT} = 10.55A		5.5	**12**	A
DC input current	I_{IN_DC}	At P_{OUT} = 240W			**3.5**	A
Transformation ratio	K	K = V_{OUT} / V_{IN}, at no load		1/4		V/V
Output power (average)	P_{OUT_AVG}	V_{IN} = 38 - 55V_{DC}			**97**	W
		V_{IN} = 46 - 55V_{DC}			**120**	
Output power (peak)	P_{OUT_PK}	V_{IN} = 46 - 55V_{DC} , 10ms max, P_{OUT_AVG} ≤ 120W			**150**	W
Output voltage	V_{OUT}		**8.5**		**14**	V
Output current (average)	I_{OUT_AVG}	P_{OUT_AVG} ≤ 120W			**10**	A
Efficiency (ambient)	η_{AMB}	V_{IN} = 48V, P_{OUT} = 120W	93.5	94.6		%
		V_{IN} = 38V to 55V, P_{OUT} = 100W	92.0			
Efficiency (hot)	η_{HOT}	V_{IN} = 48V, P_{OUT} = 120W; T_J = 100°C	92.6	93.5		%
Efficiency (over load range)	$\eta_{20\%}$	24W < P_{OUT} < P_{OUT} Max	**72.0**			%
Output resistance	R_{OUT_COLD}	P_{OUT} = 120W, T_{CASE} = -40°C	20.0	28.7	40.0	mΩ
	R_{OUT_AMB}	P_{OUT} = 120W, T_{CASE} = 25°C	25.0	38.8	50.0	
	R_{OUT_HOT}	P_{OUT} = 120W, T_{CASE} = 100°C	30.0	47.3	60.0	
Load capacitance	C_{OUT}				**500**	µF
Switching frequency	F_{SW}		**1.4**	1.5	**1.6**	MHz
Output voltage ripple	V_{OUT_PP}	C_{OUT} = 0µF, I_{OUT} = 10.55A, V_{IN} = 48V,		200	**400**	mV
V_{IN} to V_{OUT} (application of V_{IN})	T_{ON1}	V_{IN} = 48V, C_{PC} = 0		570	800	ms

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_J ≤ 125°C (T-Grade); all other specifications are at T_J = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Protection						
Input overvoltage lockout threshold	V_{IN_OVLO+}		**55.5**	58.1	**60**	V
Input overvoltage recovery threshold	V_{IN_OVLO-}		**55.1**	58.7	**60**	V
Input undervoltage recovery threshold	V_{IN_UVLO+}		**30.7**	32.9	**37.3**	V
Input undervoltage lockout threshold	V_{IN_UVLO-}		**29.1**	31.5	**35.4**	V
Output overcurrent trip threshold	I_{OCP}	V_{IN} = 48V, 25°C	**12**	17	**24**	A
Short circuit protection trip threshold	I_{SCP}		**24**		40	A
Short circuit protection response time	T_{SCP}		**0.8**	1.0	**1.2**	µs
Thermal shutdown threshold	T_{J_OTP}		**125**	130	135	°C

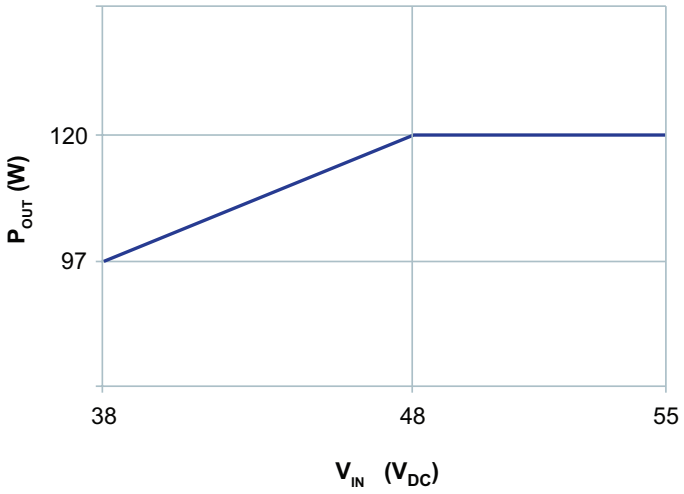


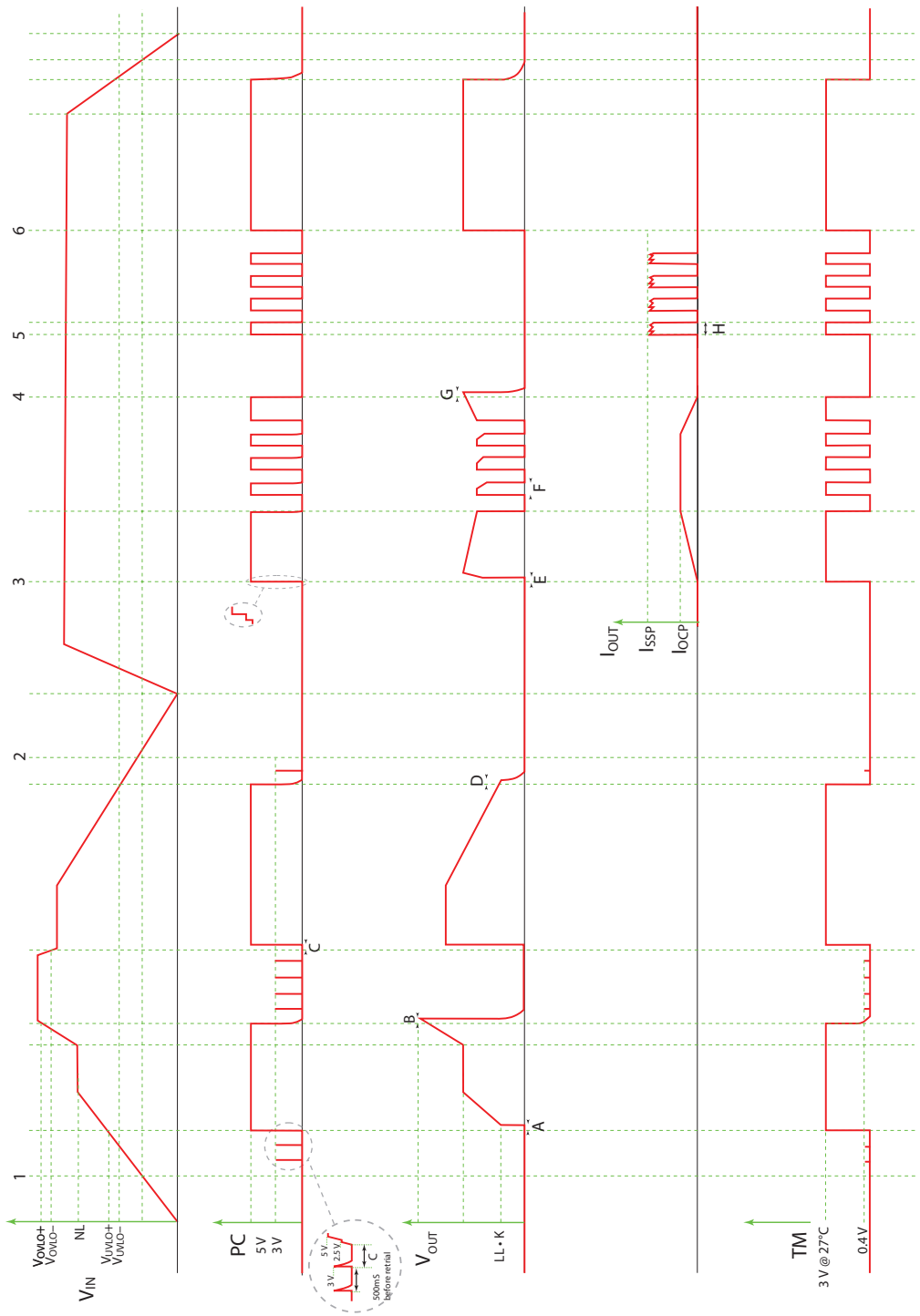
Figure 1 — *P_{OUT} derating vs V_{IN}*

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_J ≤ 125°C (T-Grade); all other specifications are at T_J = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
PC						
PC voltage (operating)	V_{PC}		**4.7**	5.0	**5.3**	V
PC voltage (enable)	V_{PC_EN}		**2.0**	2.5	**3.0**	V
PC voltage (disable)	V_{PC_DIS}				**1.95**	V
PC source current (start up)	I_{PC_EN}		**50**	100	**300**	µA
PC source current (operating)	I_{PC_OP}				**2**	mA
PC internal resistance	R_{PC_SNK}	Internal pull down resistor	**50**	150	**400**	kΩ
PC capacitance (internal)	C_{PC_INT}				**588**	pF
PC capacitance (external)	C_{PC_EXT}	External capacitance delays PC enable time			**1000**	pF
External PC resistance	R_{PC}	Connected to $-V_{IN}$	**60**			kΩ
PC external toggle rate	R_{PC_TOG}				**1**	Hz
PC to V_{OUT} with PC released	T_{ON2}	V_{IN} = 48V, pre-applied		60	**100**	µs
PC to V_{OUT}, disable PC	T_{PC_DIS}	V_{IN} = 48V, pre-applied		4	**10**	µs
TM						
TM accuracy	AC_{TM}		**-5**		**+5**	°C
TM gain	A_{TM}			10		mV / °C
TM source current	I_{TM}				**100**	µA
TM internal resistance	R_{TM_SNK}		**25**	40	**50**	kΩ
External TM capacitance	C_{TM}				**50**	pF
TM voltage ripple	V_{TM_PP}	C_{TM} = 0µF, V_{IN} = 55V, P_{OUT} = 120W	**75**	180	**250**	mV

Timing Diagram



Notes:
– Timing and voltage is not to scale
– Error pulse width is load dependent

A: T_{ON1}
B: T_{OVLO}*
C: Max recovery time
D: T_{UVLO}
E: T_{ON2}
F: T_{OCP}
G: T_{PC-DIS}
H: T_{SSP}**

1: Controller start
2: Controller turn off
3: PC release
4: PC pulled low
5: PC released on output SC
6: SC removed

*Min value switching off
**From detection of error to power train shutdown

Application Characteristics

All specifications are at T_J = 25ºC unless otherwise noted. See associated figures for general trend data

Attribute	Symbol	Conditions / Notes	Typ	Unit
No load power	P_{NL}	V_{IN} = 48V, PC enabled	1.75	W
Inrush current peak	I_{NR_P}	C_{OUT} = 500µF, P_{OUT} = 120W	6	A
Efficiency (ambient)	η	V_{IN} = 48V, P_{OUT} = 120W, C_{OUT} = 500µF	95	%
Efficiency (hot – 100ºC)	η	V_{IN} = 48V, P_{OUT} = 120W, C_{OUT} = 500µF	94	%
Output resistance (-40ºC)	R_{OUT_C}	V_{IN} = 48V	35	mΩ
Output resistance (25ºC)	R_{OUT_R}	V_{IN} = 48V	44	mΩ
Output resistance (100ºC)	R_{OUT_H}	V_{IN} = 48V	56	mΩ
Output voltage ripple	V_{OUT_PP}	C_{OUT} = 0µF, P_{OUT} = 120W @ V_{IN} = 48V, V_{IN} = 48V	160	mV
V_{OUT} transient voltage (positive)	V_{OUT_TRAN+}	I_{OUT_STEP} = 0 – 10.55A, I_{SLEW} > 10A/µs	1.4	V
V_{OUT} transient voltage (negative)	V_{OUT_TRAN-}	I_{OUT_STEP} = 10.55 – 0A, I_{SLEW} > 10A/µs	1.3	V
Undervoltage lockout response time	T_{UVLO}		2.4	µs
Output overcurrent response time	T_{OCP}	12 < I_{OCP} < 25A	4.4	ms
Overvoltage lockout response time	T_{OVLO}		2.4	µs

Application Characteristics

The following values, typical of an application environment, are collected at T_{CASE} = 25°C unless otherwise noted. See associated figures for general trend data.

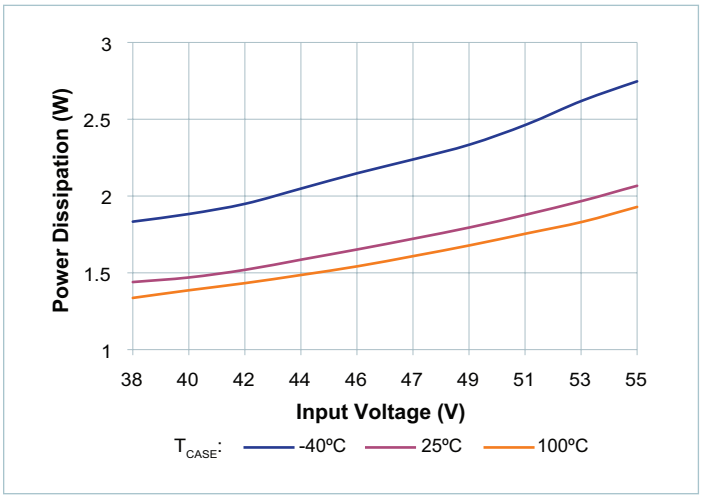


Figure 2 — *No load power dissipation vs. V_{IN}*

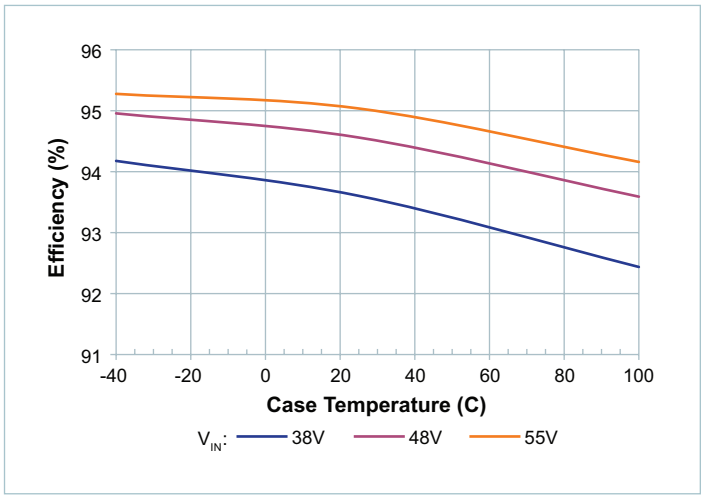


Figure 3 — *Full load efficiency vs. temperature; V_{IN}*

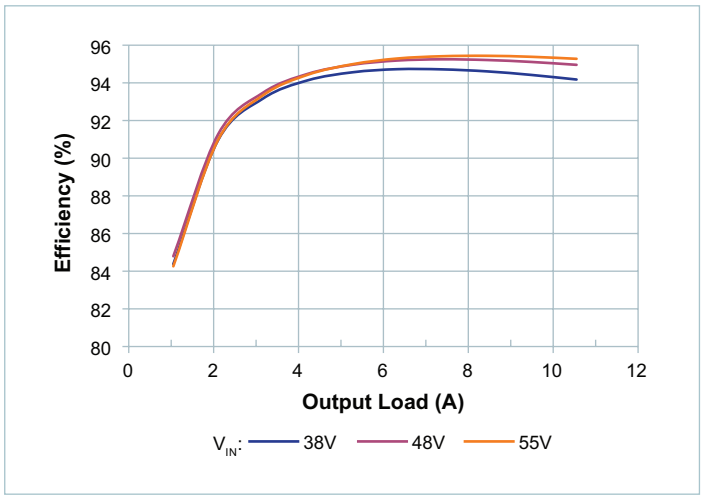


Figure 4 — *Efficiency at T_{CASE} = -40°C*

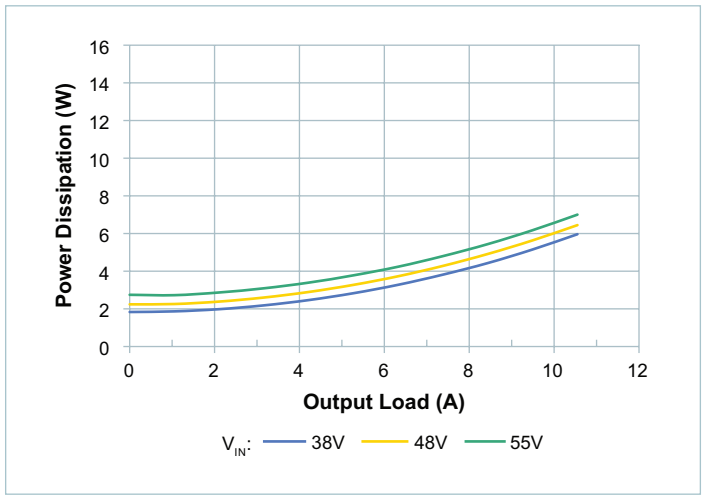


Figure 5 — *Power dissipation at T_{CASE} = -40°C*

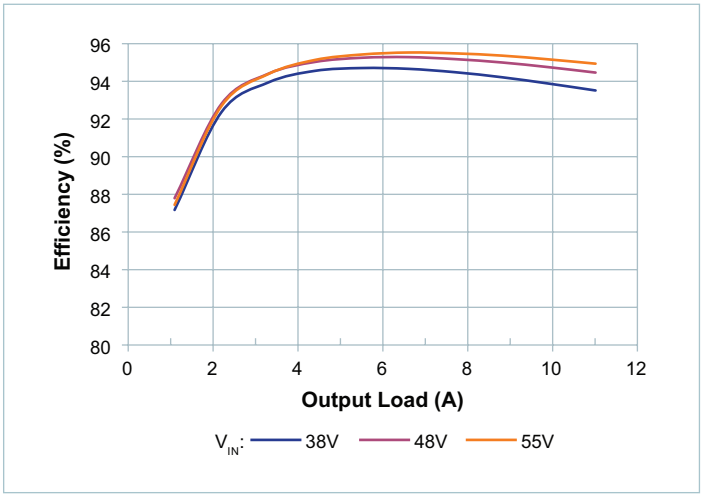


Figure 6 — *Efficiency at T_{CASE} = 25°C*

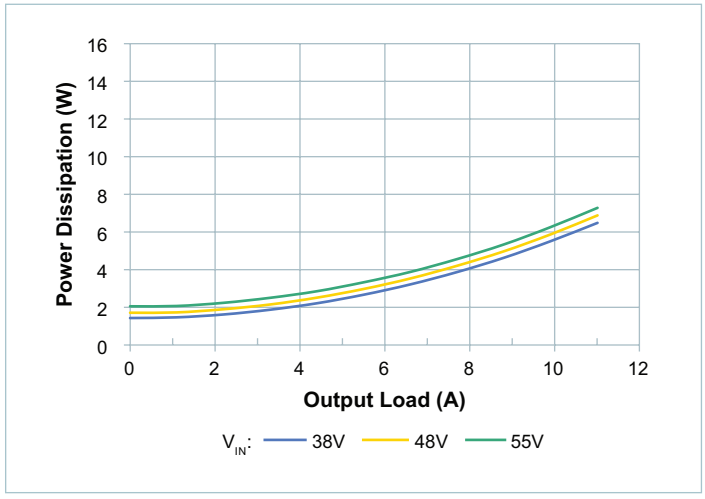


Figure 7 — *Power dissipation at T_{CASE} = 25°C*

Application Characteristics (Cont.)

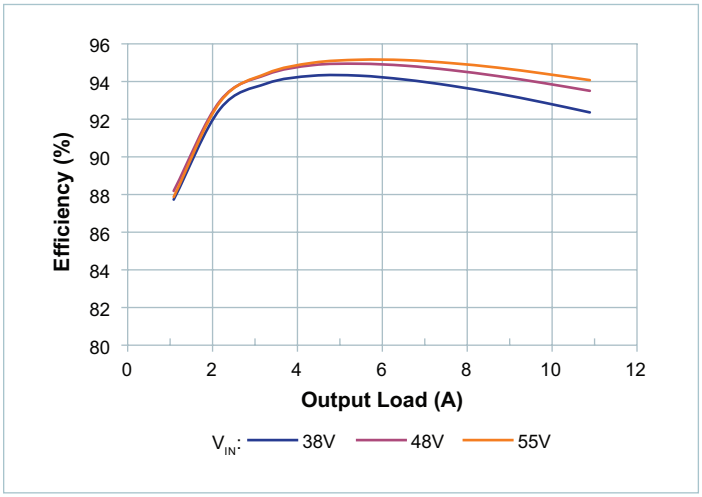


Figure 8 — *Efficiency at T_{CASE} = 100°C*

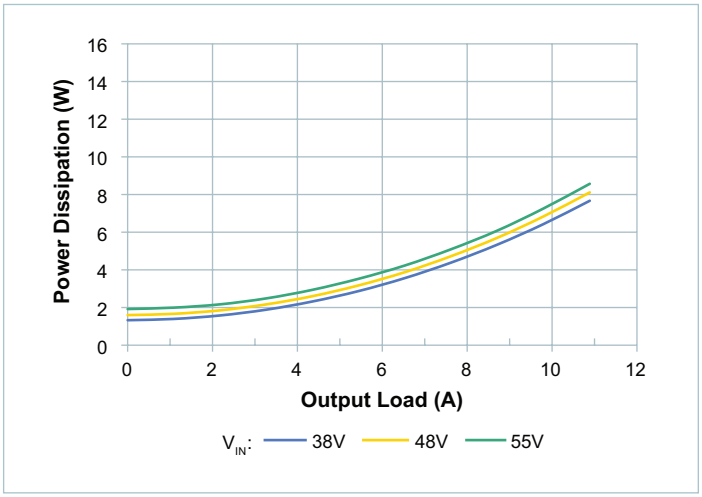


Figure 9 — *Power dissipation at T_{CASE} = 100°C*

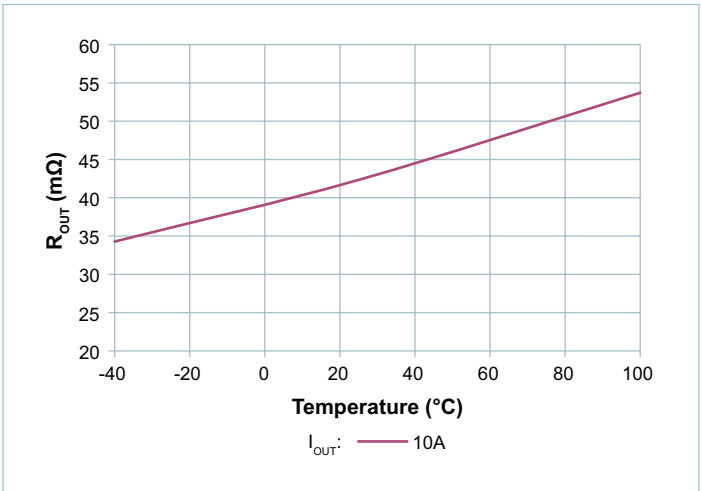


Figure 10 — *R_{OUT} vs. temperature; nominal input*

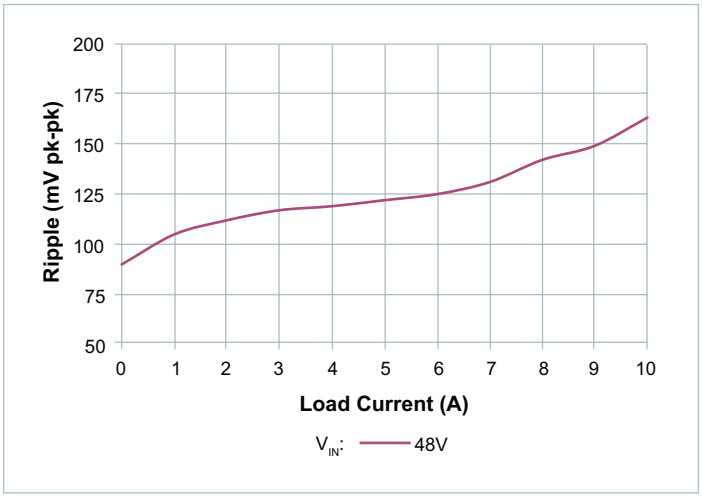


Figure 11 — *V_{RIPPLE} vs. I_{OUT}: No external C_{OUT}, board mounted module, scope setting : 20MHz analog BW*

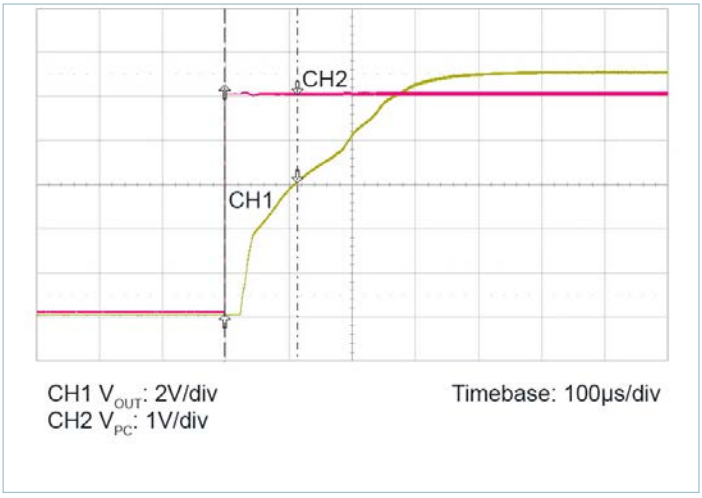


Figure 12 — *PC to V_{OUT} start up wave form*

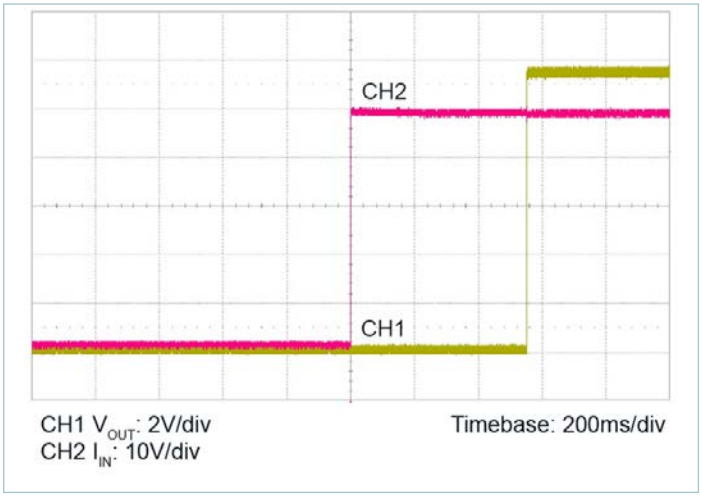


Figure 13 — *V_{IN} to V_{OUT} start up wave form*

Application Characteristics (Cont.)

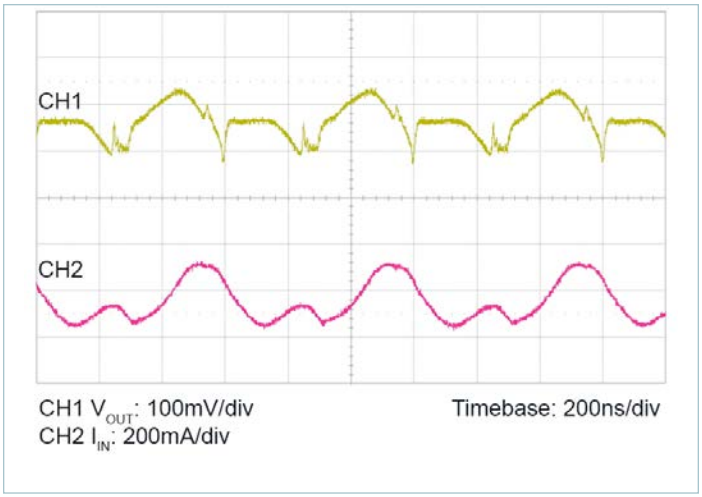


Figure 14 — *Output voltage and input current ripple; V_{IN} = 48V, 120W, no C_{OUT}*

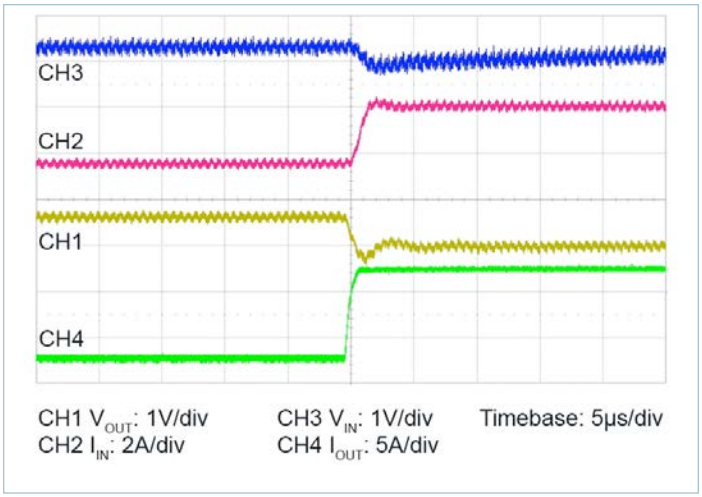


Figure 15 — *0A – 11.3A transient response: C_{IN} = 330µF, I_{IN} measured prior to C_{IN}, no external C_{OUT}*

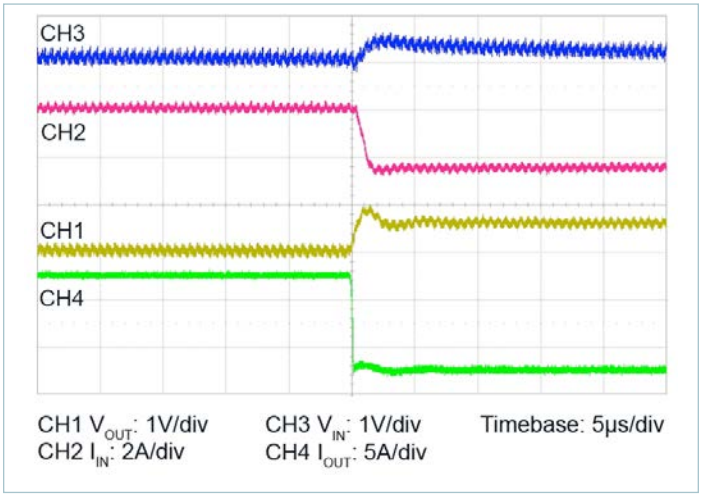


Figure 16 — *11.3A – 0A transient response: C_{IN} = 330µF, I_{IN} measured prior to C_{IN}, no external C_{OUT}*

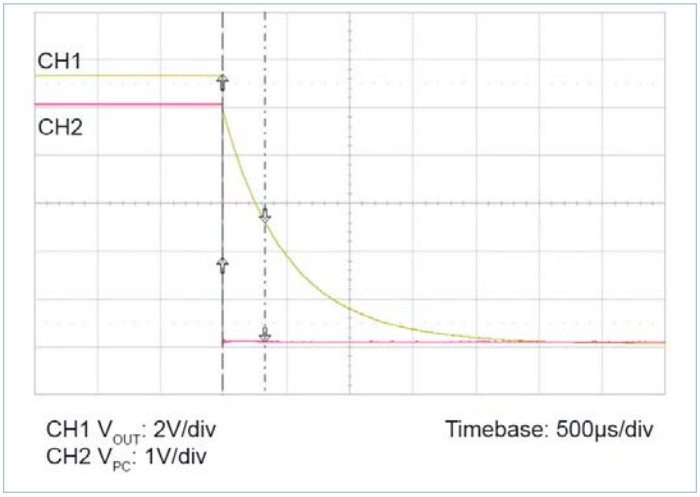


Figure 17 — *PC disable wave form; V_{IN} = 48V, C_{OUT} = 500µF, full load*

General Characteristics

All specifications are at T_J = 25°C unless otherwise noted. See associated figures for general trend data.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L		21.7 / [0.854]	22.0 / [0.866]	22.3 / [0.878]	mm / [in]
Width	W		16.37 / [0.644]	16.50 / [0.650]	16.63 / [0.655]	mm / [in]
Height	H		6.48 / [0.255]	6.73 / [0.265]	6.98 / [0.275]	mm / [in]
Volume	Vol	No heat sink		2.44 / [0.150]		cm^3/ [in^3]
Footprint	F	No heat sink		3.6 / [0.56]		cm^3/ [in^3]
Power density	P_D	No heat sink		801		W/in^3
				49		W/cm^3
Weight	W			8 / [0.28]		g / [oz]
Lead Finish		Nickel	0.51		2.03	µm
		Palladium	0.02		0.15	
		Gold	0.003		0.051	
Thermal						
Operating temperature	T_J		-40		125	°C
Storage temperature	T_{ST}		-40		125	°C
Thermal impedance	$ø_{JC}$	Junction to case			2.7	°C/W
Thermal capacity				5		Ws/°C
Assembly						
Peak compressive force applied to case (Z-axis)		Supported by J-lead only		2.5	3.0	lbs
ESD Withstand	ESD_{HBM}	Human Body Model, JEDEC JESD 22-A114C.01	1500			V_{DC}
	ESD_{MM}	Machine Model, JEDEC JESD 22-A115-A	400			
Soldering						
Peak temperature during reflow		MSL 4 (Datecode 1528 and later)			245	°C
Peak time above 217°C					150	s
Peak heating rate during reflow				1.5	3	°C/s
Peak cooling rate post reflow				1.5	6	°C/s
Safety						
Working voltage (IN – OUT)	V_{IN_OUT}				**60**	V_{DC}
Isolation voltage (hipot)	V_{HIPOT}		**2250**			V_{DC}
Isolation capacitance	C_{IN_OUT}	Unpowered unit	**1350**	**1750**	**2150**	pF
Isolation resistance	R_{IN_OUT}		**10**			MΩ
MTBF		MIL-HDBK-217Plus Parts Count - 25°C Ground Benign		7.1		MHrs
Agency approvals / standards		cTUVus				
		cURus				
		CE Marked for Low Voltage Directive and ROHS recast directive, as applicable.				

Using the Control Signals PC, TM

Primary Control (PC) pin can be used to accomplish the following functions:

- *Delayed start:* At start up, PC pin will source a constant 100µA current to the internal RC network. Adding an external capacitor will allow further delay in reaching the 2.5V threshold for module start.
- *Synchronized start up:* In an array of parallel modules, PC pins should be connected to synchronize start up across units. While every controller has a calibrated 2.5V reference on PC comparator, many factors might cause different timing in turning on the 100µA current source on each module, i.e.:

  – Different V_{IN} slew rate
  – Statistical component value distribution

  By connecting all PC pins, the charging transient will be shared and all the modules will be enabled synchronously.
- *Auxiliary voltage source:* Once enabled in regular operational conditions (no fault), each BCM module PC provides a regulated 5V, 2mA voltage source.
- *Output disable:* PC pin can be actively pulled down in order to disable the module. Pull down impedance shall be lower than 1kΩ and toggle rate lower than 1Hz.
- *Fault detection flag:* The PC 5V voltage source is internally turned off as soon as a fault is detected. After a minimum disable time, the module tries to re-start, and PC voltage is re-enabled. For system monitoring purposes (microcontroller interface) faults are detected on falling edges of PC signal.
- Note that PC doesn't have current sink capability (only 150kΩ typical pull down is present), therefore, in an array, PC line will not be capable of disabling all the modules if a fault occurs on one of them.

Temperature Monitor (TM) pin provides a voltage proportional to the absolute temperature of the converter control IC.

It can be used to accomplish the following functions:

- *Monitor the control IC temperature:* The temperature in Kelvin is equal to the voltage on the TM pin scaled by 100. (i.e. 3.0V = 300K = 27°C). It is important to remember that VI Chip® products are multi-chip modules, whose temperature distribution greatly vary for each part number as well with input/output conditions, thermal management and environmental conditions. Therefore, TM cannot be used to thermally protect the system.
- *Fault detection flag:* The TM voltage source is internally turned off as soon as a fault is detected. After a minimum disable time, the module tries to re-start, and TM voltage is re-enabled.

Sine Amplitude Converter™ Point of Load Conversion

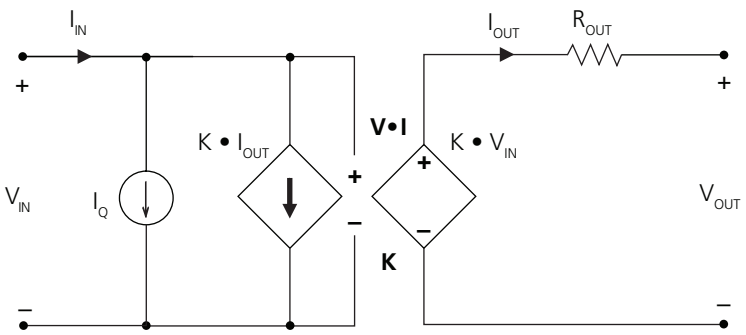


Figure 18 — *VI Chip® module DC model*

The Sine Amplitude Converter (SAC™) uses a high frequency resonant tank to move energy from input to output. The resonant LC tank, operated at high frequency, is amplitude modulated as a function of input voltage and output current. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieving power density.

The BCM48Bx120y120B00 SAC can be simplified into the preceeding model.

At no load:

$$V_{OUT} = V_{IN} \bullet K \qquad (1)$$

K represents the "turns ratio" of the SAC.
Rearranging Eq (1):

$$K = \frac{V_{OUT}}{V_{IN}} \qquad (2)$$

In the presence of load, V_{OUT} is represented by:

$$V_{OUT} = V_{IN} \bullet K - I_{OUT} \bullet R_{OUT} \qquad (3)$$

and I_{OUT} is represented by:

$$I_{OUT} = \frac{I_{IN} - I_Q}{K} \qquad (4)$$

R_{OUT} represents the impedance of the SAC, and is a function of the R_{DSON} of the input and output MOSFETs and the winding resistance of the power transformer. I_Q represents the quiescent current of the SAC control, gate drive circuitry, and core losses.

The use of DC voltage transformation provides additional interesting attributes. Assuming that $R_{OUT} = 0\Omega$ and $I_Q = 0A$, Eq. (3) now becomes Eq. (1) and is essentially load independent, resistor R is now placed in series with V_{IN}.

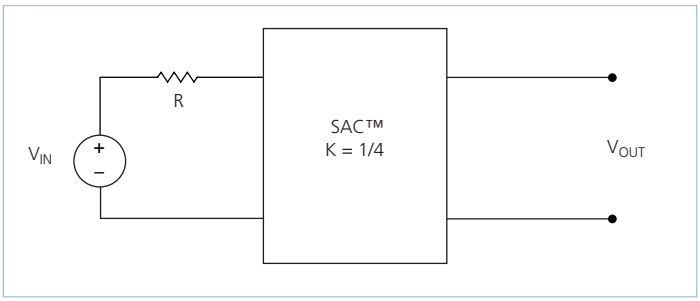


Figure 19 — *K = 1/4 Sine Amplitude Converter with series input resistor*

The relationship between V_{IN} and V_{OUT} becomes:

$$V_{OUT} = (V_{IN} - I_{IN} \bullet R) \bullet K \qquad (5)$$

Substituting the simplified version of Eq. (4) (I_Q is assumed = 0A) into Eq. (5) yields:

$$V_{OUT} = V_{IN} \bullet K - I_{OUT} \bullet R \bullet K^2 \qquad (6)$$

This is similar in form to Eq. (3), where R_{OUT} is used to represent the characteristic impedance of the SAC™. However, in this case a real R on the input side of the SAC is effectively scaled by K^2 with respect to the output.

Assuming that R = 1Ω, the effective R as seen from the secondary side is 62.5mΩ, with K = 1/4.

A similar exercise should be performed with the additon of a capacitor or shunt impedance at the input to the SAC. A switch in series with V_{IN} is added to the circuit. This is depicted in Figure 20.

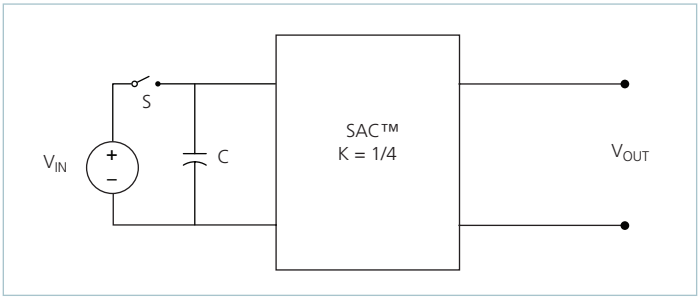


Figure 20 — *Sine Amplitude Converter™ with input capacitor*

A change in V_{IN} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C \frac{dV_{IN}}{dt} \quad (7)$$

Assume that with the capacitor charged to V_{IN}, the switch is opened and the capacitor is discharged through the idealized SAC. In this case,

$$I_C = I_{OUT} \bullet K \quad (8)$$

substituting Eq. (1) and (8) into Eq. (7) reveals:

$$I_{OUT} = \frac{C}{K^2} \bullet \frac{dV_{OUT}}{dt} \quad (9)$$

The equation in terms of the output has yielded a K^2 scaling factor for C, specified in the denominator of the equation.
A K factor less than unity results in an effectively larger capacitance on the output when expressed in terms of the input. With a K = 1/4 as shown in Figure 20, C = 1µF would appear as C = 16µF when viewed from the output.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a SAC between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, the benefits are not useful if the series impedance of the SAC is too high. The impedance of the SAC must be low, i.e. well beyond the crossover frequency of the system.

A solution for keeping the impedance of the SAC low involves switching at a high frequency. This enables small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the BCM module are:

- No load power dissipation (P_{NL}): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss ($P_{R_{OUT}}$): refers to the power loss across the BCM module modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{NL} + P_{R_{OUT}} \quad (10)$$

Therefore,

$$P_{OUT} = P_{IN} - P_{DISSIPATED} = P_{IN} - P_{NL} - P_{R_{OUT}} \quad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{IN} - P_{NL} - P_{R_{OUT}}}{P_{IN}} \quad (12)$$

$$= \frac{V_{IN} \bullet I_{IN} - P_{NL} - (I_{OUT})^2 \bullet R_{OUT}}{V_{IN} \bullet I_{IN}}$$

$$= 1 - \frac{(P_{NL} + (I_{OUT})^2 \bullet R_{OUT})}{V_{IN} \bullet I_{IN}}$$

Input and Output Filter Design

A major advantage of SAC™ systems versus conventional PWM converters is that the transformers do not require large functional filters. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of input voltage and output current and efficiently transfers charge through the isolation transformer. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieve power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

1. *Guarantee low source impedance:*

   To take full advantage of the BCM module's dynamic response, the impedance presented to its input terminals must be low from DC to approximately 5MHz. The connection of the bus converter module to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100nH, the input should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200nH, the RC damper may be as high as 47µF in series with 0.3Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

2. *Further reduce input and/or output voltage ripple without sacrificing dynamic response:*

   Given the wide bandwidth of the module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the source will appear at the output of the module multiplied by its K factor. This is illustrated in Figures 14 and 15.

3. *Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and cause failures:*

   The module input/output voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating input range. Even during this condition, the powertrain is exposed to the applied voltage and power MOSFETs must withstand it. A criterion for protection is the maximum amount of energy that the input or output switches can tolerate if avalanched.

Total load capacitance at the output of the BCM module shall not exceed the specified maximum. Owing to the wide bandwidth and low output impedance of the module, low-frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the input of the module. At frequencies <500kHz the module appears as an impedance of R_{OUT} between the source and load.

Within this frequency range, capacitance at the input appears as effective capacitance on the output per the relationship defined in Eq. 6.

$$C_{OUT} = \frac{C_{IN}}{K^2} \qquad (13)$$

This enables a reduction in the size and number of capacitors used in a typical system.

Thermal Considerations

VI Chip® products are multi-chip modules whose temperature distribution varies greatly for each part number as well as with the input / output conditions, thermal management and environmental conditions. Maintaining the top of the BCM48Bx120y120B00 case to less than 100°C will keep all junctions within the VI Chip module below 125°C for most applications.

The percent of total heat dissipated through the top surface versus through the J-lead is entirely dependent on the particular mechanical and thermal environment. The heat dissipated through the top surface is typically 60%. The heat dissipated through the J-lead onto the PCB surface is typically 40%. Use 100% top surface dissipation when designing for a conservative cooling solution.

It is not recommended to use a VI Chip module for an extended period of time at full load without proper heat sinking.

Current Sharing

The performance of the SAC™ topology is based on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple BCM modules of a given part number are connected in an array they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide as symmetric a PCB layout as possible among modules
- Apply same input / output filters (if present) to each unit.

For further details see AN:016 Using BCM Bus Converters in High Power Arrays.

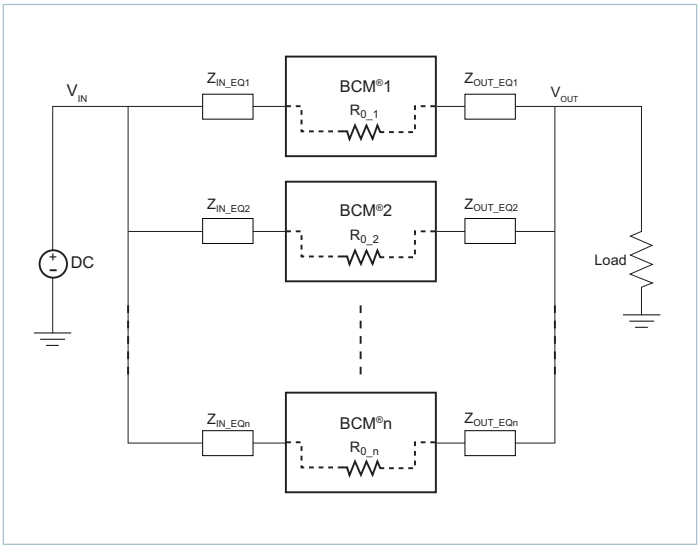


Figure 21 — *BCM module array*

Fuse Selection

In order to provide flexibility in configuring power systems VI Chip® modules are not internally fused. Input line fusing of VI Chip products is recommended at system level to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating (usually greater than maximum current of BCM module)
- Maximum voltage rating (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t
- Recommend fuse: ≤ 3.15A Littlefuse Nano² Fuse.

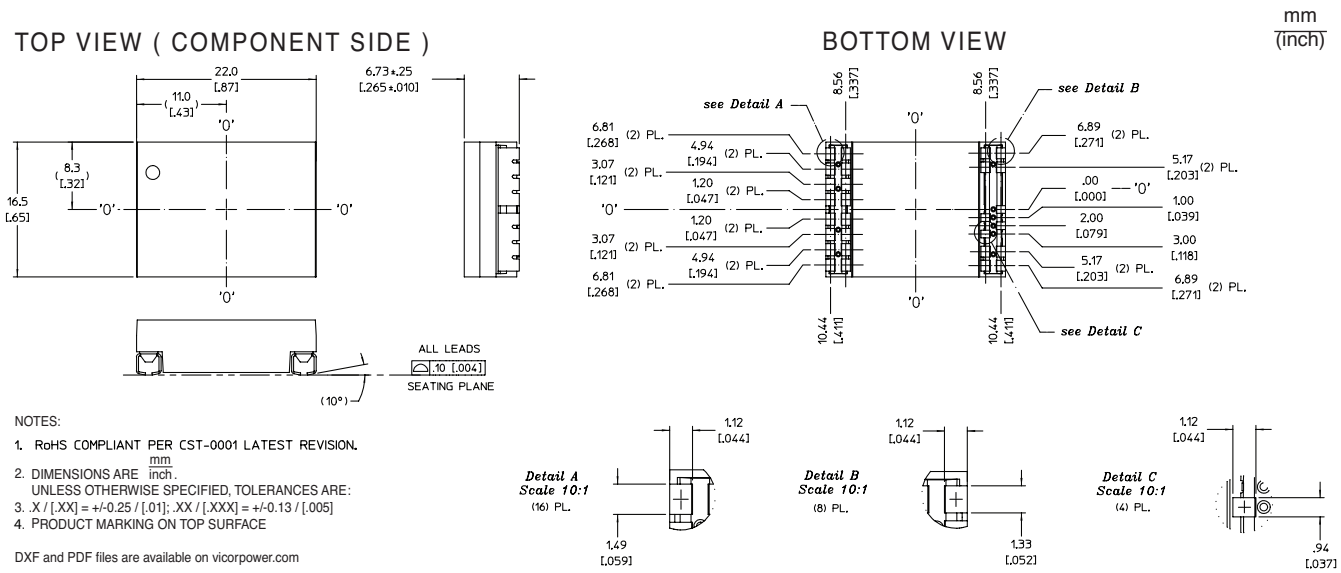
Reverse Operation

BCM modules are capable of reverse power operation. Once the unit is started, energy will be transferred from secondary back to the primary whenever the secondary voltage exceeds $V_{IN} \bullet K$. The module will continue operation in this fashion for as long as no faults occur.

The BCM48Bx120y120B00 has not been qualified for continuous operation in a reverse power condition. Furthermore fault protections which help protect the module in forward operation will not fully protect the module in reverse operation.

Transient operation in reverse is expected in cases where there is significant energy storage on the output and transient voltages appear on the input. Transient reverse power operation of less than 10ms, 10% duty cycle is permitted and has been qualified to cover these cases.

Mechanical Drawing

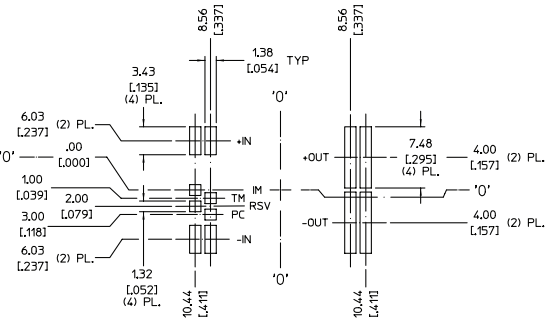


NOTES:

1. RoHS COMPLIANT PER CST-0001 LATEST REVISION.
2. DIMENSIONS ARE mm (inch).
   UNLESS OTHERWISE SPECIFIED, TOLERANCES ARE:
3. .X / [.XX] = +/-0.25 / [.01]; .XX / [.XXX] = +/-0.13 / [.005]
4. PRODUCT MARKING ON TOP SURFACE

DXF and PDF files are available on vicorpower.com

Recommended Land Pattern



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4. PRODUCT MARKING ON TOP SURFACE

DXF and PDF files are available on vicorpower.com

Recommended Heat Sink Push Pin Location

Notes:
1. Maintain 3.50 (0.138) Dia. keep-out zone free of copper, all PCB layers.

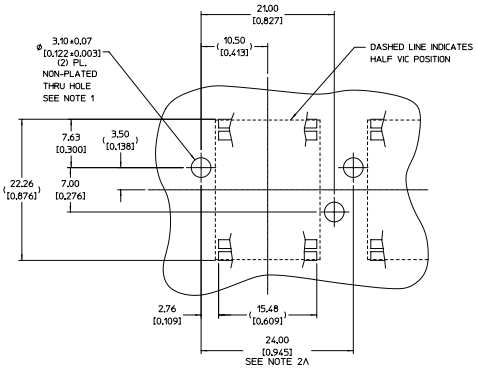
2. (A) minimum recommended pitch is 24.00 (0.945) this provides 7.50 (0.295) component edge–to–edge spacing, and 0.50 (0.020) clearance between Vicor heat sinks.
(B) Minimum recommended pitch is 25.50 (1.004). This provides 9.00 (0.354) component edge–to–edge spacing, and 2.00 (0.079) clearance between Vicor heat sinks.

3. V•I Chip™ module land pattern shown for reference only, actual land pattern may differ. Dimensions from edges of land pattern to push–pin holes will be the same for all half size V•I Chip products.

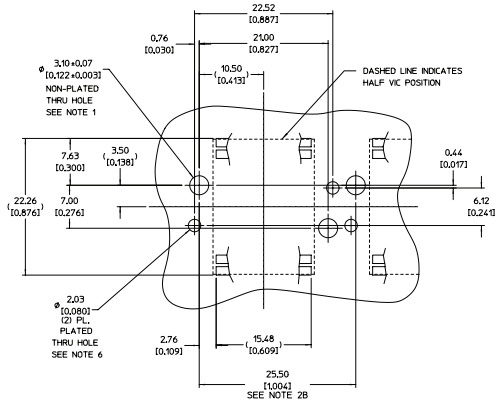
4. RoHS compliant per CST–0001 latest revision.

5. Unless otherwise specified:
Dimensions are mm (inches)
tolerances are:
x.x (x.xx) = ±0.3 (0.01)
x.xx (x.xxx) = ±0.13 (0.005)

6. Plated through holes for grounding clips (33855) shown for reference. Heat sink orientation and device pitch will dictate final grounding solution.



(NO GROUNDING CLIPS)



(WITH GROUNDING CLIPS)

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