



Z86C61/62/96

CMOS Z8® MICROCONTROLLER

FEATURES

- 8-Bit CMOS Microcontroller
- 40-Pin DIP, 44-Pin PLCC, 64-Pin DIP, or 68-Pin PLCC Package
- 32 Input/Output Lines (Z86C61 Only)
- 52 Input/Output Lines (Z86C62 and Z86C96)
- 3.0V to 5.5V Operating Range
- Low Power Consumption: 200 mW (max)
- Fast Instruction Pointer: 0.75 μ s @ 16 MHz
- Two Standby Modes: STOP and HALT
- Full-Duplex UART
- All Digital Inputs are TTL Levels
- Auto Latches
- RAM and ROM Protect
- 16 Kbytes of ROM
- 256 Bytes of RAM
- Two Programmable 8-Bit Counter/Timers, Each with 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Eight Different Sources
- Clock Speeds: 16 and 20 MHz
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive

GENERAL DESCRIPTION

The Z86C61/62/96 microcontroller is a member of the Z8 single-chip microcontroller family with 16 Kbytes of ROM and 256 bytes of RAM. The Z86C96 is ROMless.

The Z86C61 is offered in 40-pin DIP and 44-pin PLCC style packages, however, the ROMless pin option is available on the 44-pin version only. The Z86C62/96 is offered in 64-pin DIP and 68-pin PLCC style packages. A ROMless pin option enables these MCUs to address both external memory and preprogrammed ROM, making them well-suited for high-volume applications or where code flexibility is required.

With 16 Kbytes of ROM and 256 bytes of general-purpose RAM, these low-cost, low power consumption CMOS Z86C61/62/96 MCUs offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z86C61/62/96 architecture is characterized by Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For applications which demand powerful I/O capabilities, the Z86C61 fulfills this with 32 pins dedicated to input and output. These lines are grouped into four ports with eight lines each. The Z86C62/96 has 52 pins for input and output, and these lines are grouped into six, 8-bit ports and one 4-bit port. Each port is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

GENERAL DESCRIPTION (Continued)

There are three basic address spaces available to support this configuration: Program Memory, Data Memory, and 236 General-Purpose Registers.

To unburden the program from coping with the real-time tasks, such as counting/timing and serial data communication, the Z86C61/62/96 offers two on-chip counter/timers with a large number of user selectable modes, and an on-board UART (Figures 1, 2, and 3).

Notes:

All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power Ground	V_{CC} GND	V_{DD} V_{SS}

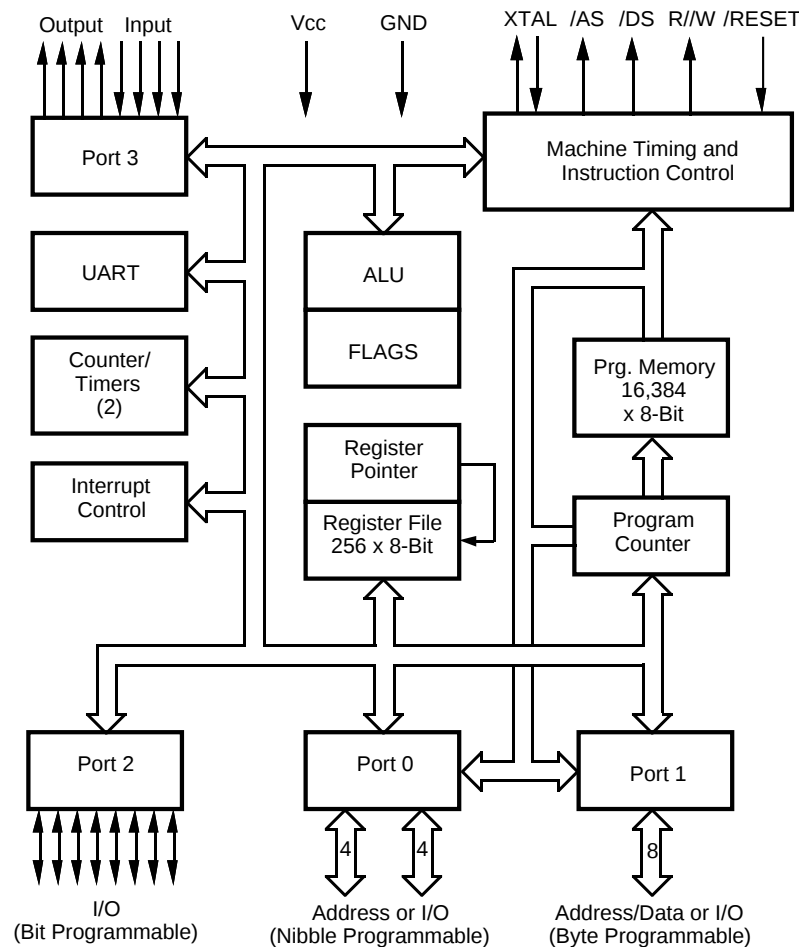


Figure 1. Z86C61 Functional Block Diagram

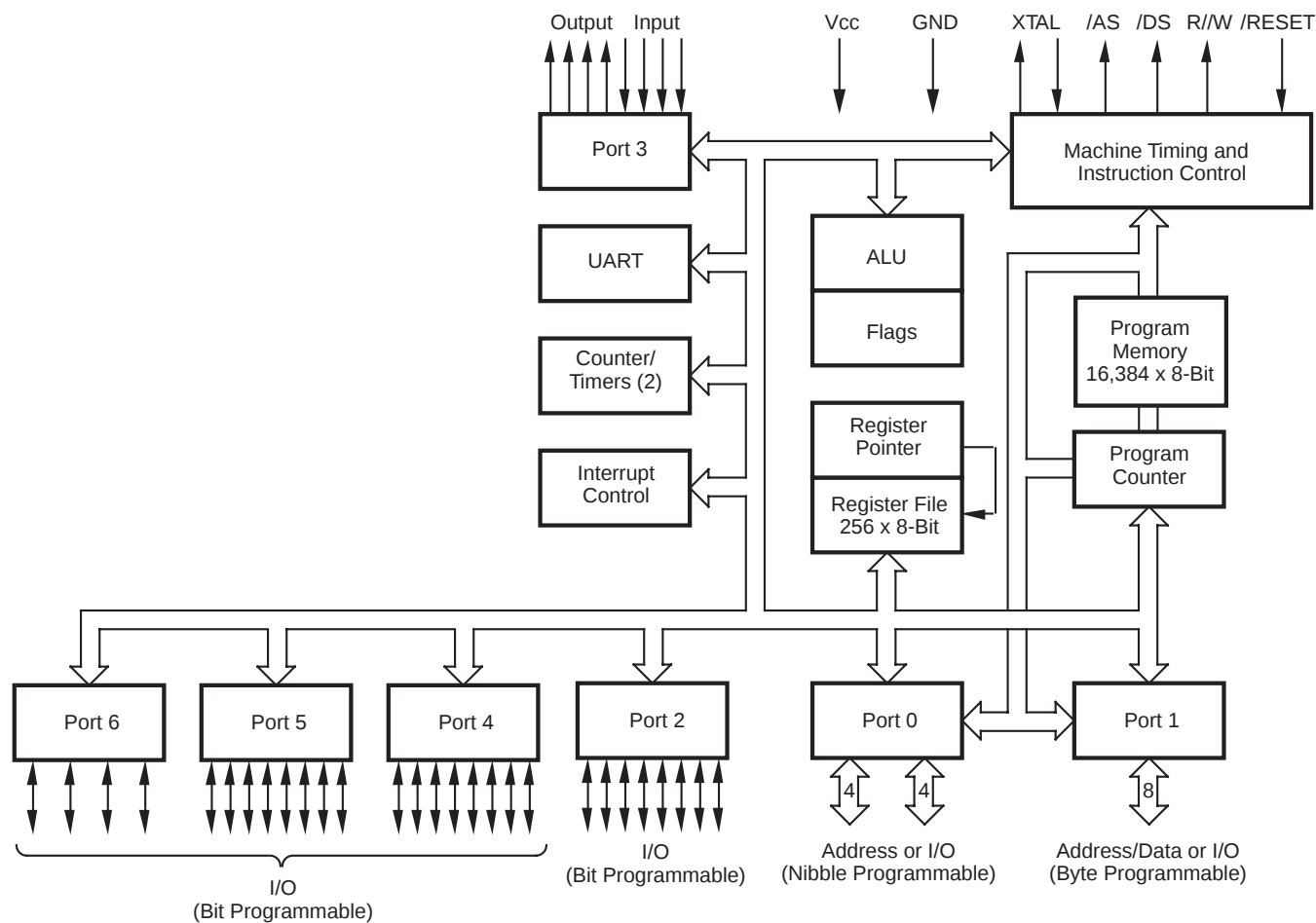


Figure 2. Z86C62 Functional Block Diagram

GENERAL DESCRIPTION (Continued)

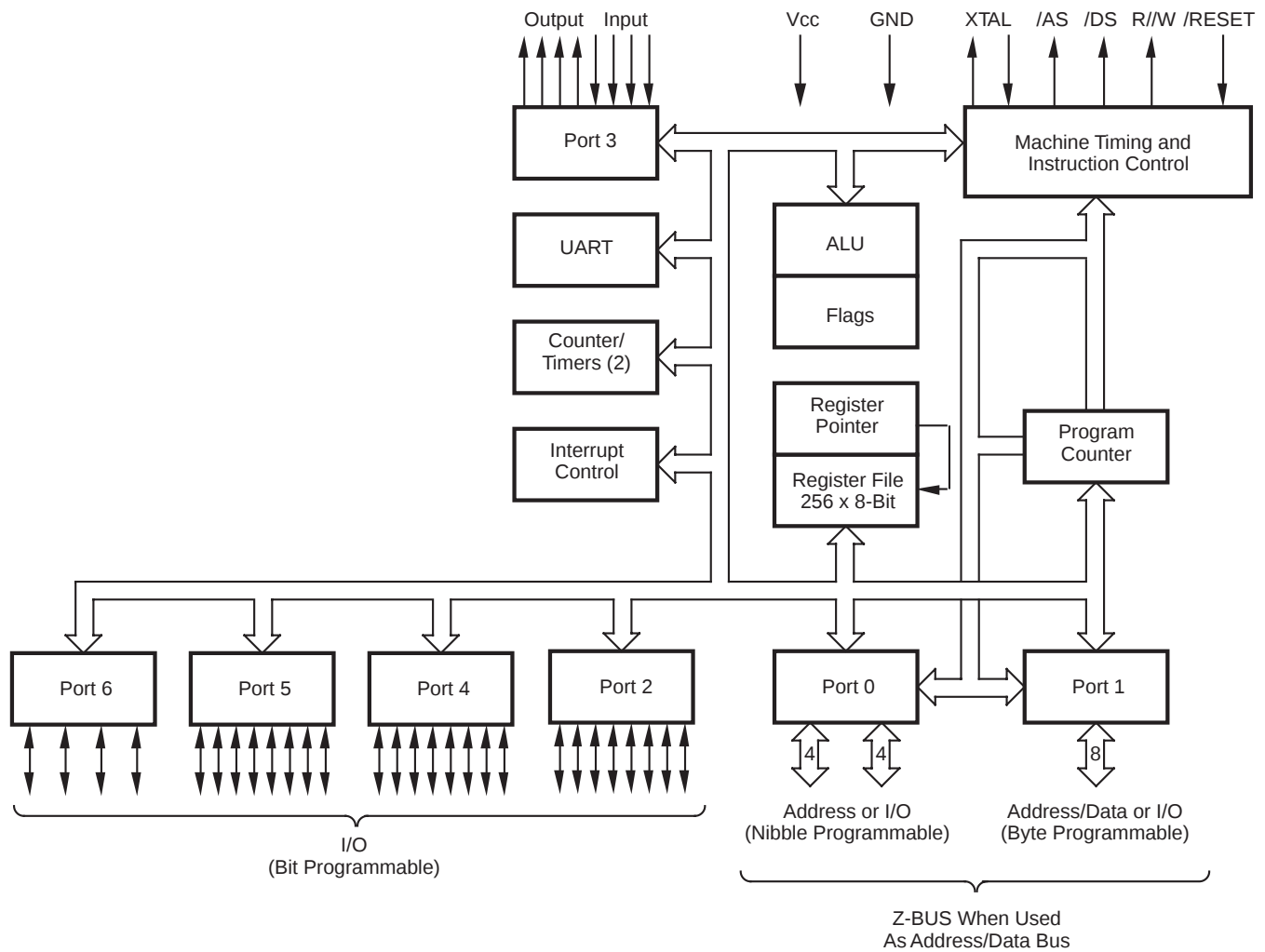
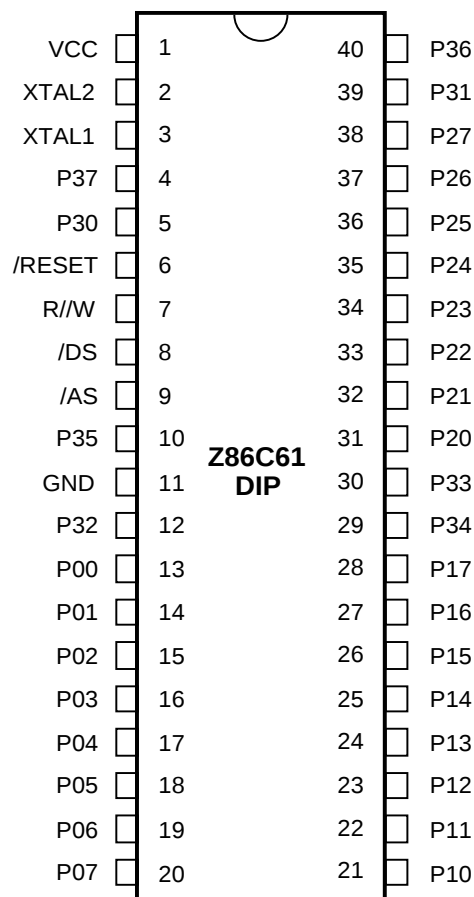


Figure 3. Z86C96 Functional Block Diagram

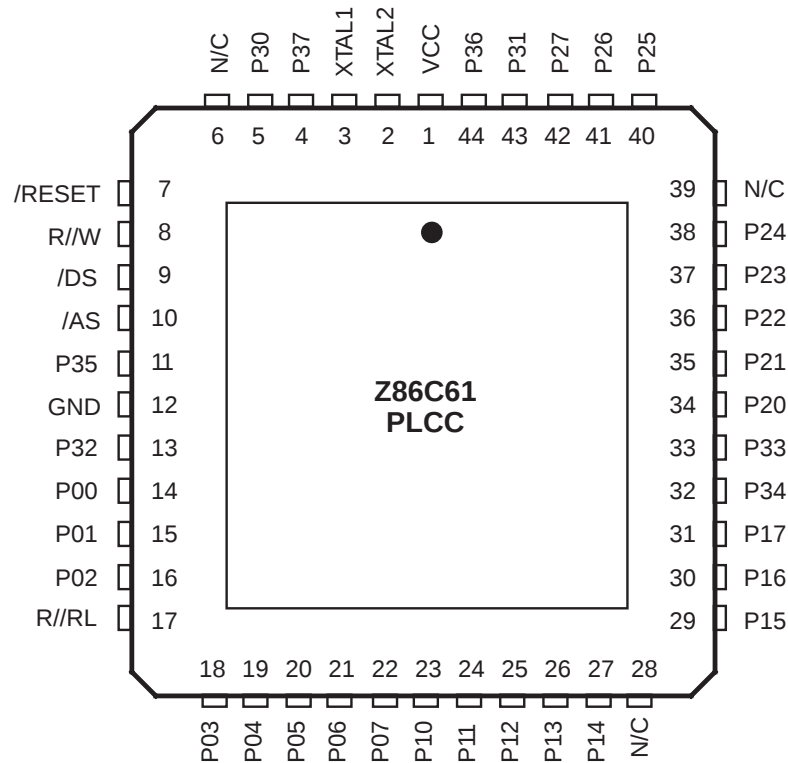
PIN DESCRIPTION



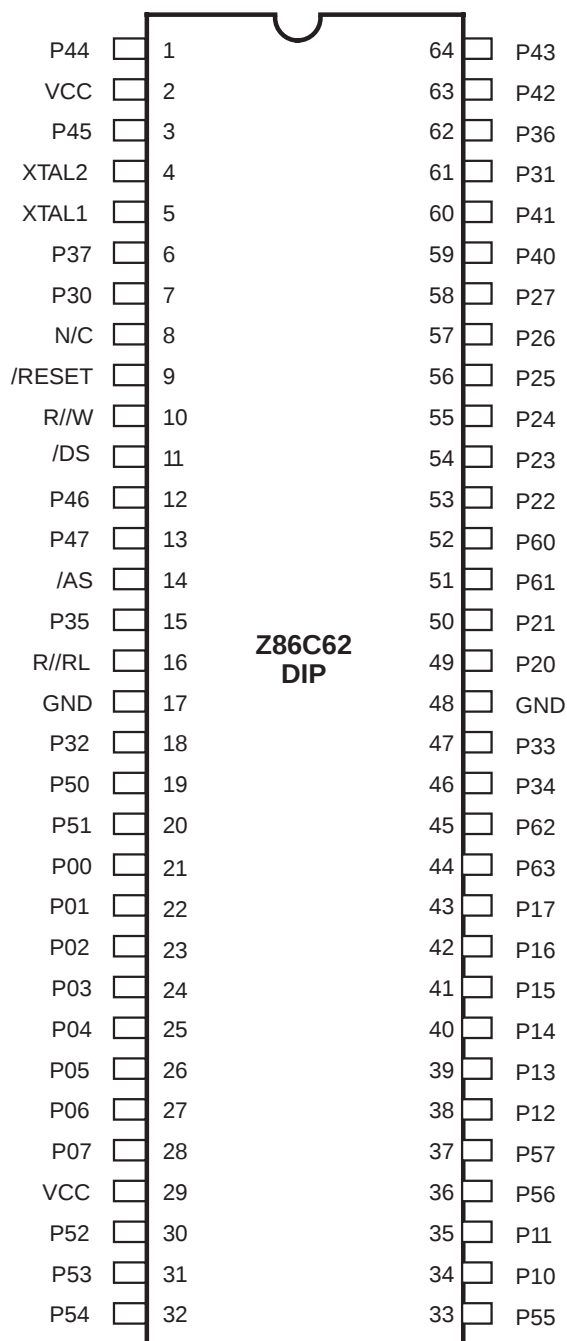
**Figure 4. Z86C61 40-Pin DIP
Pin Assignments**

Table 1. Z86C61 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	V _{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	/RESET	Reset	Input
7	R/W	Read/Write	Output
8	/DS	Data Strobe	Output
9	/AS	Address Strobe	Output
10	P35	Port 3, Pin 5	Output
11	GND	Ground	Input
12	P32	Port 3, Pin 2	Input
13-20	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
21-28	P17-P10	Port 1, Pins 0,1,2,3,4,5,6,7	In/Output
29	P34	Port 3, Pin 4	Output
30	P33	Port 3, Pin 3	Input
31-38	P27-P20	Port 2, Pins 0,1,2,3,4,5,6,7	In/Output
39	P31	Port 3, Pin 1	Input
40	P36	Port 3, Pin 6	Output

PIN DESCRIPTION (Continued)

Figure 5. Z86C61 44-Pin PLCC Pin Assignments
Table 2. Z86C61 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1	V _{CC}	Power Supply	Input	17	R//RL	ROM/ROMless control	Input
2	XTAL2	Crystal, Oscillator Clock	Output	18-22	P07-P03	Port 0, Pins 3,4,5,6,7	In/Output
3	XTAL1	Crystal, Oscillator Clock	Input	23-27	P14-P10	Port 1, Pins 0,1,2,3,4	In/Output
4	P37	Port 3, Pin 7	Output	28	N/C	Not Connected	Input
5	P30	Port 3, Pin 0	Input	29-31	P17-P15	Port 1, Pins 5,6,7	In/Output
6	N/C	Not Connected	Input	32	P34	Port 3, Pin 4	Output
7	/RESET	Reset	Input	33	P33	Port 3, Pin 3	Input
8	R/W	Read/Write	Output	34-38	P24-P20	Port 2, Pins 0,1,2,3,4	In/Output
9	/DS	Data Strobe	Output	39	N/C	Not Connected	Input
10	/AS	Address Strobe	Output	40-42	P25-P27	Port 2, Pins 5,6,7	In/Output
11	P35	Port 3, Pin 5	Output	43	P31	Port 3, Pin 1	Input
12	GND	Ground	Input	44	P36	Port 3, Pin 6	Output
13	P32	Port 3, Pin 2	Input				
14-16	P02-P00	Port 0, Pins 0,1,2	In/Output				


Table 3. Z86C62 64-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	P44	Port 4, Pin 4	In/Output
2	V _{CC}	Power Supply	Input
3	P45	Port 4, Pin 5	In/Output
4	XTAL2	Crystal, Oscillator Clock	Output
5	XTAL1	Crystal, Oscillator Clock	Input
6	P37	Port 3, Pin 7	Output
7	P30	Port 3, Pin 0	Input
8	N/C	Not Connected	Input
9	/RESET	Reset	Input
10	R/W	Read/Write	Output
11	/DS	Data Strobe	Output
12-13	P47-P46	Port 4, Pin 6,7	In/Output
14	/AS	Address Strobe	Output
15	P35	Port 3, Pin 5	Output
16	R/RL	ROM/ROMless control	Input
17	GND	Ground	Input
18	P32	Port 3, Pin 2	Input
19-20	P51-P50	Port 5, Pin 0,1	In/Output
21-28	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
29	V _{CC}	Power Supply	Input
30-33	P52-P55	Port 5, Pins 2,3,4,5	In/Output
34-35	P11-P10	Port 1, Pins 0,1	In/Output
36-37	P57-P56	Port 5, Pins 6,7	In/Output
38-43	P17-P12	Port 1, Pins 2,3,4,5,6,7	In/Output
44-45	P63-P62	Port 6, Pins 3,2	In/Output
46	P34	Port 3, Pin 4	Output
47	P33	Port 3, Pin 3	Input
48	GND	Ground	Input
49-50	P21-P20	Port 2, Pins 0,1	In/Output
51-52	P61-P60	Port 6, Pins 1,0	In/Output
53-58	P27-P22	Port 2, Pins 2,3,4,5,6,7	In/Output
59-60	P41-P40	Port 4, Pins 0,1	In/Output
61	P31	Port 3, Pin 1	Input
62	P36	Port 3, Pin 6	Output
63	P42	Port 4, Pin 2	In/Output
64	P43	Port 4, Pin 3	In/Output

Figure 6. Z86C62 64-Pin DIP Pin Assignments

PIN DESCRIPTION (Continued)

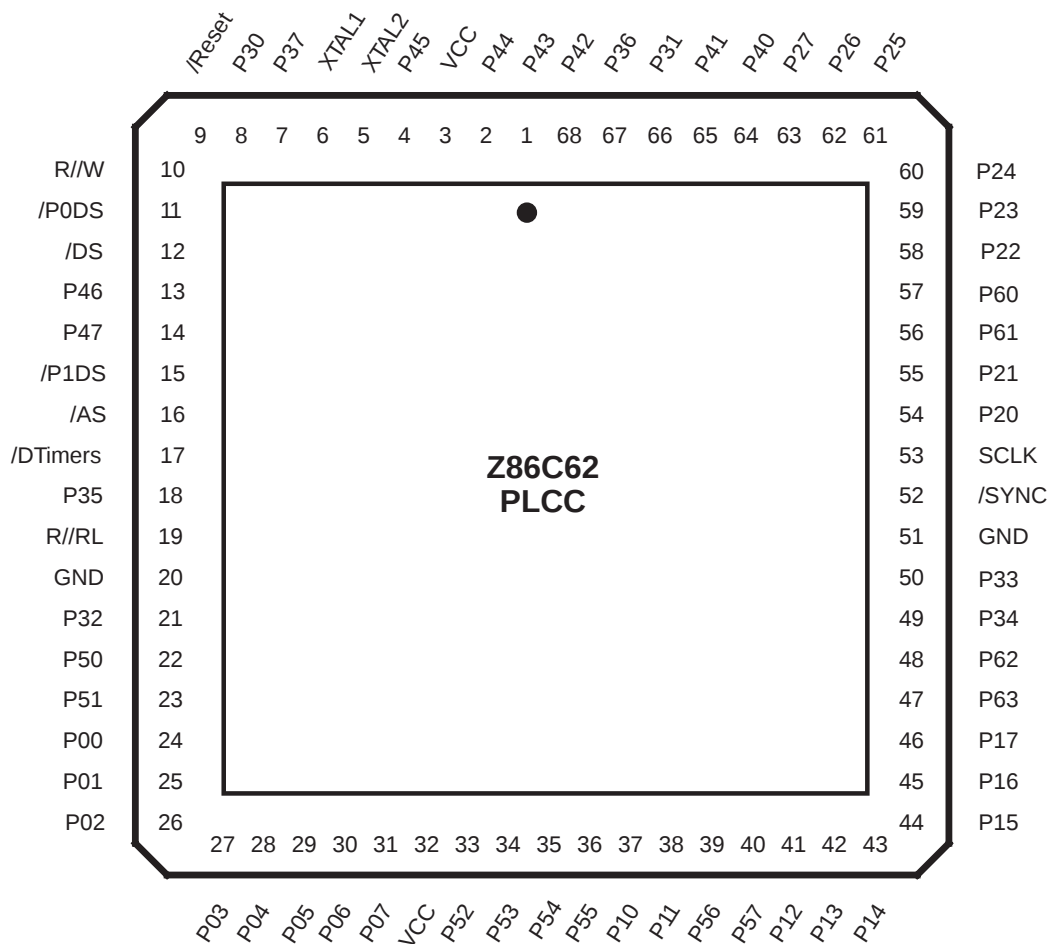
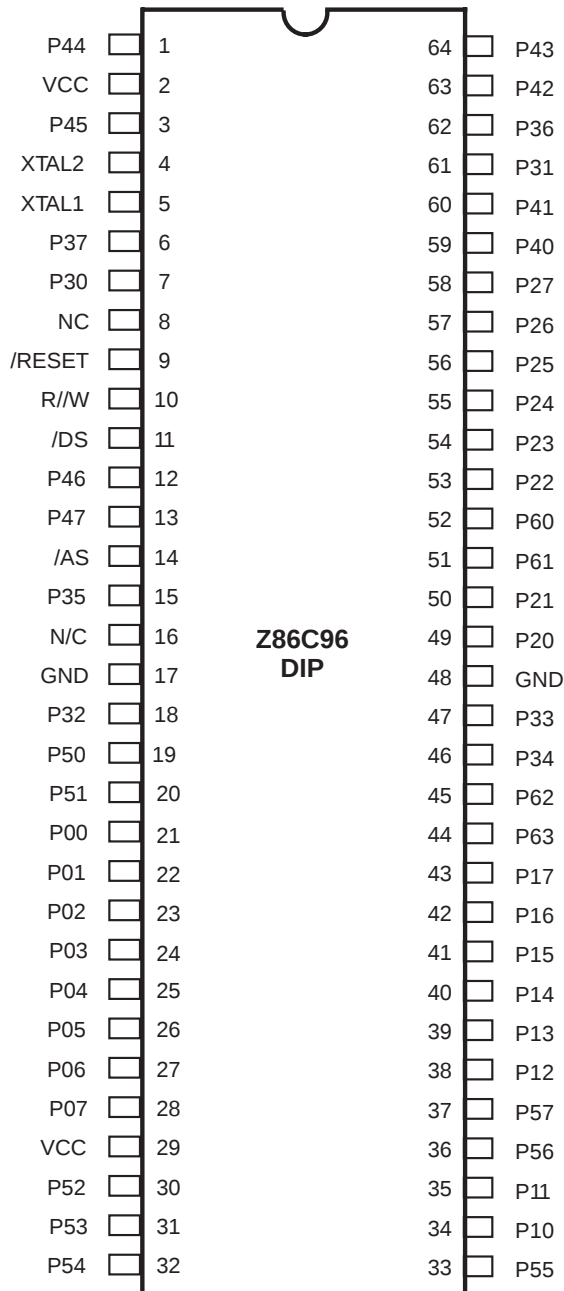


Figure 7. Z86C62 68-Pin PLCC Pin Assignments

Table 4. Z86C62 68-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1-2	P44-P43	Port 4, Pins 3,4	In/Output	24-31	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
3	V _{CC}	Power Supply	Input	32	V _{CC}	Power Supply	Input
4	P45	Port 4, Pin 5	In/Output	33-36	P55-P52	Port 5, Pins 2,3,4,5	In/Output
5	XTAL2	Crystal, Oscillator Clock	Output	37-38	P11-P10	Port 1, Pins 0,1	In/Output
6	XTAL1	Crystal, Oscillator Clock	Input	39-40	P56-P57	Port 5, Pins 6,7	In/Output
7	P37	Port 3, Pin 7	Output	41-46	P17-P12	Port 1, Pins 2,3,4,5,6,7	In/Output
8	P30	Port 3, Pin 0	Input	47-48	P63-P62	Port 6, Pins 3,2	In/Output
9	/RESET	Reset	Input	49	P34	Port 3, Pin 4	Output
10	R/W	Read/Write	Output	50	P33	Port 3, Pin 3	Input
11	/P0DS	Port 0 Data Strobe	Output	51	GND	Ground	Input
12	/DS	Data Strobe	Output	52	/SYNC	Synchronization	Output
13-14	P47-P46	Port 4, Pins 6,7	In/Output	53	SCLK	System Clock	Output
15	/P1DS	Port 1, Data Strobe	Output	54-55	P21-P20	Port 2, Pins 0,1	In/Output
16	/AS	Address Strobe	Output	56-57	P60-P61	Port 6, Pins 1,0	In/Output
17	/DTIMER	DTIMER	Input	58-63	P27-P22	Port 2, Pins 2,3,4,5,6,7	In/Output
18	P35	Port 3, Pin 5	Output	64-65	P41-P40	Port 4, Pins 0,1	In/Output
19	R//RL	ROM/ROMless control	Input	66	P31	Port 3, Pin 1	Input
20	GND	Ground	Input	67	P36	Port 3, Pin 6	Output
21	P32	Port 3, Pin 2	Input	68	P42	Port 4, Pin 2	In/Output
22-23	P51-P50	Port 5, Pins 0,1	In/Output				

PIN DESCRIPTION (Continued)

Figure 8. Z86C96 64-Pin DIP Pin Assignments
Table 5. Z86C96 64-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	P44	Port 4, Pin 4	In/Output
2	V _{CC}	Power Supply	Input
3	P45	Port 4, Pin 5	In/Output
4	XTAL2	Crystal, Oscillator Clock	Output
5	XTAL1	Crystal, Oscillator Clock	Input
6	P37	Port 3, Pin 7	Output
7	P30	Port 3, Pin 0	Input
8	N/C	Not Connected	Input
9	/RESET	Reset	Input
10	R/W	Read/Write	Output
11	/DS	Data Strobe	Output
12-13	P47-P46	Port 4, Pins 6,7	In/Output
14	/AS	Address Strobe	Output
15	P35	Port 3, Pin 5	Output
16	N/C	Not Connected	Input
17	GND	Ground	Input
18	P32	Port 3, Pin 2	Input
19-20	P51-P50	Port 5, Pins 0,1	In/Output
21-28	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
29	V _{CC}	Power Supply	Input
30-33	P55-P52	Port 5, Pins 2,3,4,5	In/Output
34-35	P11-P10	Port 1, Pins 0,1	In/Output
36-37	P56-P57	Port 5, Pins 6,7	In/Output
38-43	P17-P12	Port 1, Pins 2,3,4,5,6,7	In/Output
44-45	P63-P62	Port 6, Pins 3,2	In/Output
46	P34	Port 3, Pin 4	Output
47	P33	Port 3, Pin 3	Input
48	GND	Ground	Input
49-50	P21-P20	Port 2, Pins 0,1	In/Output
51-52	P61-P60	Port 6, Pins 1,0	In/Output
53-58	P27-P22	Port 2, Pins 2,3,4,5,6,7	In/Output
59-60	P41-P40	Port 4, Pins 0,1	In/Output
61	P31	Port 3, Pin 1	Input
62	P36	Port 3, Pin 6	Output
63	P42	Port 4, Pin 2	In/Output
64	P43	Port 4, Pin 3	In/Output

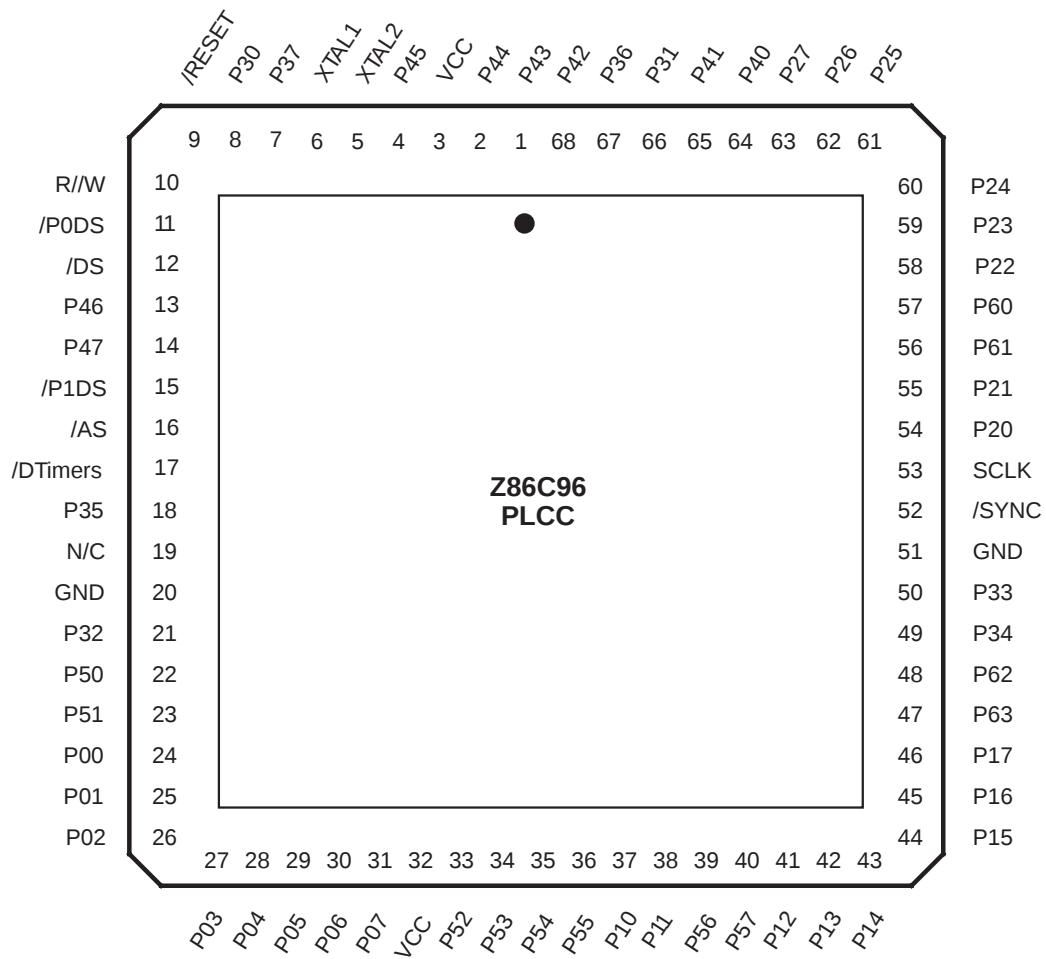


Figure 9. Z86C96 68-Pin PLCC Pin Assignments

PIN DESCRIPTION (Continued)

Table 6. Z86C96 68-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1-2	P44-P43	Port 4, Pins 3,4	In/Output	24-31	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
3	V _{CC}	Power Supply	Input	32	V _{CC}	Power Supply	Input
4	P45	Port 4, Pin 5	In/Output	33-36	P55-P52	Port 5, Pins 2,3,4,5	In/Output
5	XTAL2	Crystal, Oscillator Clock	Output	37-38	P11-P10	Port 1, Pins 0,1	In/Output
6	XTAL1	Crystal, Oscillator Clock	Input	39-40	P57-P56	Port 5, Pins 6,7	In/Output
7	P37	Port 3, Pin 7	Output	41-46	P17-P12	Port 1, Pins 2,3,4,5,6,7	In/Output
8	P30	Port 3, Pin 0	Input	47-48	P63-P62	Port 6, Pins 3,2	In/Output
9	/RESET	Reset	Input	49	P34	Port 3, Pin 4	Output
10	R/W	Read/Write	Output	50	P33	Port 3, Pin 3	Input
11	/P0DS	Port 0 Data Strobe	Output	51	GND	Ground	Input
12	/DS	Data Strobe	Output	52	/SYNC	Synchronization	Output
13-14	P47-P46	Port 4, Pins 6,7	In/Output	53	SCLK	System Clock	Output
15	/P1DS	Port 1 Data Strobe	Output	54-55	P21-P20	Port 2, Pins 0,1	In/Output
16	/AS	Address Strobe	Output	56-57	P61-P60	Port 6, Pins 1,0	In/Output
17	/DTIMER	Disable Timers	Input	58-63	P27-P22	Port 2, Pins 2,3,4,5,6,7	In/Output
18	P35	Port 3, Pin 5	Output	64-65	P41-P40	Port 4, Pins 0,1	In/Output
19	N/C	Not Connected	Input	66	P31	Port 3, Pin 1	Input
20	GND	Ground	Input	67	P36	Port 3, Pin 6	Output
21	P32	Port 3, Pin 2	Input	68	P42	Port 4, Pin 2	In/Output
22-23	P51-P50	Port 5, Pins 0,1	In/Output				

PIN FUNCTIONS

R/RL (input, active Low). This pin when connected to GND disables the internal ROM and forces the device to function as a Z86C96 ROMless Z8. (**Note:** When left unconnected or pulled High to V_{CC} the part functions as a normal Z86C61/62 ROM version.) This pin is only available on the 44-pin version of the Z86C61, and both versions of the Z86C62.

/DS (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1, XTAL2 *Crystal 1, Crystal 2* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

R/W (output, write Low). The Read/Write signal is Low when the MCU is writing to the external program or data memory.

/RESET (input, active Low). To avoid asynchronous and noisy reset problems, the Z86C61/62/96 is equipped with a reset filter of four external clocks (4TpC). If the external /RESET signal is less than 4TpC in duration, no reset occurs.

On the fifth clock after the /RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external /RESET, whichever is longer. During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. When /RESET is deactivated, program execution begins at location 000C (HEX). Reset time must be held Low for 50 ms, or until V_{CC} is stable, whichever is longer.

/P0DS *Port 0 Data Strobe* (output, active Low). Signal used to emulate Port 0 when in ROMless mode.

/P1DS *Port 1 Data Strobe* (output, active Low). Signal used to emulate Port 1 when in ROMless mode.

/DTIMERS *Disable Timers* (input, active Low). All timers are stopped by the Low level at this pin. This pin has an internal pull up resistor.

SCLK (output). System clock pin.

/SYNC *Instruction SYNC Signal* (output, active Low). This signal indicates the last clock of the current executing instruction.

Port 0 (P07-P00). Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32

and P35 are used as the handshake control /DAV0 and RDY0 (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble to be under handshake control.

For external memory references, Port 0 can provide address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register.

In ROMless mode, after a hardware reset, Port 0 lines are defined as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine includes reconfiguration to eliminate this extended timing mode (Figure 10).

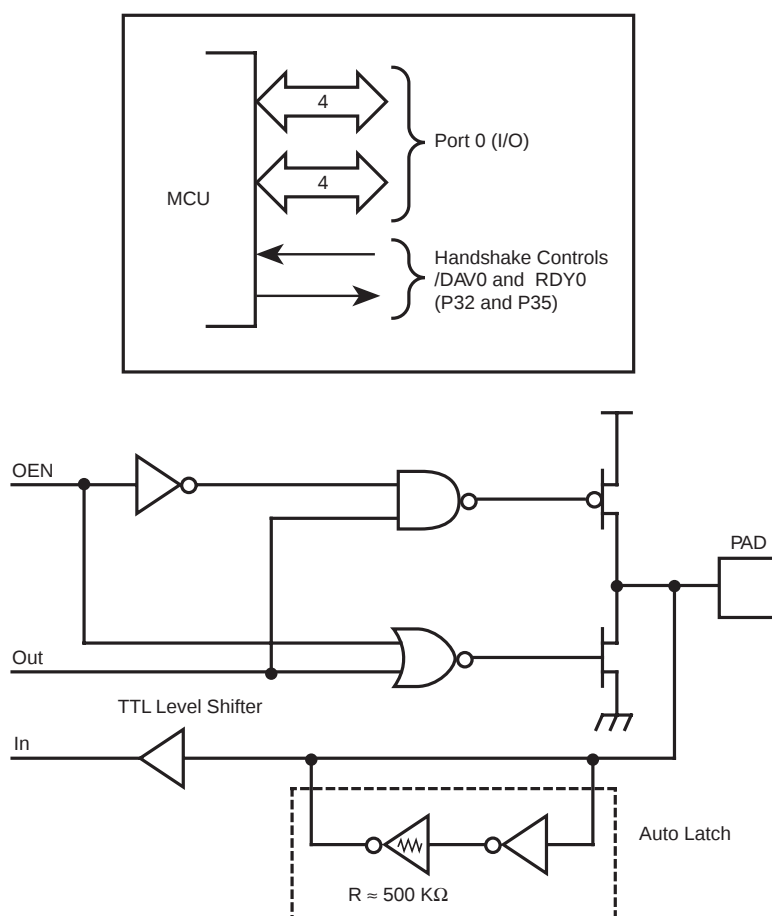


Figure 10. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 1 (P17-P10). Port 1 is an 8-bit, byte programmable, bidirectional, TTL compatible port. It has multiplexed Address (A7-A0) and Data (D7-D0) ports. For Z86C61/62/96, these eight I/O lines can be programmed as Input or Output lines or can be configured under software control as an address/data port for interfacing external memory. When used as an I/O port, Port 1 may be placed under handshake control. In this configuration, Port 3 line P33 and P34 are used as the handshake controls RDY1 and /DAV1.

Memory locations greater than 16,384 are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 must output the additional lines.

Port 1 can be placed in high-impedance state along with Port 0, /AS, /DS, and R/W, allowing the microcontroller to share common resources in multiprocessor and DMA applications. Data transfers can be controlled by assigning P33 as a Bus Acknowledge input, and P34 as a Bus request output (Figure 11).

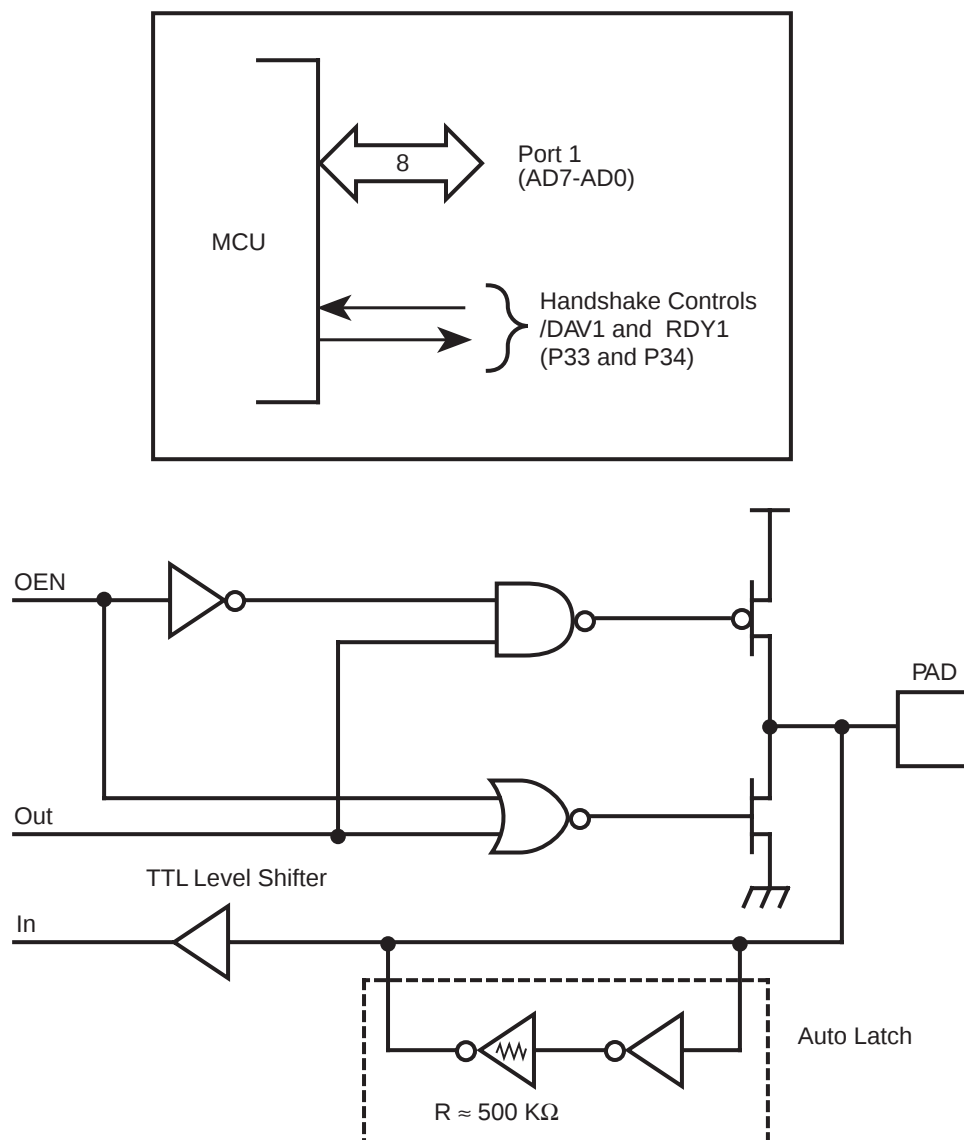


Figure 11. Port 1 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bit programmable, bidirectional, CMOS compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 may be placed under handshake control. In this

configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 12).

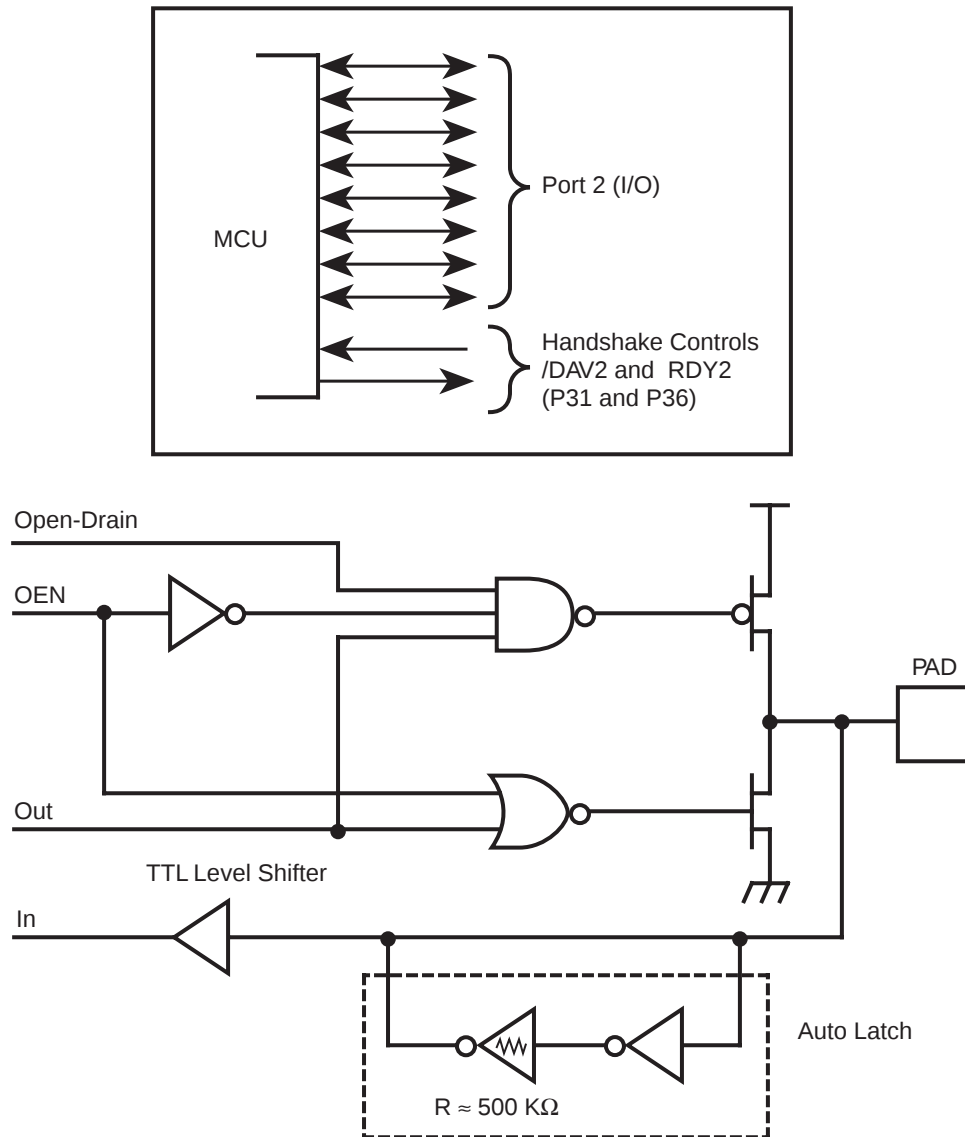


Figure 12. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS compatible four-fixed input and four-fixed output port. These eight I/O lines have four-fixed (P33-P30) input and four-fixed (P37-

P34) output ports. Port 3, when used as serial I/O, are programmed as serial in and serial out, respectively (Figure 13).

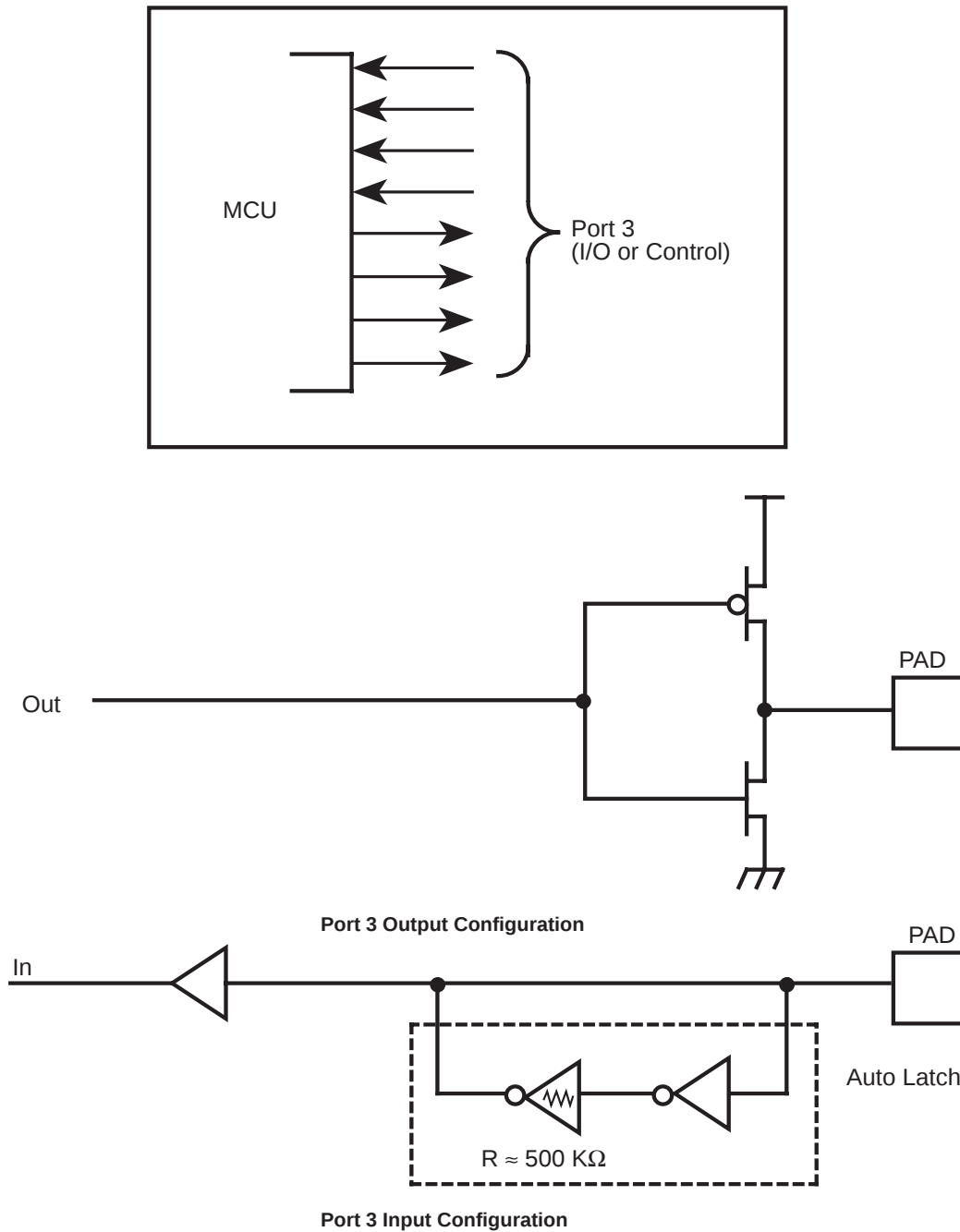


Figure 13. Port 3 Configuration

Port 3 can be configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals

(IRQ3-IRQ0); timer input and output signals (T_{IN} and T_{OUT}), and Data Memory Select (/DM).

Table 7. Port 3 Pin Assignments

Pin	I/O	CTC1	Int.	P0 HS	P1 HS	P2 HS	UART	Ext
P30	IN	T_{IN}	IRQ3	D/R	D/R	D/R	Serial In	
P31	IN		IRQ2					
P32	IN		IRQ0					
P33	IN		IRQ1					
P34	OUT	T_{OUT}		R/D	R/D	R/D	Serial Out	DM
P35	OUT							
P36	OUT							
P37	OUT							
T0			IRQ4					
T1			IRQ5					

Notes:

HS = Handshake Signals
D = Data Available
R = Ready

UART OPERATION

Port 3 lines P30 and P37, can be programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by the Counter/Timer0.

The Z86C61/62/96 automatically adds a start bit and two stop bits to transmitted data (Figure 14). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the

eightth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

Note: UART function is only available in standard timing mode (i.e., P01M D5 = 0).

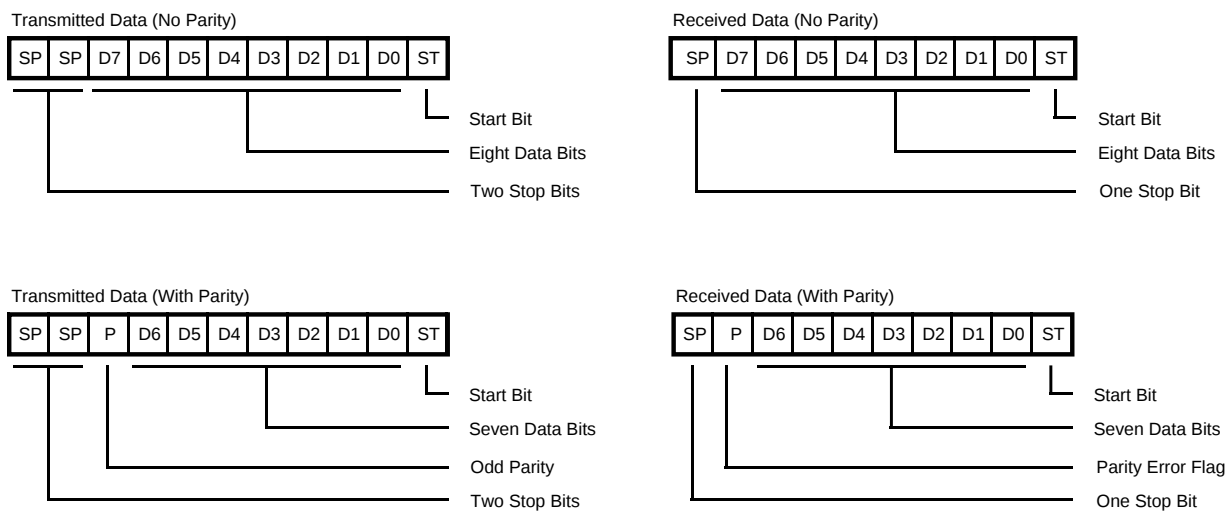


Figure 14. Serial Data Formats

PIN FUNCTIONS (Continued)

Port 4 (P47-P40). Port 4 is an 8-bit, bit programmable, bidirectional, CMOS compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 4 is always available for I/O operation (Figure 15). Port address (F)02.

Port 5 (P57-P50). Same as Port 4. Port address (F)04.

Port 6 (P63-P60). Same as Port 4. (**Note:** this is a 4-bit port, bits D3-D0.) Port address (F)07.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not being driven by any source.

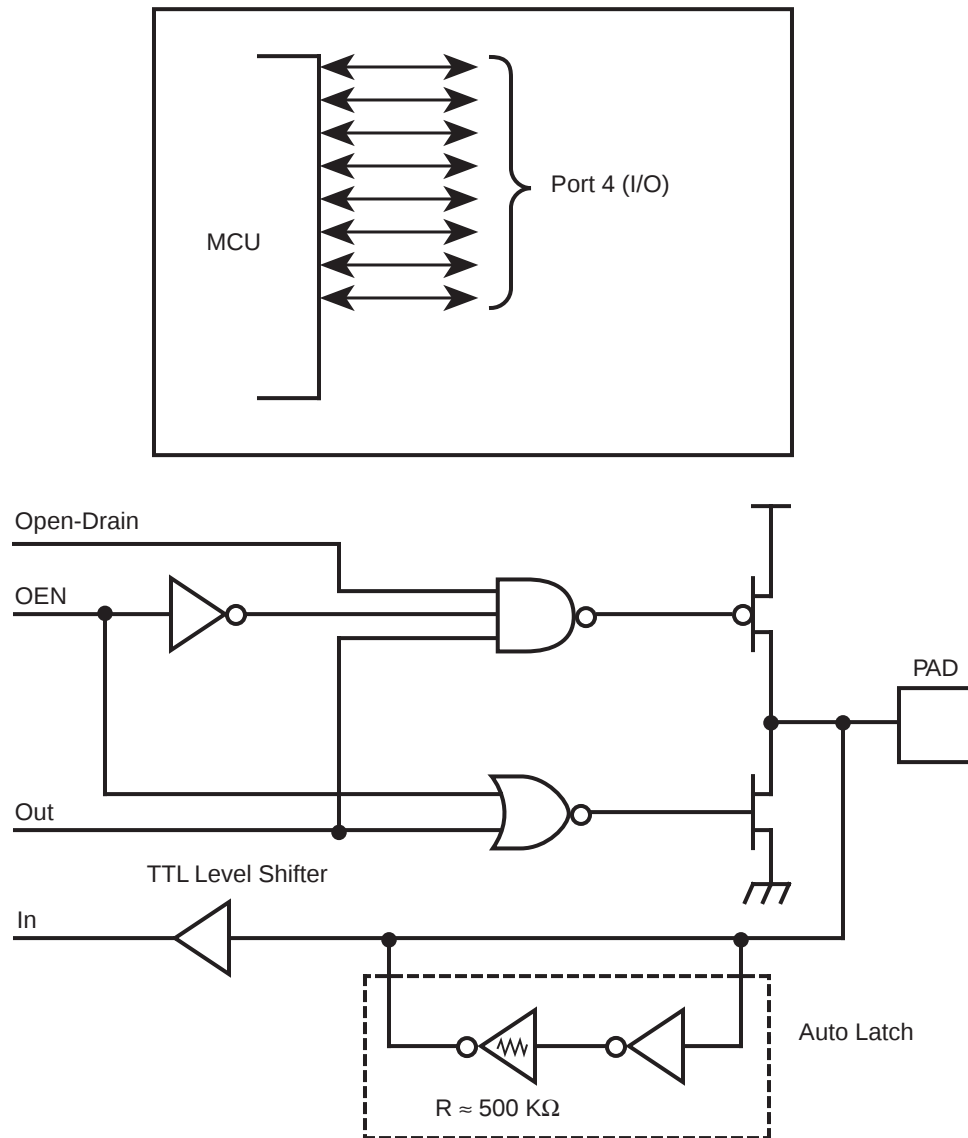


Figure 15. Port 4 Configuration

FUNCTIONAL DESCRIPTION

Address Space

Program Memory. The Z86C61/62 can address up to 48 Kbytes of external program memory (Figure 16). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For ROM mode, byte 13 to byte 16383 consists of on-chip ROM. At addresses 16384 and greater, the Z86C61/62 executes external program memory fetches. The Z86C96, and the Z86C61/62 in ROMless mode, can address up to 64 Kbytes of external program memory. Program execution begins at external location 000CH after a reset.

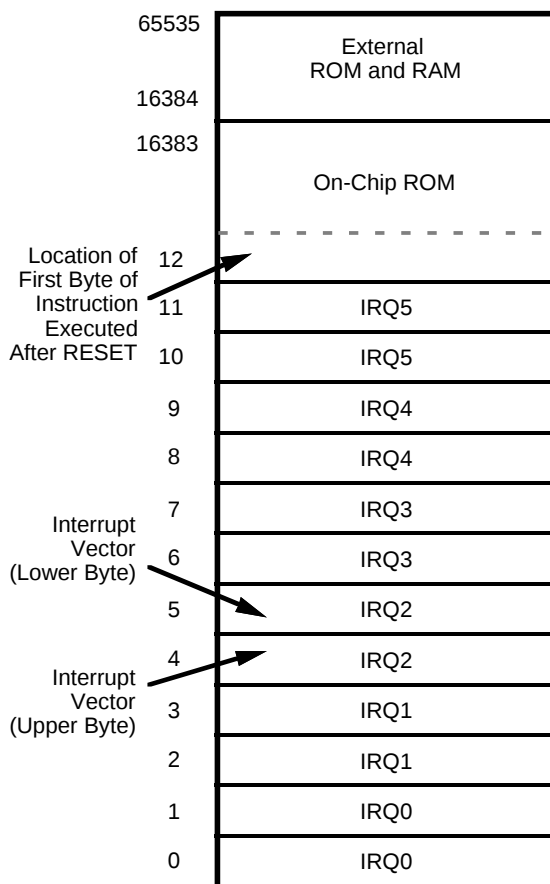


Figure 16. Program Memory Configuration

Data Memory (/DM). The ROM version can address up to 48 Kbytes of external data memory space beginning at location 16384. The ROMless version can address up to 64 Kbytes of external data memory. External data memory may be included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 17). The state of the /DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references DATA (/DM active Low) memory.

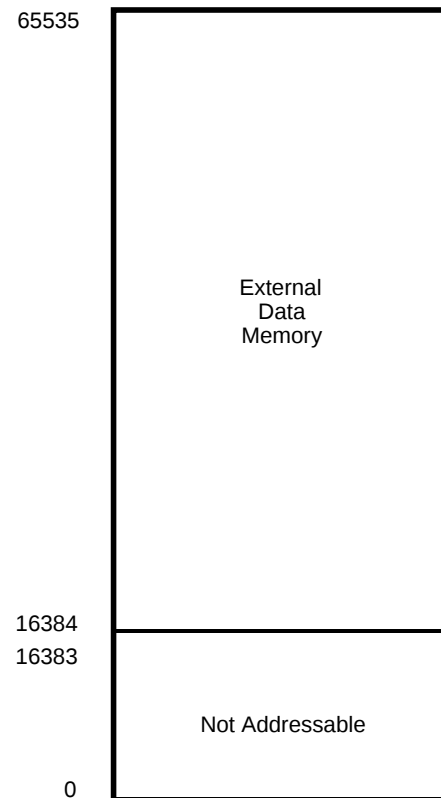


Figure 17. Data Memory Configuration

FUNCTIONAL DESCRIPTION (Continued)

Register File. The Register File consists of four I/O port registers, 236 general-purpose registers and 16 control and status registers (Figure 18). There are eight further registers for I/O ports 4, 5 and 6 in the Expanded Register File (Bank F, R9-R2) (Figure 20).

The instructions can access registers directly or indirectly through an 8-bit address field. The Z86C61/62/96 also allows short 4-bit register addressing using the Register Pointer (Figure 19). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: Register Bank E0-EF can only be accessed through working registers and indirect addressing modes.

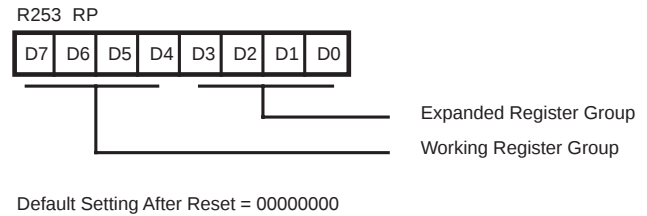


Figure 19. Register Pointer Register

Location		Identifiers
R255	Stack Pointer (Bits 7-0)	SPL
R254	Stack Pointer (Bits 15-8)	SPH
R253	Register Pointer	RP
R252	Program Control Flags	FLAGS
R251	Interrupt Mask Register	IMR
R250	Interrupt Request Register	IRQ
R249	Interrupt Priority Register	IPR
R248	Ports 0-1 Mode	P01M
R247	Port 3 Mode	P3M
R246	Port 2 Mode	P2M
R245	T0 Prescaler	PRE0
R244	Timer/Counter0	T0
R243	T1 Prescaler	PRE1
R242	Timer/Counter1	T1
R241	Timer Mode	TMR
R240	Serial I/O	SIO
R239	General-Purpose Registers	
R4		
R3		P3
R2		P2
R1		P1
R0	Port 0	P0

Figure 18. Register File

Z8 STANDARD CONTROL REGISTERS

RESET CONDITION

D7	D6	D5	D4	D3	D2	D1	D0
U	U	U	U	U	U	U	U
U	U	U	U	U	U	U	U
0	0	0	0	0	0	0	0
U	U	U	U	U	U	U	U
0	U	U	U	U	U	U	U
0	0	0	0	0	0	0	0
U	U	U	U	U	U	U	U
0	1	0	0	1	1	0	1
0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1
U	U	U	U	U	U	U	0
U	U	U	U	U	U	U	U
U	U	U	U	U	U	0	0
U	U	U	U	U	U	U	U
0	0	0	0	0	0	0	0
U	U	U	U	U	U	U	U

REGISTER

% FF	SPL
% FE	SPH
% FD	RP
% FC	FLAGS
% FB	IMR
% FA	IRQ
% F9	IPR
† % F8	P01M
% F7	P3M
% F6	P2M
% F5	PRE0
% F4	T0
% F3	PRE1
% F2	T1
% F1	TMR
% F0	SIO

†

REGISTER POINTER

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

Working Register
Group Pointer

Expanded Register
Group Pointer

Z8 Reg. File

%FF
%F0

%7F

%0F
%00

Reserved

EXPANDED REG. GROUP (F)

REGISTER

% (F) 0F	Reserved
% (F) 0E	Reserved
% (F) 0D	Reserved
% (F) 0C	Reserved
% (F) 0B	Reserved
% (F) 0A	ICE
% (F) 09	P6M
% (F) 08	P6D
% (F) 07	P6
% (F) 06	P45M
% (F) 05	P5D
% (F) 04	P5
% (F) 03	P4D
% (F) 02	P4
% (F) 01	Reserved
% (F) 00	Reserved

RESET CONDITION

EXPANDED REG. GROUP (0)

REGISTER

% (0) 03	P3
% (0) 02	P2
% (0) 01	P1
% (0) 00	P0

RESET CONDITION

1	1	1	1	U	U	U	U
U	U	U	U	U	U	U	U
U	U	U	U	U	U	U	U
U	U	U	U	U	U	U	U

U = Unknown

† = For Z86C96 (ROMless) Reset condition: "10110110"

Figure 20. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

Expanded Register File. The register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area. The Z8 register address space R0 through R15 has now been implemented as 16 groups of 16 registers per group. These register groups are known as the ERF (Expanded Register File). Bits 7-4 of Register RP select the working register group. Bits 3-0 of Register RP select the expanded register group (Figure 21). Eight I/O port registers reside in the Expanded Register File at Bank F. The rest of the Expanded Register is not physically implemented and is open for future expansion.

The upper nibble of the register pointer (Figure 20) selects which group of 16 bytes in the register file, out of the full 256, will be accessed. The lower nibble selects the expanded register file bank and in the case of the Z86C61/62/96, only Bank F is implemented. A 0H in the lower nibble will allow the normal register file to be addressed, but any other value from 1H to FH will exchange the lower 16 registers in favor of an expanded register group of 16 registers.

For example:

Z86C61: (See Figures 18 and 19)

R253 RP = 00H	R0 = Port 0	R2 = Port 2
	R1 = Port 1	R3 = Port 3

But If:

R253 RP = 0FH	R0 = Reserved
	R1 = Reserved
	R2 = Port 4
	R3 = Port 4, Direction Register
	R9 = Port 6, Mode Register

Further examples:

SRP #0FH	Set working group 0 and Bank F
LD R2, #10010110	Load value into Port 4 using working register addressing.
LD 2, #10010110	Load value into Port 4 using absolute addressing.
LD 9, #11110000	Load value into Port 6 mode.
SRP #1FH	Set working group 1 and Bank F
LD R2, #11010110	Load value into general purpose register 12H
LD 12H, #11010110	Load value into general purpose register 12H
LD 2, #10010110	Load value into Port 4

RAM Protect. The upper portion of the RAM's address spaces 80FH to EFH (excluding the control registers) can be protected from reading and writing. The RAM Protect bit option is mask-programmable and is selected by the customer when the ROM code is submitted. After the mask option is selected, the user can activate from the internal ROM code to turn off/on the RAM Protect by loading a bit D6 in the IMR register to either a 0 or a 1, respectively. A 1 in D6 indicates RAM Protect enabled.

ROM Protect. The first 16 Kbytes of program memory is mask programmable. A ROM protect feature prevents “dumping” of the ROM contents by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions by external program memory when pointing to internal memory locations. Therefore these instructions can be used only when they are executed from internal memory, or if they are executed from external memory and pointing to external memory locations.

The ROM Protect option is mask-programmable, to be selected by the customer at the time when the ROM code is submitted.

Stack. The Z86C61/62/96 has a 16-bit Stack Pointer (R255-R254) used for external stack that resides anywhere in the data memory for the ROMless mode, but only from 16384 to 65535 in the ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R239-R4). The high byte of the Stack Pointer (SPH-Bit 8-15) can be used as a general purpose register when using internal stack only.

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 22).

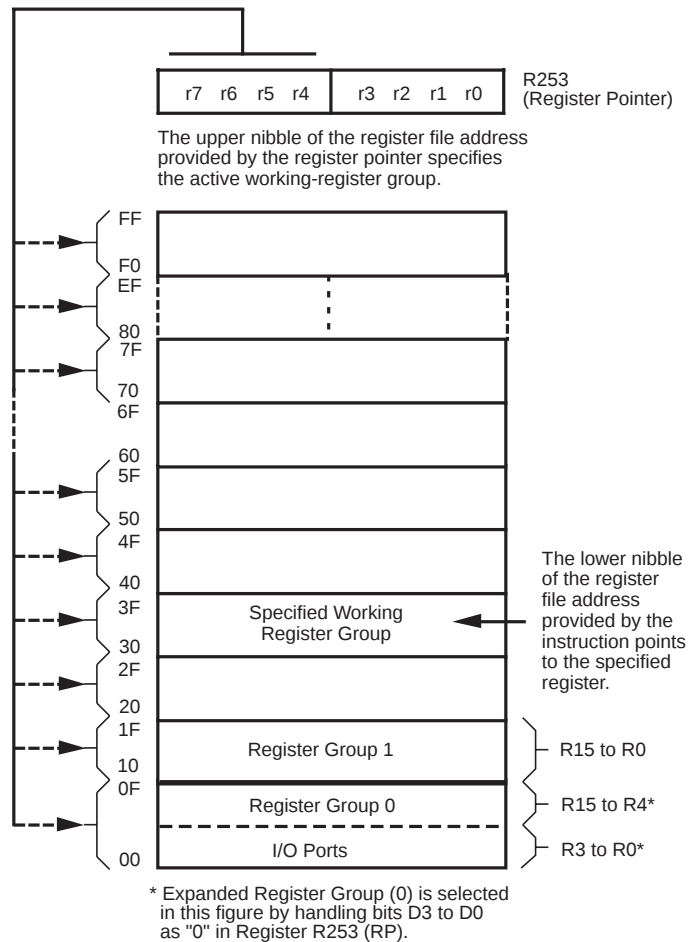


Figure 21. Register Pointer

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counters and prescaler reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counter, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3, line P36, also serves as a timer output (T_{OUT}) through which T0, T1 or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

FUNCTIONAL DESCRIPTION (Continued)

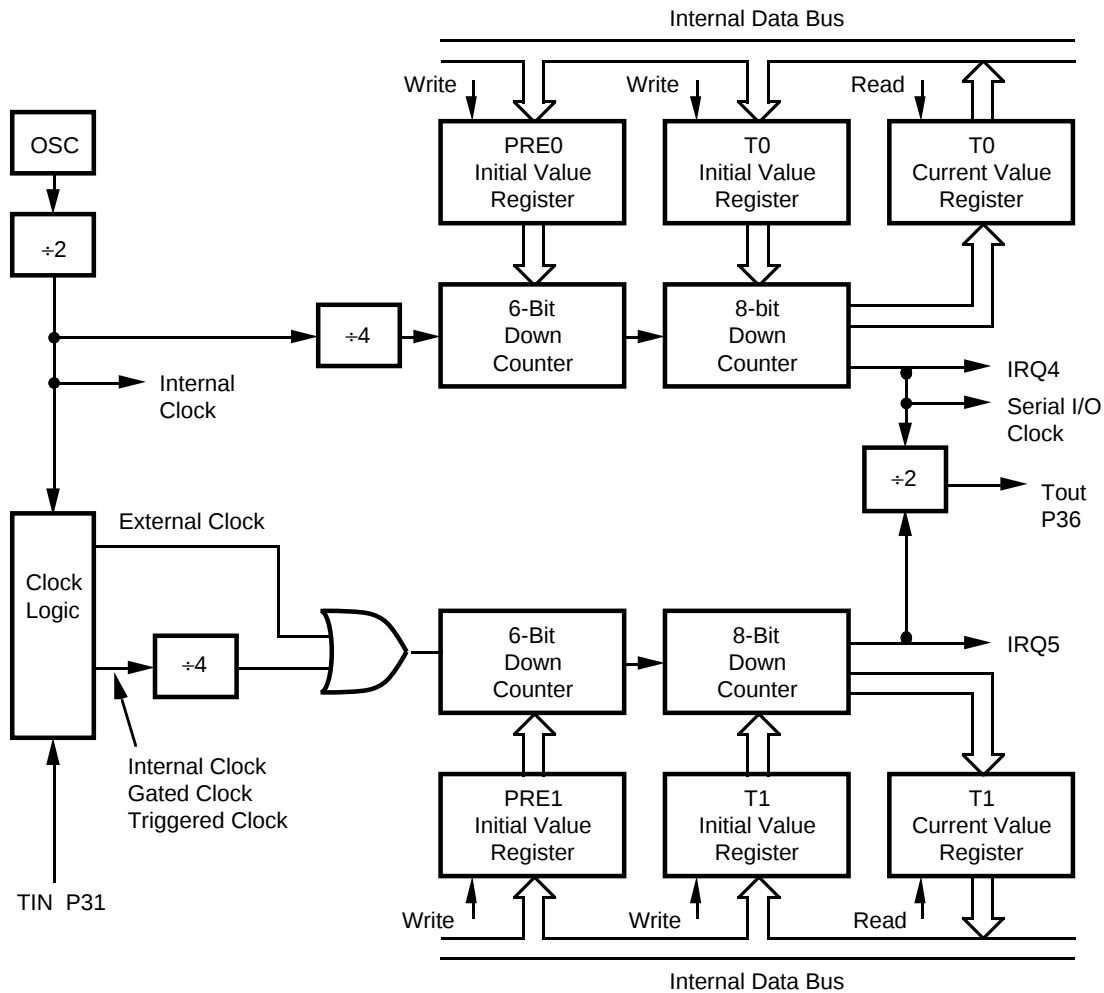


Figure 22. Counter/Timers Block Diagram

Interrupts. The Z86C61/62/96 has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The eight sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, one in Serial Out, one is Serial In, and two in the counter/timers (Figure 23). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86C61/62/96 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initiated interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction. The interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

For the ROMless mode, when the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register onto the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

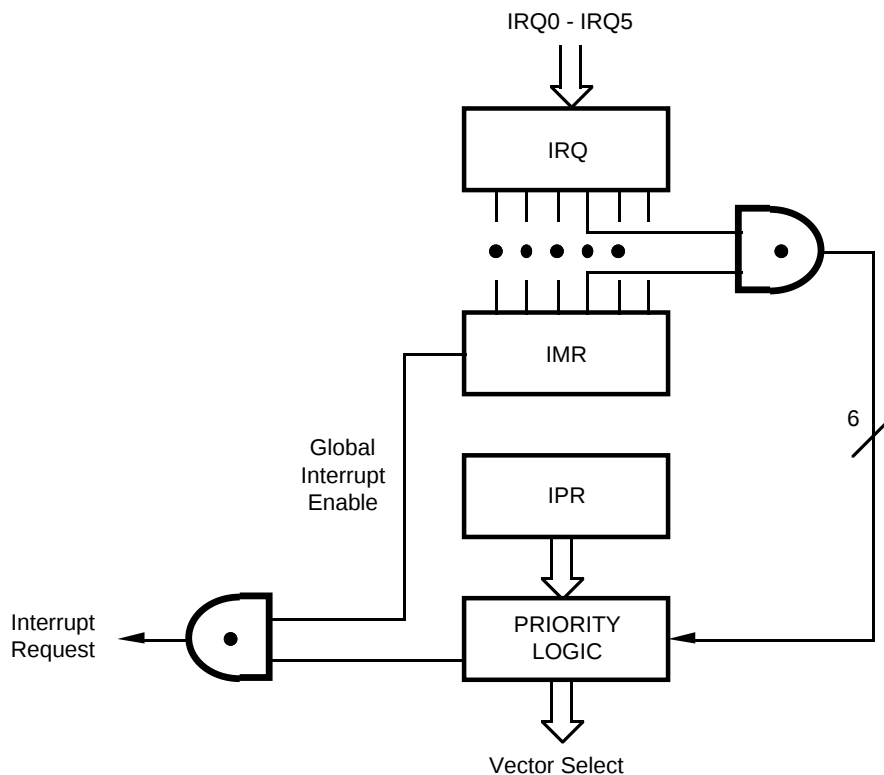


Figure 23. Interrupt Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Clock. The Z86C61/62/96 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 20 MHz max, and series resistance (RS) is less than or equal to 100 Ohms. The

crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors ($10\text{ pF} < C_L < 100\text{ pF}$) from each pin to device ground (Figure 24).

Note: Actual capacitor values specified by the crystal manufacturer.

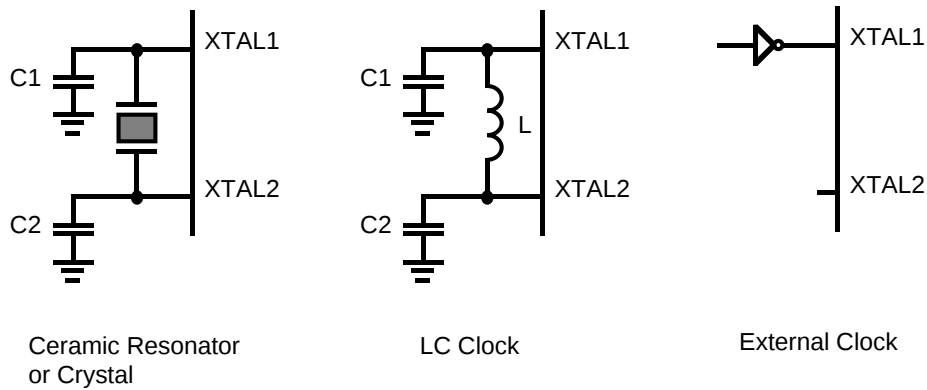


Figure 24. Oscillator Configuration

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and the external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to $5\text{ }\mu\text{A}$ (typical) or less. The STOP mode is terminated by a reset, which causes the processor to restart the application program at address 000CH.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=0FFH) immediately before the appropriate sleep instruction, i.e.,

FF	NOP	; clear the pipeline
6F	STOP	; enter STOP mode
		or
FF	NOP	; clear the pipeline
7F	HALT	; enter HALT mode

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	-0.3	+7.0	V
T_{STG}	Storage Temp	-65	+150	C
T_A	Oper Ambient Temp	†	†	

Notes:

* Voltages on all pins with respect to GND.

† See ordering information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 25).

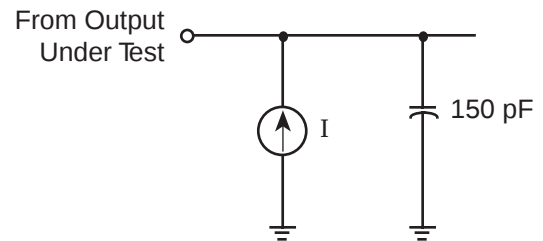


Figure 25. Test Load Diagram

DC ELECTRICAL CHARACTERISTICS

Z86C61/62/96

Sym	Parameter	$T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$		$T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$		Typical @ 25°C	Units	Conditions
		Min	Max	Min	Max			
	Max Input Voltage		7		7		V	$I_{IN} < 250 \mu\text{A}$
V_{CH}	Clock Input High Voltage	$0.85 V_{CC}$	$V_{CC} + 0.3$	$0.85 V_{CC}$	$V_{CC} + 0.3$		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	$V_{SS} - 0.3$	0.8	$V_{SS} - 0.3$	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2	$V_{CC} + 0.3$	2	$V_{CC} + 0.3$		V	
V_{IL}	Input Low Voltage	$V_{SS} - 0.3$	$0.2 V_{CC}$	$V_{SS} - 0.3$	$0.2 V_{CC}$		V	
V_{OH}	Output High Voltage	2.4		2.4			V	$I_{OH} = -2.0 \text{ mA}$
V_{OH}	Output High Voltage		$V_{CC} - 100 \text{ mV}$		$V_{CC} - 100 \text{ mV}$		V	$I_{OH} = -100 \mu\text{A}$
V_{OL}	Output Low Voltage		0.4		0.4		V	$I_{OL} = +5.0 \text{ mA}$ [3]
V_{OL}	Output Low Voltage		0.6		0.6		V	$I_{OL} = +4.0 \text{ mA}$ [2]
V_{RH}	Reset Input High Voltage	$0.85 V_{CC}$	$V_{CC} + 0.3$	$0.85 V_{CC}$	$V_{CC} + 0.3$		V	
V_{RI}	Reset Input Low Voltage	-0.3	$0.2 V_{CC}$	-0.3	$0.2 V_{CC}$		V	
I_{IL}	Input Leakage	-2	2	-2	2		μA	$V_{IN} = 0 \text{ V}, V_{CC}$
I_{OL}	Output Leakage	-2	2	-2	2		μA	$V_{IN} = 0 \text{ V}, V_{CC}$
I_{IR}	Reset Input Current		-80		-80		μA	$V_{RL} = 0 \text{ V}$
I_{CC}	Supply Current		35		35	24	mA	[1] @ 16 MHz
I_{CC}	Supply Current		40		40	30	mA	[1] @ 20 MHz
I_{CC1}	Standby Current		15		15	4.5	mA	[1] HALT Mode $V_{IN} = 0 \text{ V}, V_{CC}$ @ 16 MHz
I_{CC2}	Standby Current		10		20	5	μA	[1] STOP Mode $V_{IN} = 0 \text{ V}, V_{CC}$
I_{ALL}	Auto Latch Low Current	-14	14	-20	20	5	μA	

Notes:

[1] All inputs driven to either 0V or V_{CC} , outputs floating.

[2] $V_{CC} = 3.0\text{V}$ to 3.6V

[3] $V_{CC} = 4.5\text{V}$ to 5.5V

AC CHARACTERISTICS

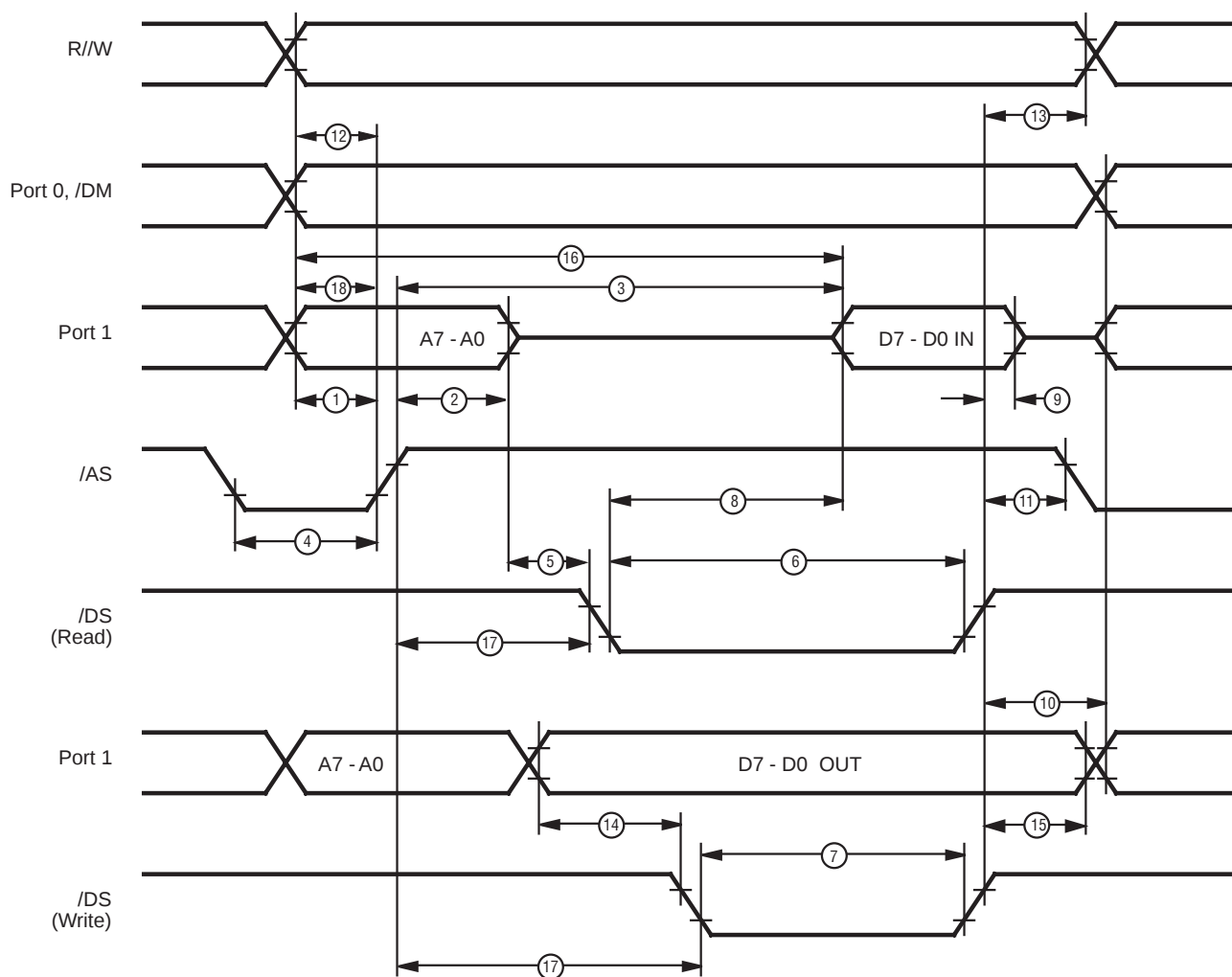


Figure 26. External I/O or Memory Read/Write

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing
Z86C61/62/96 (16 MHz)

No	Symbol	Parameter	$T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ 16 MHz		$T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$ 16 MHz		Units	Notes
			Min	Max	Min	Max		
1	TdA(AS)	Address Valid to /AS rise Delay	25		25		ns	[2,3]
2	TdAS(A)	/AS rise to Address Float Delay	35		35		ns	[2,3]
3	TdAS(DR)	/AS rise to Read Data Req'd Valid		150		150	ns	[1,2,3]
4	TwAS	/AS Low Width	40		40		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS fall	0		0		ns	
6	TwDSR	/DS (Read) Low Width		135		135	ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	80		80		ns	[1,2,3]
8	TdDSR(DR)	/DS fall to Read Data Req'd Valid	75		75		ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS rise Hold Time	0		0		ns	[2,3]
10	TdDS(A)	/DS rise to Address Active Delay	50		50		ns	[2,3]
11	TdDS(AS)	/DS rise to /AS fall Delay	35		35		ns	[2,3]
12	TdR/W(AS)	R/W Valid to /AS rise Delay	25		25		ns	[2,3]
13	TdDS(R/W)	/DS rise to R/W Not Valid	35		35		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS fall (Write) Delay	25		25		ns	[2,3]
15	TdDS(DW)	/DS rise to Write Data Not Valid Delay	35		35		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		210		210	ns	[1,2,3]
17	TdAS(DS)	/AS rise to /DS fall Delay	45		45		ns	[2,3]
18	TdDM(AS)	/DM Valid to /AS rise Delay	25		25		ns	[2,3]

Notes:

[1] When using extended memory timing add 2 TpC.

[2] Timing numbers given are for minimum TpC.

[3] See clock cycle dependent characteristics table.

Standard Test Load

All timing references use 2.0 V for a logic 1 and 0.8 V for a logic 0.

Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	$0.40 \text{ TpC} + 0.32$
2	TdAS(A)	$0.59 \text{ TpC} - 3.25$
3	TdAS(DR)	$2.83 \text{ TpC} + 6.14$
4	TwAS	$0.66 \text{ TpC} - 1.65$
6	TwDSR	$2.33 \text{ TpC} - 10.56$
7	TwDSW	$1.27 \text{ TpC} + 1.67$
8	TdDSR(DR)	$1.97 \text{ TpC} - 42.5$
10	TdDS(A)	0.8 TpC
11	TdDS(AS)	$0.59 \text{ TpC} - 3.14$
12	TdR/W(AS)	0.4 TpC
13	TdDS(R/W)	$0.8 \text{ TpC} - 15$
14	TdDW(DSW)	0.4 TpC
15	TdDS(DW)	$0.88 \text{ TpC} - 19$
16	TdA(DR)	$4 \text{ TpC} - 20$
17	TdAS(DS)	$0.91 \text{ TpC} - 10.7$
18	TdDM(AS)	$0.9 \text{ TpC} - 26.3$

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing
Z86C61/62/96 (20 MHz)

No	Symbol	Parameter	T _A = 0°C to +70°C 20 MHz		T _A = -40°C to +105°C 20 MHz		Units	Notes
			Min	Max	Min	Max		
1	TdA(AS)	Address Valid to /AS rise Delay	15		25		ns	[2,3]
2	TdAS(A)	/AS rise to Address Float Delay	25		35		ns	[2,3]
3	TdAS(DR)	/AS rise to Read Data Req'd Valid		120		120	ns	[1,2,3]
4	TwAS	/AS Low Width	30		30		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS fall	0		0		ns	
6	TwDSR	/DS (Read) Low Width		105		105	ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	65		65		ns	[1,2,3]
8	TdDSR(DR)	/DS fall to Read Data Req'd Valid	55		55		ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS rise Hold Time	0		0		ns	[2,3]
10	TdDS(A)	/DS rise to Address Active Delay	40		40		ns	[2,3]
11	TdDS(AS)	/DS rise to /AS fall Delay	25		25		ns	[2,3]
12	TdR/W(AS)	R/W Valid to /AS rise Delay	20		20		ns	[2,3]
13	TdDS(R/W)	/DS rise to R/W Not Valid	25		25		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS fall (Write) Delay	20		20		ns	[2,3]
15	TdDS(DW)	/DS rise to Write Data Not Valid Delay	25		25		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		150		150	ns	[1,2,3]
17	TdAS(DS)	/AS rise to /DS fall Delay	35		35		ns	[2,3]
18	TdDM(AS)	/DM Valid to /AS rise Delay	15		15		ns	[2,3]

Notes:

[1] When using extended memory timing add 2 TpC.

[2] Timing numbers given are for minimum TpC.

[3] See clock cycle dependent characteristics table.

AC CHARACTERISTICS

Additional Timing Diagram

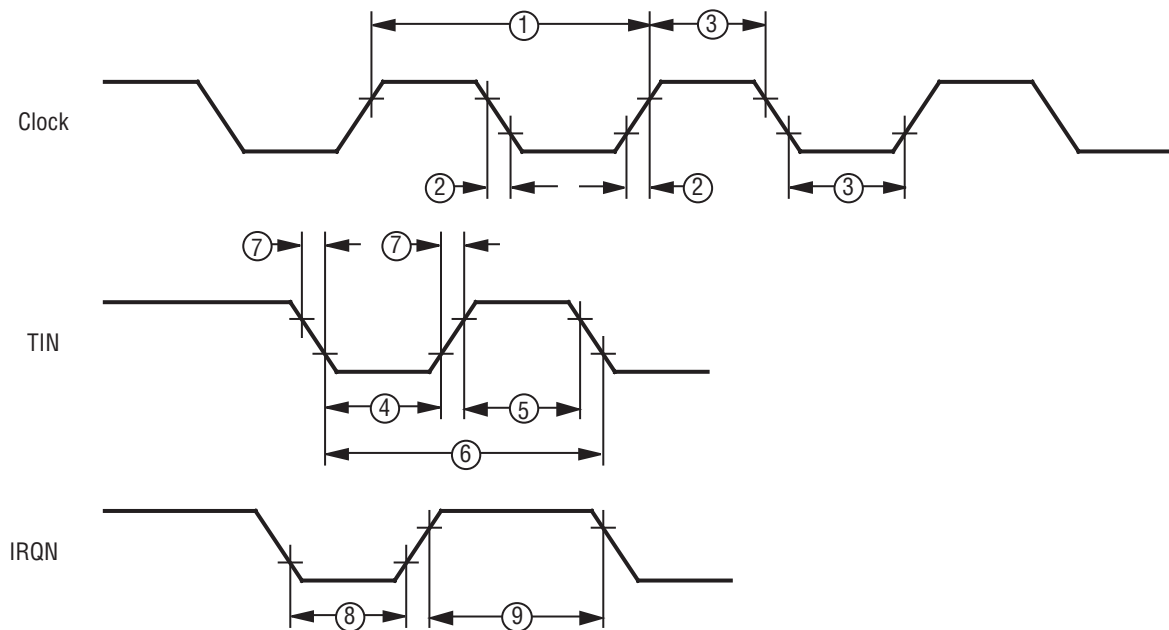


Figure 27. Additional Timing

AC CHARACTERISTICS

Additional Timing Table

Z86C61/62/96

No	Symbol	Parameter	$T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ 20/16 MHz		$T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$ 20/16 MHz		Units	Notes
			Min	Max	Min	Max		
1	TpC	Input Clock Period	50/62.5	1000	50/62.5	1000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		10	10		ns	[1]
3	TwC	Input Clock Width	25		25		ns	[1]
4	TwTinL	Timer Input Low Width	75		75		ns	[2]
5	TwTinH	Timer Input High Width	5 TpC		5 TpC		ns	[2]
6	TpTin	Timer Input Period	8 TpC		8 TpC		ns	[2]
7	TrTin,TfTin	Timer Input Rise and Fall Times	100		100		ns	[2]
8a	TwIL	Interrupt Request Input Low Times	70		50		ns	[2,4]
8b	TwIL	Interrupt Request Input Low Times	5 TpC		5 TpC		ns	[2,5]
9	TwIH	Interrupt Request Input High Times	5 TpC		5 TpC		ns	[2,3]

Notes:

[1] Clock timing references use $0.8V_{CC}$ for a logic 1 and $0.8V$ for a logic 0.

[2] Timing references use $2.0V$ for a logic 1 and $0.8V$ for a logic 0.

[3] Interrupt references request through Port 3.

[4] Interrupt request through Port 3 (P33-P31).

[5] Interrupt request through Port 30.

AC CHARACTERISTICS

Handshake Timing Diagrams

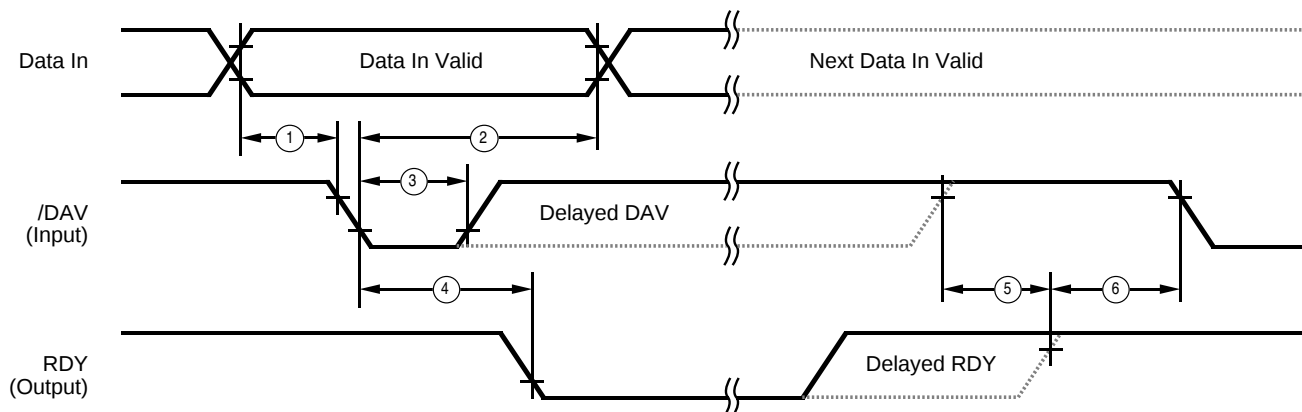


Figure 28. Input Handshake Timing

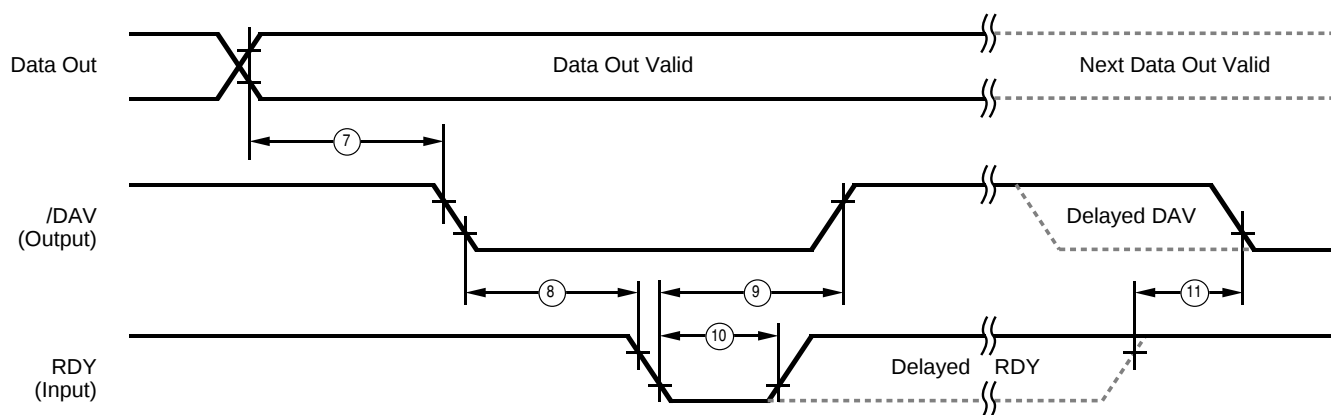


Figure 29. Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Table

Z86C61/62/96

No	Symbol	Parameter	$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ 20/16 MHz		$T_A = -40^{\circ}\text{C to } +105^{\circ}\text{C}$ 20/16 MHz		Data Direction
			Min	Max	Min	Max	
1	TsDI(DAV)	Data In Setup Time	0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		IN
3	TwDAV	Data Available Width	110		110		IN
4	TdDAVI(RDY)	DAV fall to RDY fall Delay	115		115		IN
5	TdDAVIId(RDY)	DAV rise to RDY rise Delay	115		115		IN
6	TdRDY0(DAV)	RDY rise to DAV fall Delay	0		0		IN
7	TdDO(DAV)	Data Out to DAV fall Delay	TpC		TpC		OUT
8	TdDAV0(RDY)	DAV fall to RDY fall Delay	0		0		OUT
9	TdRDY0(DAV)	RDY fall to DAV rise Delay	115		115		OUT
10	TwRDY	RDY Width	110		110		OUT
11	TdRDY0d(DAV)	RDY rise to DAV fall Delay	115		115		OUT

Z8 CONTROL REGISTER DIAGRAMS

R240 SIO

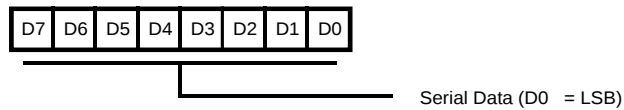


Figure 30. Serial I/O Register
(F0_H: Read/Write)

R241 TMR

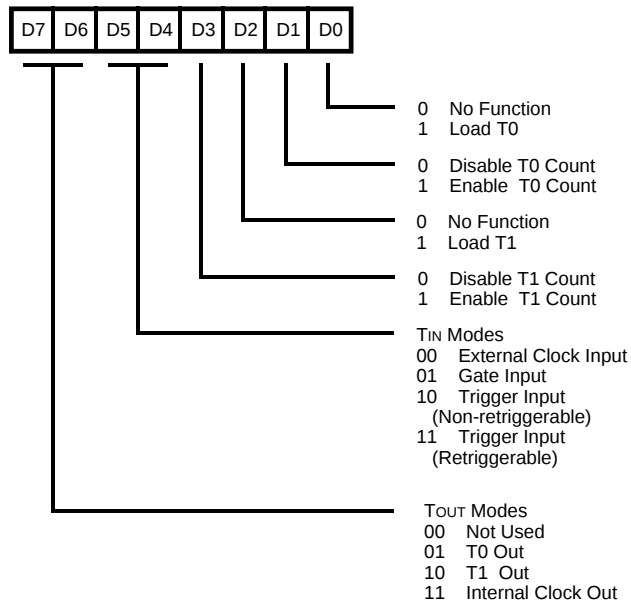


Figure 31. Timer Mode Register
(F1_H: Read/Write)

R242 T1

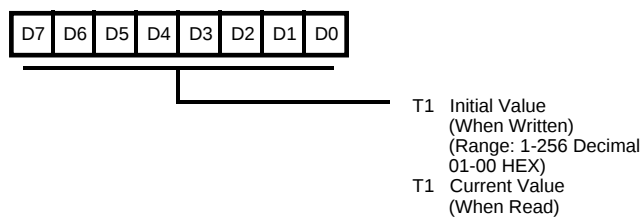


Figure 32. Counter/Timer 1 Register
(F2_H: Read/Write)

R243 PRE1

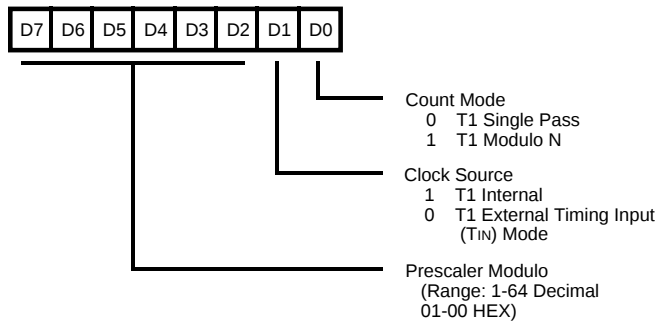


Figure 33. Prescaler 1 Register
(F3_H: Write Only)

R244 T0

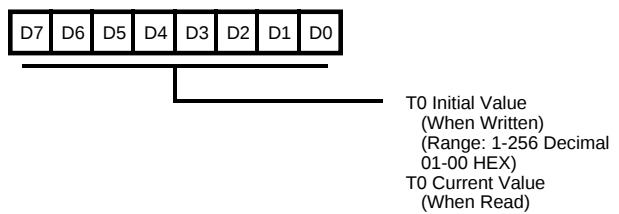


Figure 34. Counter/Timer 0 Register
(F4_H: Read/Write)

R245 PRE0

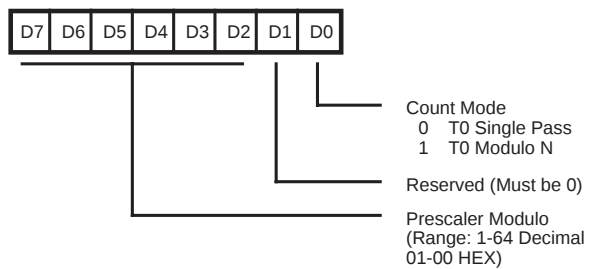


Figure 35. Prescaler 0 Register
(F5_H: Write Only)

R246 P2M



P20 - P27 I/O Definition
0 Defines Bit as Output
1 Defines Bit as Input

Figure 36. Port 2 Mode Register
(F6_H: Write Only)

R247 P3M



0 Port 2 Open Drain
1 Port 2 Push-pull
Reserved (Must be 0)
0 P32 = Input
P35 = Output
1 P32 = /DAV0/RDY0
P35 = RDY0//DAV0
00 P33 = Input
P34 = Output
01 } P33 = Input
P34 = /DM
10 } P33 = /DAV1/RDY1
P34 = RDY1//DAV1
11 }
0 P31 = Input (TIN)
P36 = Output (TOUT)
1 P31 = /DAV2/RDY2
P36 = RDY2//DAV2
0 P30 = Input
P37 = Output
1 P30 = Serial In
P37 = Serial Out
0 Parity Off
1 Parity On

Figure 37. Port 3 Mode Register
(F7_H: Write Only)

R248 P01M



P00 - P00 Mode
00 Output
01 Input
1X A11 - A8
Stack Selection
0 External
1 Internal
P17 - P10 Mode
00 Byte Output
01 Byte Input
10 AD7 - AD0
11 High-Impedance AD7 - DA0,
/AS, /DS, /R//W, A11 - A8,
A15 - A12, If Selected
Reserved (Must be 0)
P07 - P04 Mode
00 Output
01 Input
1X A15 - A12

Figure 38. Port 0 and 1 Mode Register
(F8_H: Write Only)

R249 IPR



Interrupt Group Priority
Reserved = 000
C > A > B = 001
A > B > C = 010
A > C > B = 011
B > C > A = 100
C > B > A = 101
B > A > C = 110
Reserved = 111
IRQ1, IRQ4 Priority (Group C)
0 IRQ1 > IRQ4
1 IRQ4 > IRQ1
IRQ0, IRQ2 Priority (Group B)
0 IRQ2 > IRQ0
1 IRQ0 > IRQ2
IRQ3, IRQ5 Priority (Group A)
0 IRQ5 > IRQ3
1 IRQ3 > IRQ5
Reserved (Must be 0)

Figure 39. Interrupt Priority Register
(F9_H: Write Only)

Z8 CONTROL REGISTER DIAGRAMS (Continued)

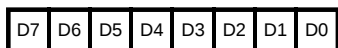
R250 IRQ



IRQ0 = P32 Input (D0 = IRQ0)
 IRQ1 = P33 Input
 IRQ2 = P31 Input
 IRQ3 = P30 Input, Serial Input
 IRQ4 = T0 Serial Output
 IRQ5 = T1
 Reserved (Must be 0)

Figure 40. Interrupt Request Register
(FA_H: Read/Write)

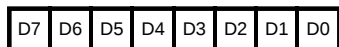
R251 IMR



1 Enables IRQ5-IRQ0
 (D0 = IRQ0)
 1 Enables RAM Protect
 1 Enables Interrupts

Figure 41. Interrupt Mask Register
(FB_H: Read/Write)

R252 FLAGS



User Flag F1
 User Flag F2
 Half Carry Flag
 Decimal Adjust Flag
 Overflow Flag
 Sign Flag
 Zero Flag
 Carry Flag

Figure 42. Flag Register
(FC_H: Read/Write)

R253 RP



Expanded Register Pointer
 Working Register Pointer

Figure 43. Register Pointer Register
(FD_H: Read/Write)

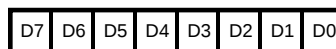
R254 SPH



Stack Pointer Upper
Byte (SP₁₅ - SP₈)

Figure 44. Stack Pointer Register
(FE_H: Read/Write)

R255 SPL

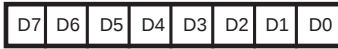


Stack Pointer Lower
Byte (SP₇ - SP₀)

Figure 45. Stack Pointer Register
(FF_H: Read/Write)

Z8 EXPANDED REGISTER FILE CONTROL REGISTERS

P4 (FH) 02H



Data
0 Defines Level 0
1 Defines Level 1

**Figure 46. Port 4 Data Register
(F)02: (Read/Write)**

P4M (FH) 03H



P40 - P47 I/O Definition
0 Defines Bit as Output
1 Defines Bit as Input

**Figure 47. Port 4 Direction Register
(F)03: (Write Only)**

P5 (FH) 04H



Data
0 Defines Level 0
1 Defines Level 1

**Figure 48. Port 5 Data Register
(F)04: (Read/Write)**

P5D (FH) 05H



P50 - P57 I/O Definition
0 Defines Bit as Output
1 Defines Bit as Input*

*Default Value After RESET

**Figure 49. Port 5 Direction Register
(F)05: (Write Only)**

P45M (FH) 06H

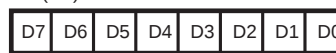


0 Port 4 Open-drain*
1 Port 4 Push-pull
Reserved (Must be 0)
0 Port 5 Open-drain*
1 Port 5 Push-pull
Reserved (Must be 0)

*Default Value After RESET

**Figure 50. Port 4/5 Mode Register
(F)06: (Write Only)**

P6 (FH) 07H



Data
0 Defines Level 0
1 Defines Level 1
Reserved (Must be 0)

**Figure 51. Port 6 Data Register
(F)07: (Read/Write)**

P6D (FH) 08H



P60 - P63 I/O Definition
0 Defines Bit as Output
1 Defines Bit as Input*
Reserved (Must be 0)

*Default Value After RESET

**Figure 52. Port 6 Direction Register
(F)08: (Write Only)**

P6M (FH) 09H



0 Port 6 Open-drain*
1 Port 6 Push-pull

*Default Value After RESET

**Figure 53. Port 6 Mode Register
(F)09: (Write Only)**

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag
Affected flags are indicated by:	
0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

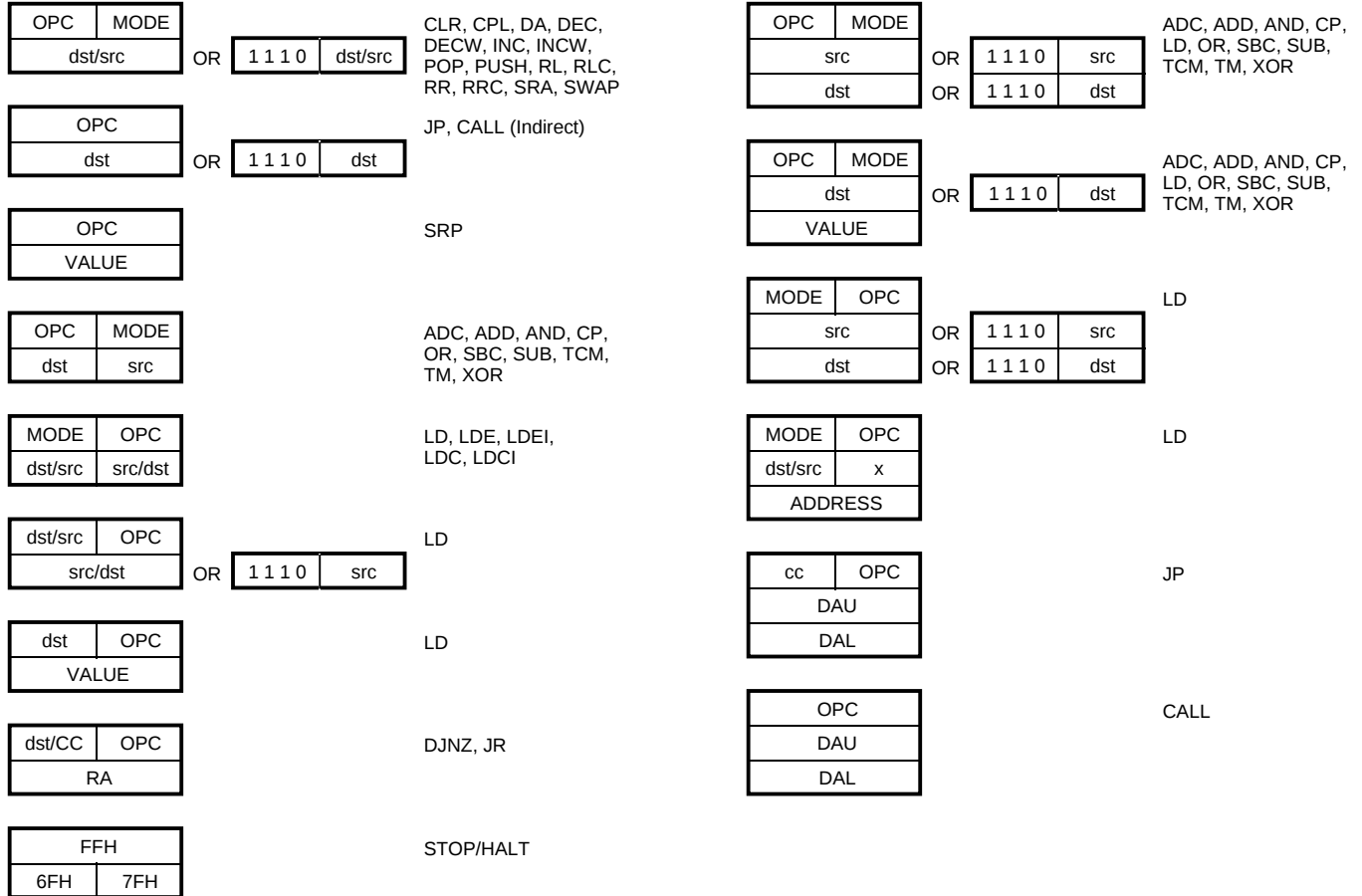
CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	

INSTRUCTION FORMATS



One-Byte Instructions



Two-Byte Instructions

Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol “←”. For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The

notation “addr (n)” is used to refer to bit (n) of a given operand location. For example:

dst (7)

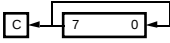
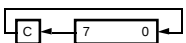
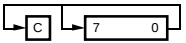
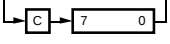
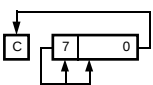
refers to bit 7 of the destination operand.

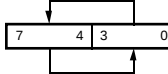
INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address		Opcode Byte (Hex)	Flags Affected						
	Mode	dst src		C	Z	S	V	D	H	
ADC dst, src dst←dst +src + C	†		1[]	*	*	*	*	0	*	
ADD dst, src dst←dst +src	†		0[]	*	*	*	*	0	*	
AND dst, src dst←dst AND src	†		5[]	-	*	*	0	-	-	
CALL dst SP←SP – 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-	
CCF C←NOT C			EF	*	-	-	-	-	-	
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-	
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-	
CP dst, src dst – src	†		A[]	*	*	*	*	-	-	
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-	
DEC dst dst←dst – 1	R IR		00 01	-	*	*	*	-	-	
DECW dst dst←dst – 1	RR IR		80 81	-	*	*	*	-	-	
DI IMR(7)←0			8F	-	-	-	-	-	-	
DJNZ r, dst r←r – 1 if r ≠ 0 PC←PC +dst Range: +127, –128	RA		rA r = 0 – F	-	-	-	-	-	-	
EI IMR(7)←1			9F	-	-	-	-	-	-	
HALT			7F	-	-	-	-	-	-	

Instruction and Operation	Address		Opcode Byte (Hex)	Flags Affected						
	Mode	dst src		C	Z	S	V	D	H	
INC dst dst←dst + 1	r R IR		rE r = 0 – F 20 21	-	*	*	*	-	-	
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-	
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*	
JP cc, dst if cc is true PC←dst	DA IRR		cD c = 0 – F 30	-	-	-	-	-	-	
JR cc, dst if cc is true, PC←PC +dst Range: +127, –128	RA		cB c = 0 – F	-	-	-	-	-	-	
LD dst, src dst←src	r r R r X r r lr lr R R R R IR IR IR	lm R r X r lr r r R R R R IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-	
LDC dst, src	r	lrr	C2	-	-	-	-	-	-	
LDCI dst, src dst←src r←r +1; rr←rr +1	lr	lrr	C3	-	-	-	-	-	-	

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode		Opcode Byte (Hex)	Flags Affected							
	dst	src		C	Z	S	V	D	H		
NOP			FF	-	-	-	-	-	-	-	-
OR dst, src dst←dst OR src	†		4[]	-	*	*	0	-	-	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-	-	-
PUSH src SP←SP - 1; @SP←src		R IR	70 71	-	-	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-	-	-
SBC dst, src dst←dst←src←C	†		3[]	*	*	*	*	1	*	*	*
SCF C←1			DF	1	-	-	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-	-	-
SRP src RP←src		Im	31	-	-	-	-	-	-	-	-

Instruction and Operation	Address Mode		Opcode Byte (Hex)	Flags Affected							
	dst	src		C	Z	S	V	D	H		
STOP			6F	-	-	-	-	-	-	-	-
SUB dst, src dst←dst←src	†		2[]	*	*	*	*	1	*	*	*
SWAP dst 	R IR		F0 F1	X	*	*	X	-	-	-	-
TCM dst, src (NOT dst) AND src	†		6[]	-	*	*	0	-	-	-	-
TM dst, src dst AND src	†		7[]	-	*	*	0	-	-	-	-
XOR dst, src dst←dst XOR src	†		B[]	-	*	*	0	-	-	-	-

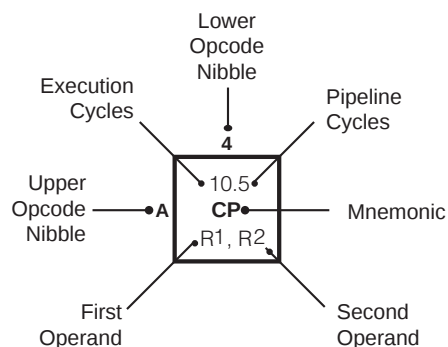
† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode		Lower Opcode Nibble
dst	src	
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

		Lower Nibble (Hex)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Upper Nibble (Hex)	0	6.5 DEC R1	6.5 DEC IR1	6.5 ADD r1, r2	6.5 ADD r1, Ir2	10.5 ADD R2, R1	10.5 ADD IR2, R1	10.5 ADD R1, IM	10.5 ADD IR1, IM	6.5 LD r1, R2	6.5 LD r2, R1	12/10.5 DJNZ r1, RA	12/10.0 JR cc, RA	6.5 LD r1, IM	12.10.0 JP cc, DA	6.5 INC r1	
	1	6.5 RLC R1	6.5 RLC IR1	6.5 ADC r1, r2	6.5 ADC r1, Ir2	10.5 ADC R2, R1	10.5 ADC IR2, R1	10.5 ADC R1, IM	10.5 ADC IR1, IM								
	2	6.5 INC R1	6.5 INC IR1	6.5 SUB r1, r2	6.5 SUB r1, Ir2	10.5 SUB R2, R1	10.5 SUB IR2, R1	10.5 SUB R1, IM	10.5 SUB IR1, IM								
	3	8.0 JP IRR1	6.1 SRP IM	6.5 SBC r1, r2	6.5 SBC r1, Ir2	10.5 SBC R2, R1	10.5 SBC IR2, R1	10.5 SBC R1, IM	10.5 SBC IR1, IM								
	4	8.5 DA R1	8.5 DA IR1	6.5 OR r1, r2	6.5 OR r1, Ir2	10.5 OR R2, R1	10.5 OR IR2, R1	10.5 OR R1, IM	10.5 OR IR1, IM								
	5	10.5 POP R1	10.5 POP IR1	6.5 AND r1, r2	6.5 AND r1, Ir2	10.5 AND R2, R1	10.5 AND IR2, R1	10.5 AND R1, IM	10.5 AND IR1, IM								
	6	6.5 COM R1	6.5 COM IR1	6.5 TCM r1, r2	6.5 TCM r1, Ir2	10.5 TCM R2, R1	10.5 TCM IR2, R1	10.5 TCM R1, IM	10.5 TCM IR1, IM								6.0 STOP
	7	10/12.1 PUSH R2	12/14.1 PUSH IR2	6.5 TM r1, r2	6.5 TM r1, Ir2	10.5 TM R2, R1	10.5 TM IR2, R1	10.5 TM R1, IM	10.5 TM IR1, IM								7.0 HALT
	8	10.5 DECW RR1	10.5 DECW IR1	12.0 LDE r1, Irr2	18.0 LDEI Ir1, Irr2												6.1 DI
	9	6.5 RL R1	6.5 RL IR1	12.0 LDE r2, Irr1	18.0 LDEI Ir2, Irr1												6.1 EI
	A	10.5 INCW RR1	10.5 INCW IR1	6.5 CP r1, r2	6.5 CP r1, Ir2	10.5 CP R2, R1	10.5 CP IR2, R1	10.5 CP R1, IM	10.5 CP IR1, IM								14.0 RET
	B	6.5 CLR R1	6.5 CLR IR1	6.5 XOR r1, r2	6.5 XOR r1, Ir2	10.5 XOR R2, R1	10.5 XOR IR2, R1	10.5 XOR R1, IM	10.5 XOR IR1, IM								16.0 IRET
	C	6.5 RRC R1	6.5 RRC IR1	12.0 LDC r1, Irr2	18.0 LDCI Ir1, Irr2				10.5 LD r1,x,R2								6.5 RCF
	D	6.5 SRA R1	6.5 SRA IR1	12.0 LDC r1, Irr2	18.0 LDCI Ir1, Irr2	20.0 CALL* IRR1		20.0 CALL DA	10.5 LD r2,x,R1								6.5 SCF
	E	6.5 RR R1	6.5 RR IR1		6.5 LD r1, IR2	10.5 LD R2, R1	10.5 LD IR2, R1	10.5 LD R1, IM	10.5 LD IR1, IM								6.5 CCF
	F	8.5 SWAP R1	8.5 SWAP IR1		6.5 LD Ir1, r2		10.5 LD R2, IR1										6.0 NOP
		2		3			2		3			1					
		Bytes per Instruction															



Legend:

R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

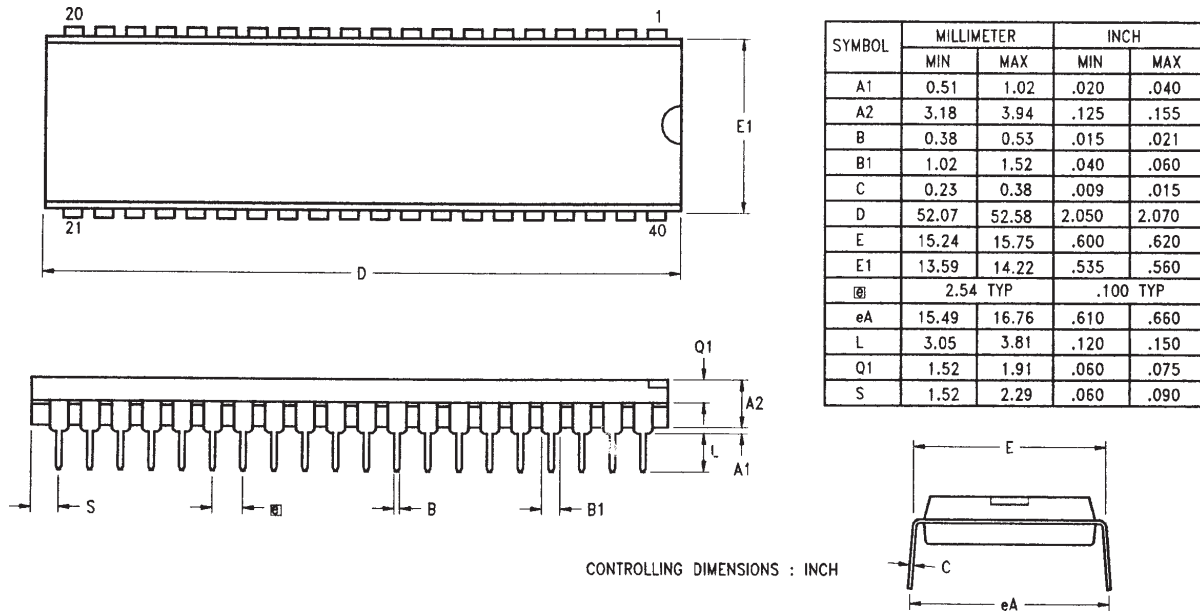
Sequence:

Opcode, First Operand,
Second Operand

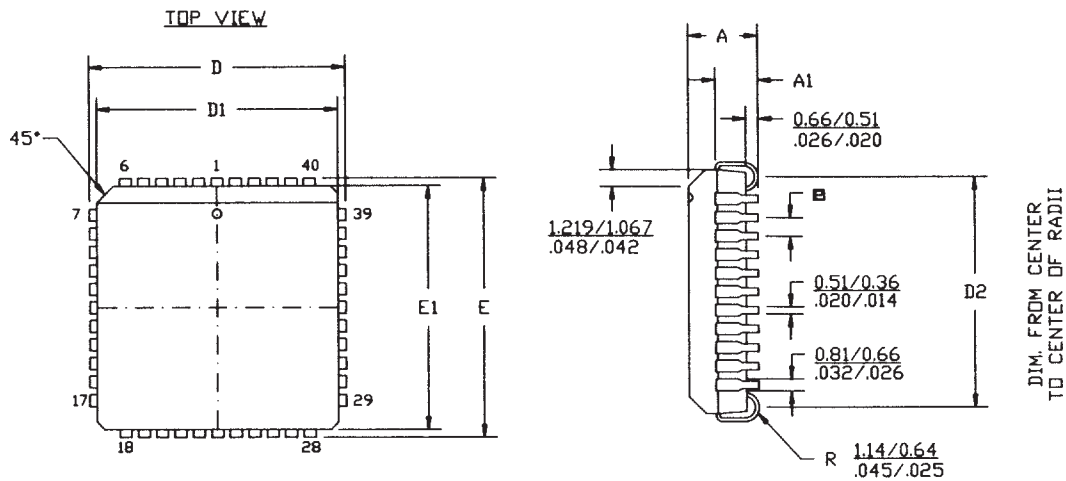
Note: Blank areas not defined.

*2-byte instruction appears as
a 3-byte instruction

PACKAGE INFORMATION



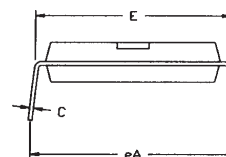
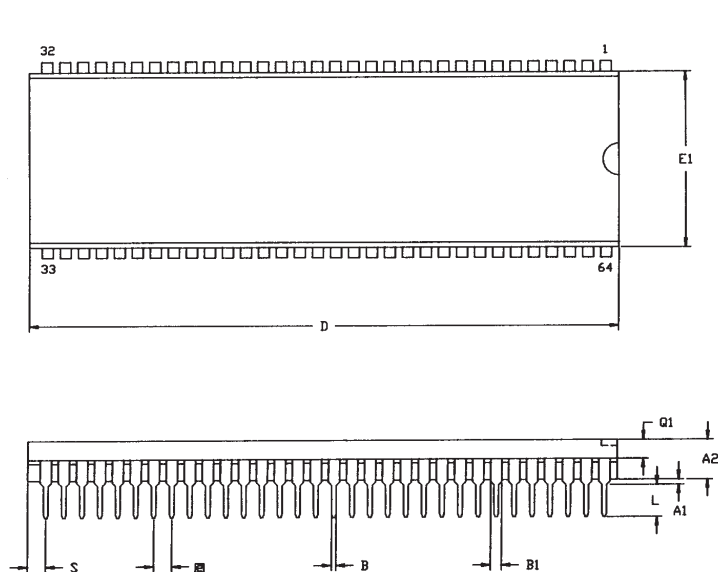
40-Pin Plastic DIP Package



NOTES:

1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : $\frac{\text{MM}}{\text{INCH}}$

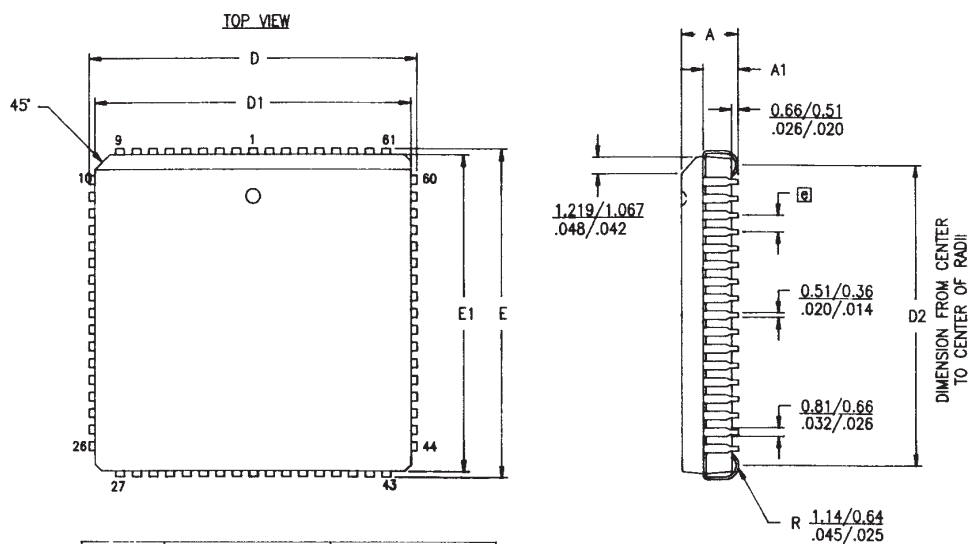
44-Pin PLCC Package



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.38	1.07	.015	.042
A2	3.68	3.94	.145	.155
B	0.38	0.53	.015	.021
B1	0.94	1.09	.037	.043
C	0.23	0.38	.009	.015
D	57.40	58.17	2.260	2.290
E	18.80	19.30	.740	.760
E1	16.76	17.27	.660	.680
□	1.78	TYP	.070	TYP
eA	19.30	20.32	.760	.800
L	3.18	3.81	.125	.150
Q1	1.65	1.91	.065	.075
S	1.02	1.78	.040	.070

CONTROLLING DIMENSIONS : INCH

64-Pin Plastic DIP Package



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.32	4.57	.170	.180
A1	2.43	2.92	.095	.115
D/E	25.02	25.40	.985	1.000
D1/E1	24.13	24.33	.950	.958
D2	22.86	23.62	.900	.930
□	1.27	TYP	.050	TYP

NOTES:

1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN RANGE.
3. DIMENSION : $\frac{\text{MM}}{\text{INCH}}$

68-Pin PLCC Package

ORDERING INFORMATION

Z86C61/62/96

16 MHz

40-pin DIP

Z86C6116PSC

44-pin PLCC

Z86C6116VSC

44-pin QFP

Z86C6116FSC

16 MHz

64-pin DIP

Z86C6216PSC

68-pin PLCC

Z86C6216VSC

20 MHz

64-pin DIP

Z86C9620PSC

68-pin PLCC

Z86C9620VSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

CODES

Package

P = Plastic DIP

V = Plastic Chip Carrier

Preferred Temperature

S = 0°C to +70°C

Longer Lead Time

E = -40°C to +105°C

Speeds

16 = 16 MHz

20 = 20 MHz

Environmental

C = Plastic Standard

Example:

Z 86C61 16 P S C is an 86C61, 16 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

