CALISTO™ VoP PRODUCT Brief

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CALISTO VoP SOLUTION

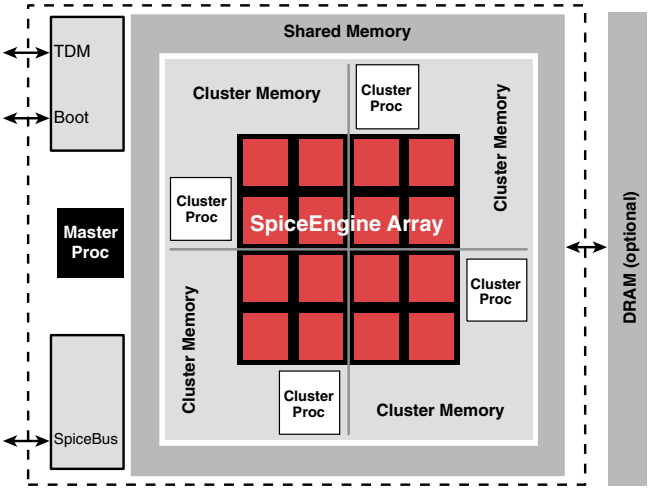
CALISTO VoP FEATURES

- **Gateway xChange field-hardened software integrated with the CALISTO communication processor**
- **Gateway xChange software provides:**
  - Packet voice
  - Line echo cancellation with 16–128 ms tail length
    - VAD/CNG
    - Voice compression: G.711 µ-law/A-law PCM 64 Kbps, G.726 16/24/32/40 Kbps, G.729A/B 8 Kbps, G.729E 11.8 Kbps, G.723.1/A 5.3/6.3 Kbps, G.728 16 Kbps
  - Dynamic jitter buffer manager for all services
  - Fax relay
    - Fax synchronization
    - T.38 relay and fax over AAL2
    - Data pumps: V.17 14400 bps, V.29 9600 bps, V.27ter
  - Data relay
    - Data synchronization
    - Data pumps: V.34 33600 bps, V.32bis/V.32 14400 bps, V.22bis/V.22 2400 bps
  - Signaling relay: DTMF, MF-R1, Type 1 Caller ID, and CPM/CPG
  - Robust API
- **BCM1500/1510 chip**
  - 21 processing units per chip: 16 SpiceEngines™ and 5 RISC processors
  - 8 physical interfaces: 2 TDM ports, 2 SpiceBus ports, SDRAM port, JTAG port, SPI serial boot port, and PLL port
  - 19-mm, 239-ball ceramic fine-pitch BGA
  - Reconfigurable-adaptive instruction sets
  - Over 3.3 GMACs of signal processing power
  - C compiler and robust Integrated Development Environment (IDE) included

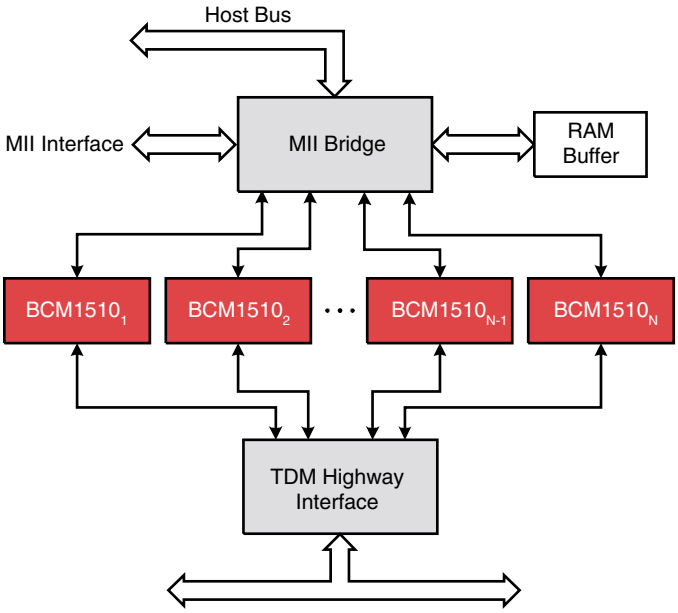
SUMMARY OF BENEFITS

- **HausWare Framework's RTOS provides the ability to dynamically configure the system for over 200 channels of carrier class G.711 or 60 channels of full universal port processing.**
- **Includes field-hardened Gateway xChange services.**
- **Open platform provides customers with the flexibility to customize the solutions by adding their own unique services.**
- **Enables toll-quality voice.**
- **Shorten product development time with CALISTO GUI-based tools suite:**
  - Industry-leading optimizing C compiler
  - Assembler
  - Linker
  - Debugger with cycle-accurate simulator and profiler
  - Unique multichannel, multiservice debug paradigm
  - Remote debug capability
- **Reference design platform and training is available for testing and customization projects.**

CALISTO Architecture



CALISTO Sub-system Diagram



CALISTO BCM1500/1510 Architecture

The CALISTO architecture employs reconfigurable-adaptive instruction sets, hierarchical DSP multi-processing, and a hybrid RISC/DSP implementation to provide over 3.3 GMACS of signal processing horsepower (that's over 200 packet telephony channels per chip). This unique architecture enables the convergence of voice and data services over a unified data network with the highest voice density per square inch, and per watt, in the industry.

CALISTO was explicitly designed to meet and to exceed the current and future challenges of complex packet processing, signal processing, and high-speed memory requirements for carrier and broadband access networks. Working with the Gateway xChange suite of VoP services, CALISTO manages all of the compute-intensive tasks such as echo cancellation, voice and fax/data modem signal processing, packetization, transformation of data into cells, delay equalization, and telephony protocols within packet telephony applications including carrier gateways, broadband access gateways, and remote access concentrators.

All of this power is packed into a 19-mm, 239-ball ceramic fine-pitch BGA.

Chip Interfaces

- Two line-side TDM ports provide glueless connection to off-the-shelf framers and MVIP switches.
- Two packet-side full-duplex SpiceBus ports, running at up to 50 MHz, provide efficient connection to the backplane.
- One SDRAM port provides a 32-bit-wide data path capable of running at 166 MHz.
- One serial boot port provides a standard Serial Peripheral Interface (SPI) running at up to 5 MHz.
- One standard test access port provides support for JTAG IEEE 1149.1.
- One internal PLL provides core frequencies of up to 166 MHz.

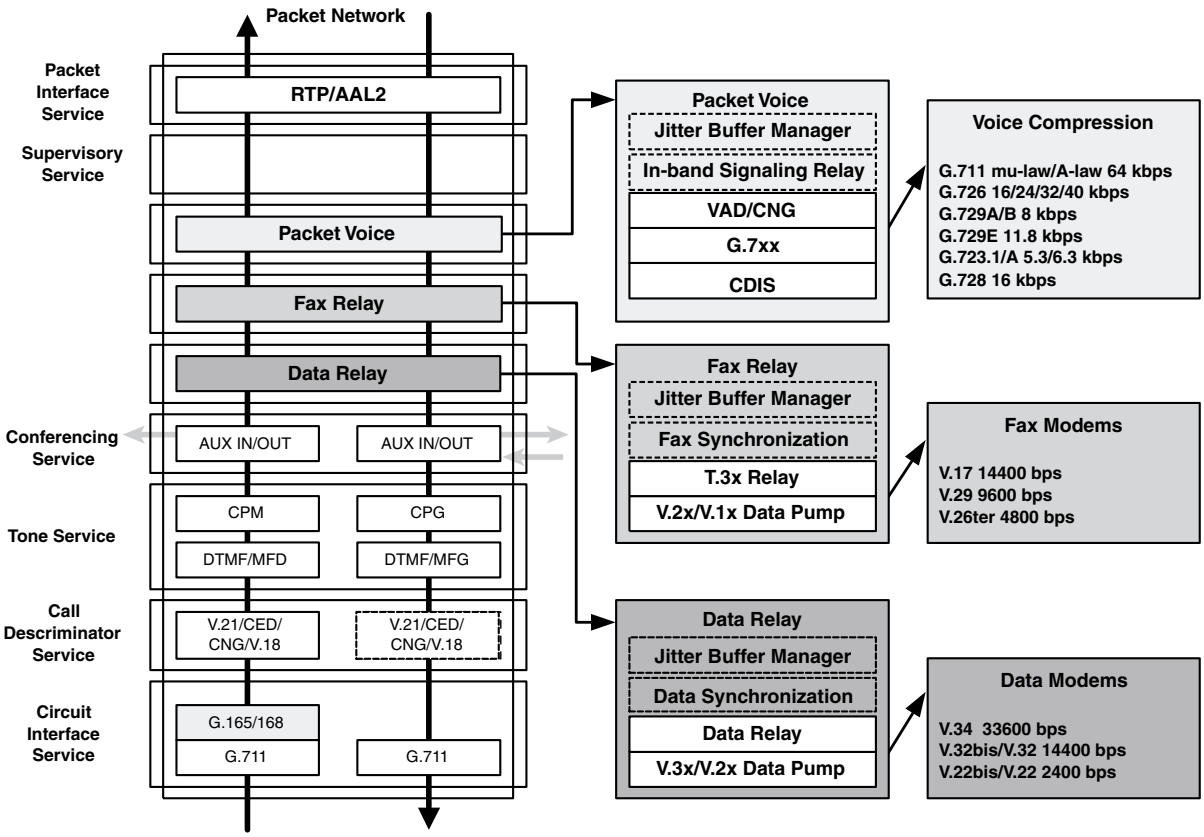
CALISTO Subsystem

The preceding figure shows a CALISTO-based subsystem capable of handling an OC-3 (2016 DS0). Each CALISTO pushes data towards the system interface, the SpiceBus, thus eliminating the need for host-assisted DMA from shared memory, and allowing the use of efficient aggregation devices, the SpiceBridges. Each SpiceBridge aggregates, in a single step, control and data traffic from up to eight CALISTO devices towards the system backplane. Broadcom provides several flavors of the SpiceBridge as flexible logic cores.

For example, the Bridge in the preceding figure, the CALISTO MII (Media Independent Interface) Bridge, supports FPGA implementation of the MII to the CALISTO BCM1500/1510 carrier-access architecture. A device built around this logic core can bridge up to eight BCM1500/1510s to a single MII interface. The MII SpiceBridge enables the design of high density Voice over IP subsystems.

The CALISTO MII Bridge is integral to Broadcom's multichannel, multiservice, carrier-access architecture. By handling packet-side control and data flows, the bridge supports flexible integration of circuit-switched and packet-switched networks. As a Broadcom-supported Verilog block, the CALISTO MII Bridge can be quickly reconfigured to meet changing customer requirements.

Gateway xChange on CALISTO



Gateway xChange VoP software in conjunction with the CALISTO BCM1500/1510 enables the highest density processing of voice/fax/data over packet networks in the industry.

xChange Services

The **Circuit Interface Service** (PCM or AAL1) supports G.711 µ-law/A-law, hosts G.168 echo cancellation with 32/64/128 ms tail lengths, detects and generates idle patterns, initializes linear ingress and egress media buffers, stores ingress/egress history, provides loopback towards circuit or packet network, provides gain control on ingress/egress samples, and provides energy measurement of ingress media.

The **Call Discrimination Service** (CDIS) hosts fax/modem/V.18 detection, allows detection events to be used by the supervisory service to reconfigure the channel, and runs in either the ingress or egress direction.

The **Tone Service** (PTE) detects DTMF, MF, and PTP tones, and incorporates programmable tone generation in packet or TDM direction, with features to support special tones like calling cards.

The **Conferencing Service** transmits samples to another channel, receives samples and sums with local data, and includes an aggregation channel to provide support for larger conferences.

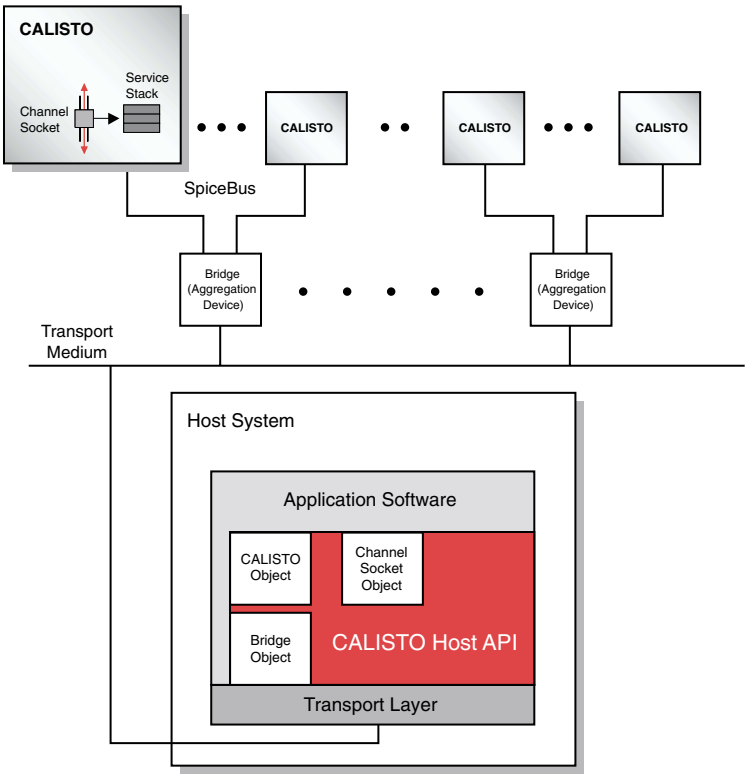
The **Packet Voice Service** (PVE) incorporates an adaptable/configurable jitter buffer, vocoders, and VAD/CNG; supports asymmetric encode/decode; provides G.711, G.726, G.729A/B/E, G.728, G.723.1, AMR, and GSM/EFR algorithms, with 5-ms packetizations for G.711, G.726, and G.278; allows super-packetization of up to eight frames, reorders packets in the jitter buffer, provides jitter buffer statistics, includes a packet loss concealment algorithm, provides egress VAD for jitter buffer adaptation control (in the absence of arriving SIDS) and for noise level/spectrum matching; supports voice band data mode, with clock drift compensation, for modem/fax pass-through.

The **Fax Relay Service** accepts T.38 or AAL2 packet formats, supports V.21, V.27ter, V.29, V.17 and V.33 data algorithms, incorporates end-of-line spoofing for non-ECM calls and HDLC spoofing for V.21 and ECM calls and supports both T.32 Data Rate Management methods.

The **Supervisory Service** intercepts and filters events generated by services, and provides a high-level control interface.

The **Packet Interface Service** supports either RTP/UDP/IP or AAL1/AAL2 packet encapsulation, converts from internal packet headers to protocol-specific headers, sends and receives data on the packet interface, provides support for loopback towards circuit or packet network.

Scalable System Design



CALISTO Host API

The CALISTO Host API is a C-language, re-entrant library that lets multi-threaded applications control CALISTO and SpiceBridge devices. The library is implemented in the ANSI standard C programming language, and is protected from the underlying operating system by an OS abstraction layer.

The library can be ported between operating systems and host platforms. As a library, the CALISTO Host API always executes in task contexts provided by the application software.

The CALISTO Host API allows users to embed CALISTO and SpiceBridge products into custom hardware architectures. The API provides C language software objects that correspond to the hardware components, and can be tied together to reflect the architecture of the custom system. The object-oriented design provides the flexibility to add to and to expand the API as capability is added to CALISTO, or when new hardware devices become available.

Users can place the library objects into tables maintained by call management applications, or add system-specific data to the objects so that they themselves become the table entries. The objects encapsulate addressing and state data to provide a flexible and scalable data organization.

The object-oriented approach also lets the API manage state for related objects. If users reset a CALISTO, all Channel Socket Objects associated with the CALISTO change state as well. This encapsulation assists users in managing connections, and in implementing a hot backup redundancy scheme.

For more information please contact us at:
Phone: 949-450-8700, FAX: 949-450-8710
Email: info@broadcom.com

Visit our web site at: www.broadcom.com

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BROADCOM CORPORATION
16215 Alton Parkway, P.O. Box 57013
Irvine, California 92619-7013