

IR2109(4) (S) & (PbF) HALF-BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
Fully operational to +600V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- High side output in phase with IN input
- Logic and power ground +/- 5V offset.
- Internal 540ns dead-time, and programmable
up to 5us with one external R_{DT} resistor (IR21094)
- Lower di/dt gate driver for better noise immunity
- Shut down input turns off both channels.
- Available in Lead-Free

Description

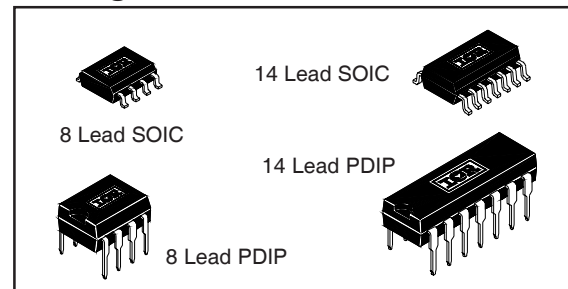
The IR2109(4)(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high

pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

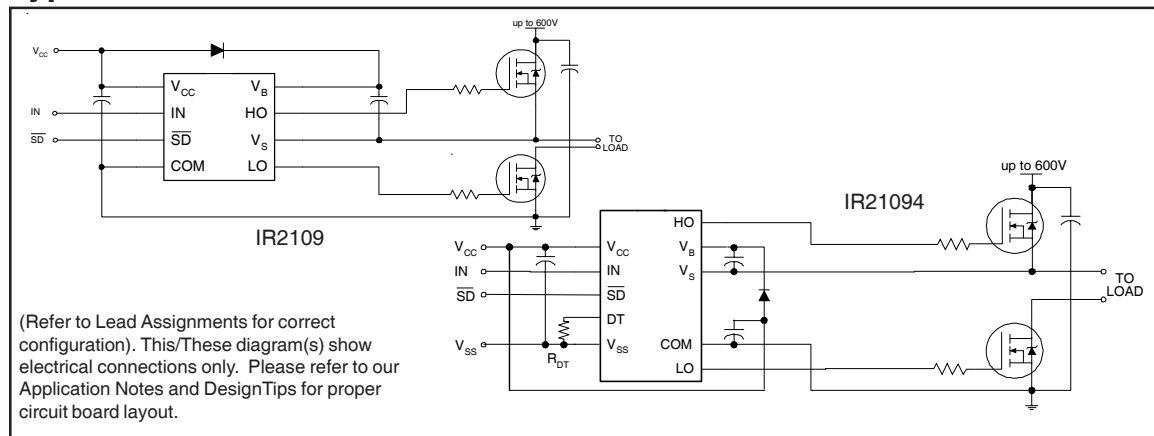
Product Summary

V_{OFFSET}	600V max.
$I_{O+/-}$	120 mA / 250 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	750 & 200 ns
Dead Time	540 ns
(programmable up to 5us for IR21094)	

Packages



Typical Connection



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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V _B	High side floating absolute voltage	-0.3	625	V	
V _S	High side floating supply offset voltage	V _B - 25	V _B + 0.3		
V _{HO}	High side floating output voltage	V _S - 0.3	V _B + 0.3		
V _{CC}	Low side and logic fixed supply voltage	-0.3	25		
V _{LO}	Low side output voltage	-0.3	V _{CC} + 0.3		
DT	Programmable dead-time pin voltage (IR21094 only)	V _{SS} - 0.3	V _{CC} + 0.3		
V _{IN}	Logic input voltage (IN & $\overline{SD}$)	V _{SS} - 0.3	V _{CC} + 0.3		
V _{SS}	Logic ground (IR21094/IR21894 only)	V _{CC} - 25	V _{CC} + 0.3		
dV _S /dt	Allowable offset supply voltage transient	—	50	V/ns	
P _D	Package power dissipation @ T _A ≤ +25°C	(8 Lead PDIP)	—	1.0	W
		(8 Lead SOIC)	—	0.625	
		(14 lead PDIP)	—	1.6	
		(14 lead SOIC)	—	1.0	
R _{thJA}	Thermal resistance, junction to ambient	(8 Lead PDIP)	—	125	°C/W
		(8 Lead SOIC)	—	200	
		(14 lead PDIP)	—	75	
		(14 lead SOIC)	—	120	
T _J	Junction temperature	—	150	°C	
T _S	Storage temperature	-50	150		
T _L	Lead temperature (soldering, 10 seconds)	—	300		

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	$V_S + 10$	$V_S + 20$	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)	V_{SS}	V_{CC}	
DT	Programmable dead-time pin voltage (IR21094 only)	V_{SS}	V_{CC}	
V_{SS}	Logic ground (IR21094 only)	-5	5	°C
T_A	Ambient temperature	-40	125	

Note 1: Logic operational for V_S of -5V to +600V. Logic state held for V_S of -5V to - V_{BS} . (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C, DT = V_{SS} unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	750	950	nsec	$V_S = 0V$
t_{off}	Turn-off propagation delay	—	200	280		$V_S = 0V$ or 600V
t_{sd}	Shut-down propagation delay	—	200	280		
MT	Delay matching, HS & LS turn-on/off	—	0	70		
t_r	Turn-on rise time	—	150	220		$V_S = 0V$
t_f	Turn-off fall time	—	50	80		$V_S = 0V$
DT	Deadtime: LO turn-off to HO turn-on (DTLO-HO) & HO turn-off to LO turn-on (DTHO-LO)	400 4	540 5	680 6	usec	RDT = 0 RDT = 200k (IR21094)
MDT	Deadtime matching = DTLO - HO - DTHO-LO	—	0	60	nsec	RDT=0
		—	0	600		RDT = 200k (IR21094)

IR2109(4) (s) & (PbF)

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Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, V_{SS} = COM, $DT = V_{SS}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified. The V_{IL} , V_{IH} and I_{IN} parameters are referenced to V_{SS} /COM and are applicable to the respective input leads: IN and SD. The V_O , I_O and R_{on} parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage for HO & logic "0" for LO	2.9	—	—	V	$V_{CC} = 10\text{V to } 20\text{V}$
V_{IL}	Logic "0" input voltage for HO & logic "1" for LO	—	—	0.8		$V_{CC} = 10\text{V to } 20\text{V}$
$V_{SD,TH+}$	$\overline{SD}$ input positive going threshold	2.9	—	—		$V_{CC} = 10\text{V to } 20\text{V}$
$V_{SD,TH-}$	$\overline{SD}$ input negative going threshold	—	—	0.8		$V_{CC} = 10\text{V to } 20\text{V}$
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	0.8	1.4		$I_O = 20\text{ mA}$
V_{OL}	Low level output voltage, V_O	—	0.3	0.6		$I_O = 20\text{ mA}$
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 600\text{V}$
I_{QBS}	Quiescent V_{BS} supply current	20	75	130	mA	$V_{IN} = 0\text{V or } 5\text{V}$
I_{QCC}	Quiescent V_{CC} supply current	0.4	1.0	1.6		$V_{IN} = 0\text{V or } 5\text{V}$ $R_{DT} = 0$
I_{IN+}	Logic "1" input bias current	—	5	20	μA	$IN = 5\text{V}, \overline{SD} = 0\text{V}$
I_{IN-}	Logic "0" input bias current	—	—	2		$IN = 0\text{V}, \overline{SD} = 5\text{V}$
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed current	120	200	—	mA	$V_O = 0\text{V}, PW \leq 10\text{ }\mu\text{s}$
I_{O-}	Output low short circuit pulsed current	250	350	—		$V_O = 15\text{V}, PW \leq 10\text{ }\mu\text{s}$

The image displays two circuit diagrams for MOSFET drivers, labeled IR2109 and IR21094.

IR2109: This diagram shows a single-channel MOSFET driver. The input IN is connected to a resistor and an inverter. The output of the inverter is connected to a DEADTIME block. The output of the DEADTIME block is connected to the VSS/COM LEVEL SHIFT block. The output of the VSS/COM LEVEL SHIFT block is connected to the PULSE GENERATOR. The output of the PULSE GENERATOR is connected to the HV LEVEL SHIFTER. The output of the HV LEVEL SHIFTER is connected to the PULSE FILTER. The output of the PULSE FILTER is connected to the R, Q, and S inputs of a 3-input NAND gate. The output of the 3-input NAND gate is connected to the UV DETECT block. The output of the UV DETECT block is connected to the VCC pin. The output of the VCC pin is connected to the HO pin. The output of the HO pin is connected to the VS pin. The output of the VS pin is connected to the COM pin. The output of the COM pin is connected to the VSS pin.

IR21094: This diagram shows a dual-channel MOSFET driver. The input IN is connected to a resistor and an inverter. The output of the inverter is connected to a DEADTIME block. The output of the DEADTIME block is connected to the VSS/COM LEVEL SHIFT block. The output of the VSS/COM LEVEL SHIFT block is connected to the PULSE GENERATOR. The output of the PULSE GENERATOR is connected to the HV LEVEL SHIFTER. The output of the HV LEVEL SHIFTER is connected to the PULSE FILTER. The output of the PULSE FILTER is connected to the R, Q, and S inputs of a 3-input NAND gate. The output of the 3-input NAND gate is connected to the UV DETECT block. The output of the UV DETECT block is connected to the VCC pin. The output of the VCC pin is connected to the HO pin. The output of the HO pin is connected to the VS pin. The output of the VS pin is connected to the COM pin. The output of the COM pin is connected to the VSS pin. The output of the VSS pin is connected to the DT pin. The output of the DT pin is connected to the DEADTIME block. The output of the DEADTIME block is connected to the VSS/COM LEVEL SHIFT block. The output of the VSS/COM LEVEL SHIFT block is connected to the PULSE GENERATOR. The output of the PULSE GENERATOR is connected to the HV LEVEL SHIFTER. The output of the HV LEVEL SHIFTER is connected to the PULSE FILTER. The output of the PULSE FILTER is connected to the R, Q, and S inputs of a 3-input NAND gate. The output of the 3-input NAND gate is connected to the UV DETECT block. The output of the UV DETECT block is connected to the VCC pin. The output of the VCC pin is connected to the HO pin. The output of the HO pin is connected to the VS pin. The output of the VS pin is connected to the COM pin. The output of the COM pin is connected to the VSS pin.

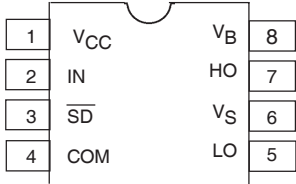
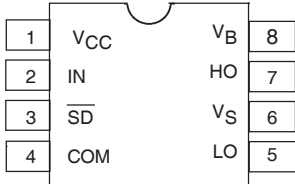
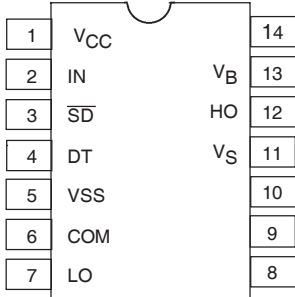
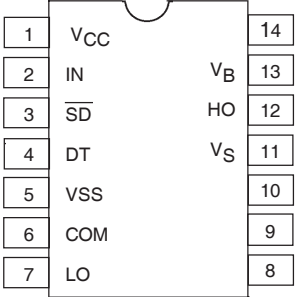
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Lead Definitions

Symbol	Description
IN	Logic input for high and low side gate driver outputs (HO and LO), in phase with HO (referenced to COM for IR2109 and VSS for IR21094)
$\overline{SD}$	Logic input for shutdown (referenced to COM for IR2109 and VSS for IR21094)
DT	Programmable dead-time lead, referenced to VSS. (IR21094 only)
VSS	Logic Ground (21094 only)
V _B	High side floating supply
HO	High side gate drive output
V _S	High side floating supply return
V _{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments

 8 Lead PDIP IR2109	 8 Lead SOIC IR2109S
 14 Lead PDIP IR21094	 14 Lead SOIC IR21094S

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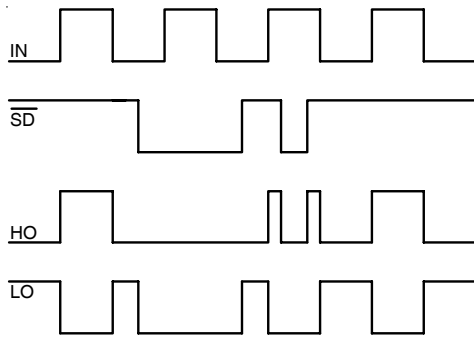


Figure 1. Input/Output Timing Diagram

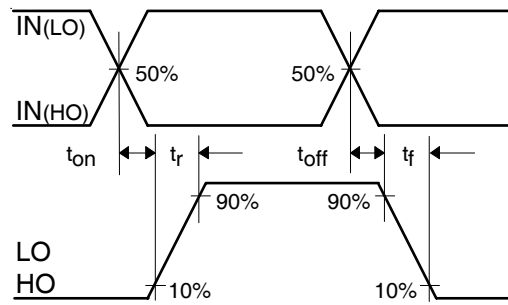


Figure 2. Switching Time Waveform Definitions

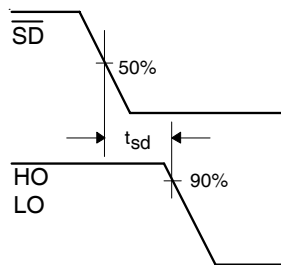


Figure 3. Shutdown Waveform Definitions

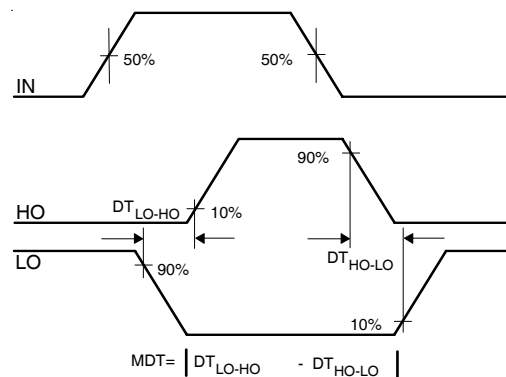


Figure 4. Deadtime Waveform Definitions

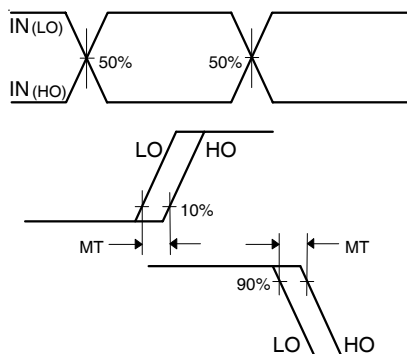


Figure 5. Delay Matching Waveform Definitions

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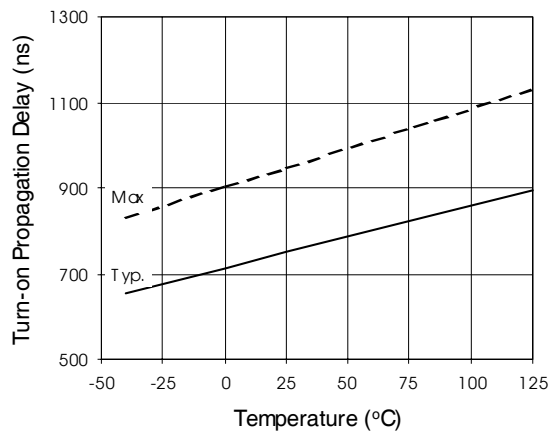


Figure 6A. Turn-on Propagation Delay vs. Temperature

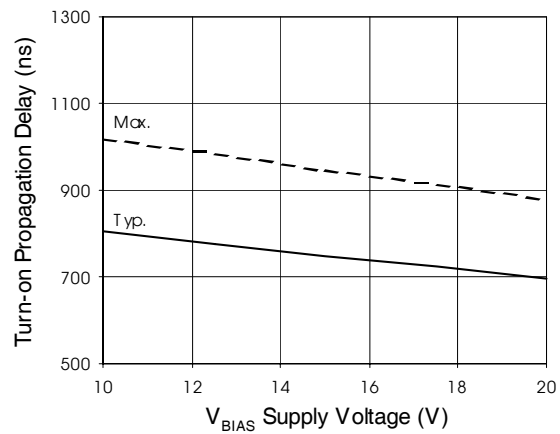


Figure 6B. Turn-on Propagation Delay vs. Supply Voltage

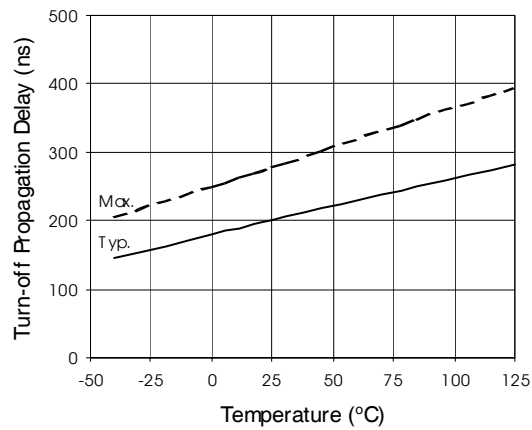


Figure 7A. Turn-off Propagation Delay vs. Temperature

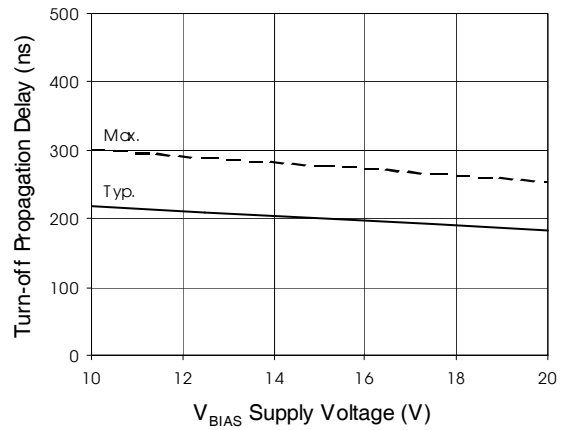


Figure 7B. Turn-off Propagation Delay vs. Supply Voltage

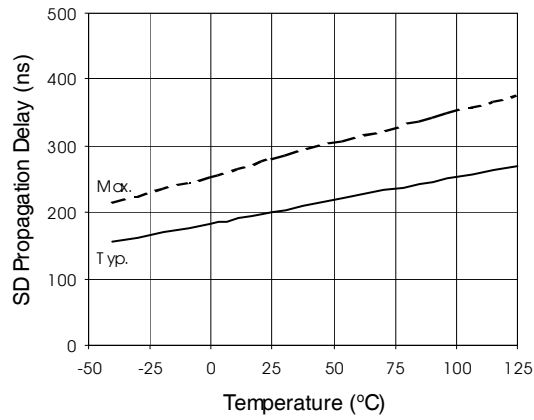


Figure 8A. SD Propagation Delay vs. Temperature

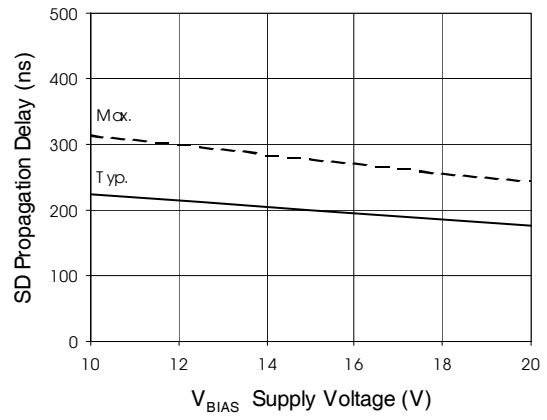


Figure 8B. SD Propagation Delay vs. Supply Voltage

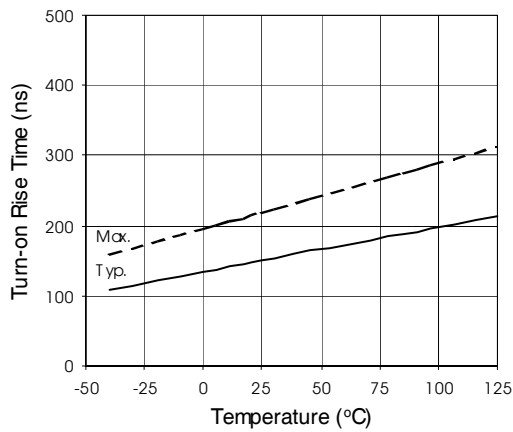


Figure 9A. Turn-on Rise Time vs. Temperature

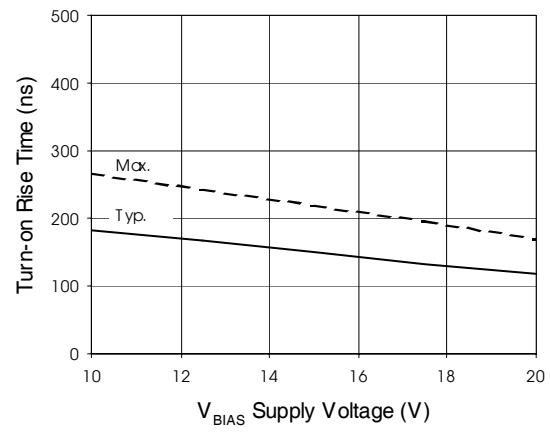


Figure 9B. Turn-on Rise Time vs. Supply Voltage

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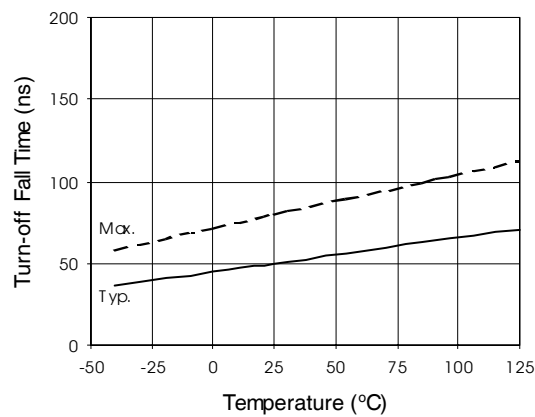


Figure 10A. Turn-off Fall Time vs. Temperature

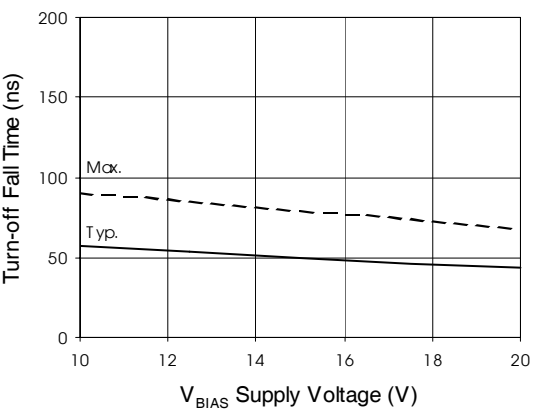


Figure 10B. Turn-off Fall Time vs. Supply Voltage

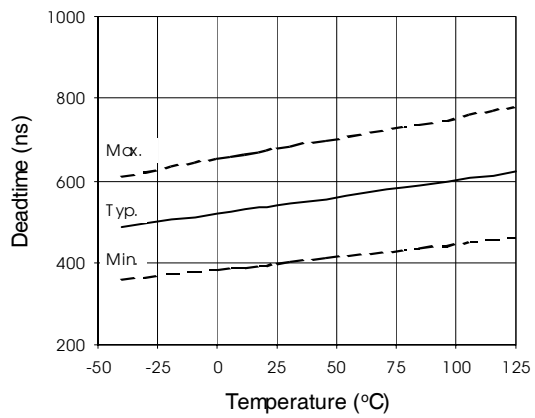


Figure 11A. Deadtime vs. Temperature

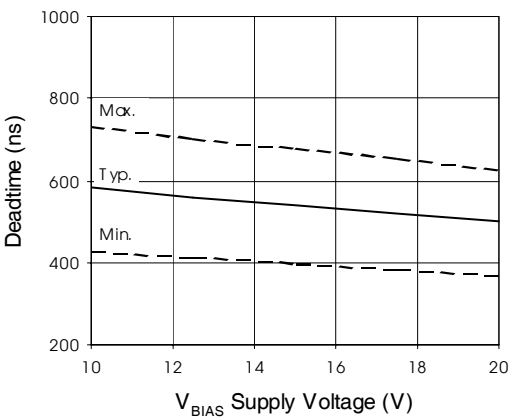


Figure 11B. Deadtime vs. Supply Voltage

IR2109(4) (s) & (PbF)

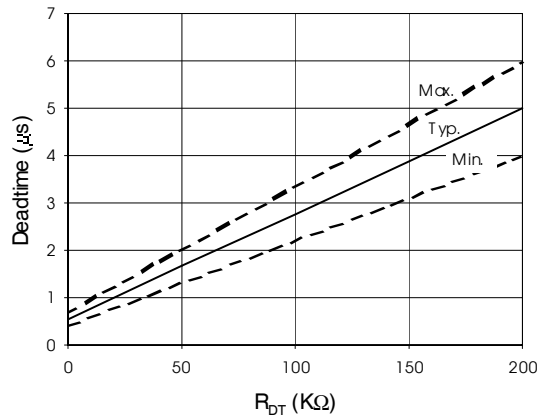


Figure 11C. Deadtime vs. R_{DT}
(IR21094 only)

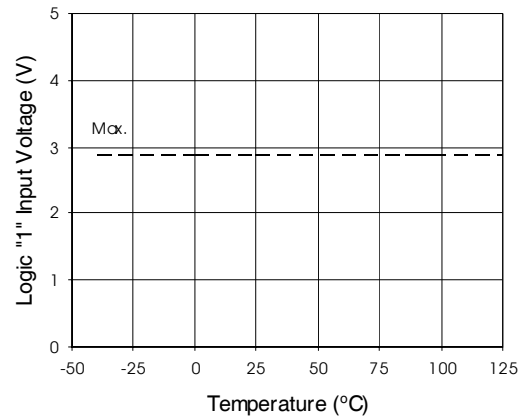


Figure 12A. Logic "1" Input Voltage
vs. Temperature

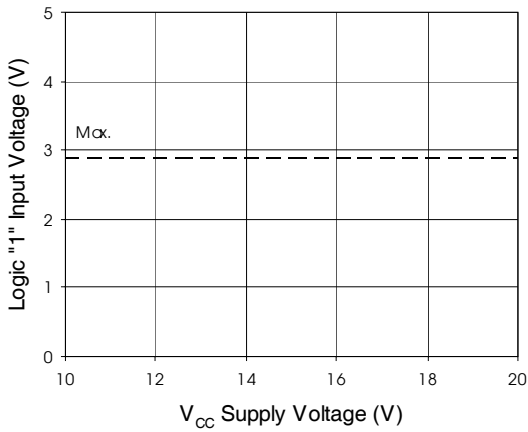


Figure 12B. Logic "1" Input Voltage
vs. Supply Voltage

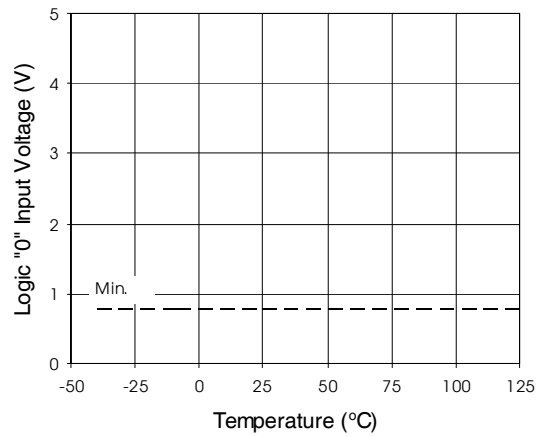


Figure 13A. Logic "0" Input Voltage
vs. Temperature

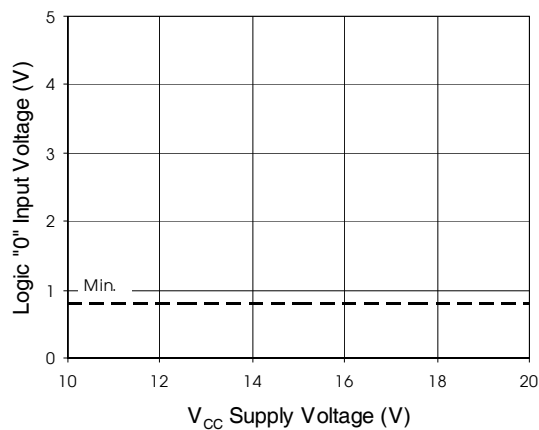


Figure 13B. Logic “0” Input Current vs. Supply Voltage

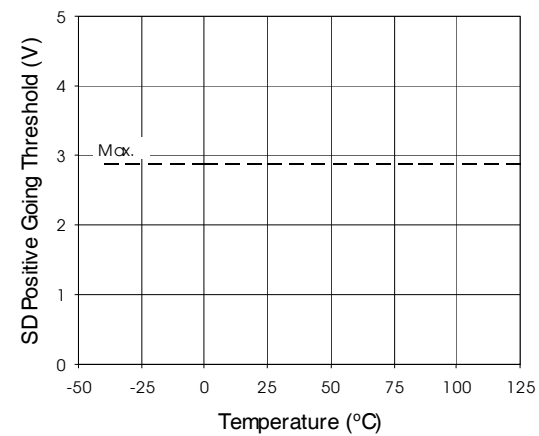


Figure 14A. SD Positive Going Threshold vs. Temperature

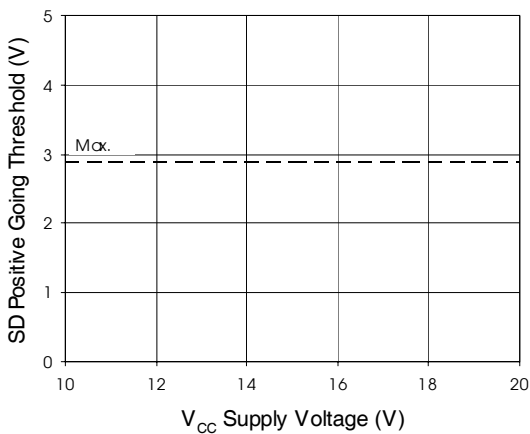


Figure 14B. SD Positive Going Threshold vs. Supply Voltage

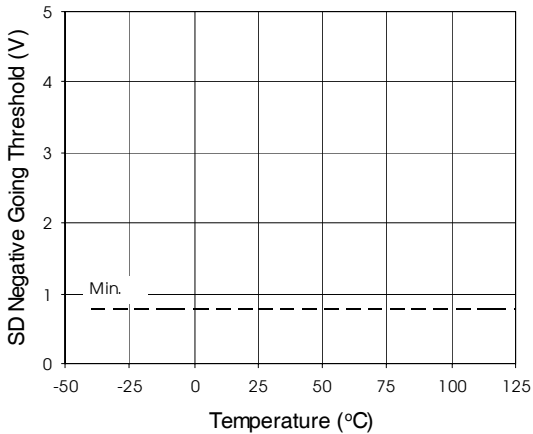


Figure 15A. SD Negative Going Threshold vs. Temperature

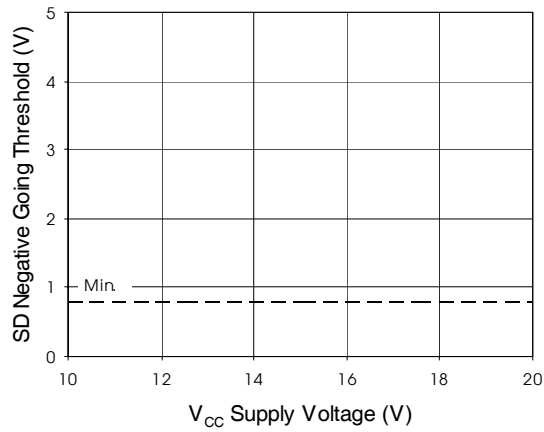


Figure 15B. SD Negative Going Threshold vs. Supply Voltage

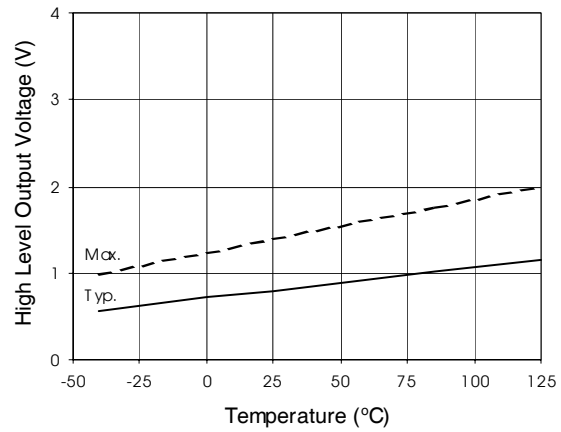


Figure 16A. High Level Output Voltage vs. Temperature

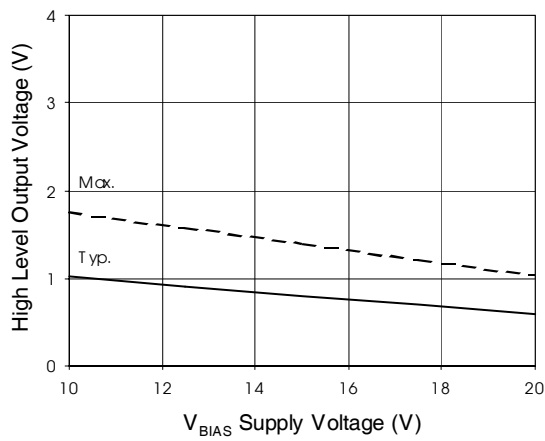


Figure 16B. High Level Output Voltage vs. Supply Voltage

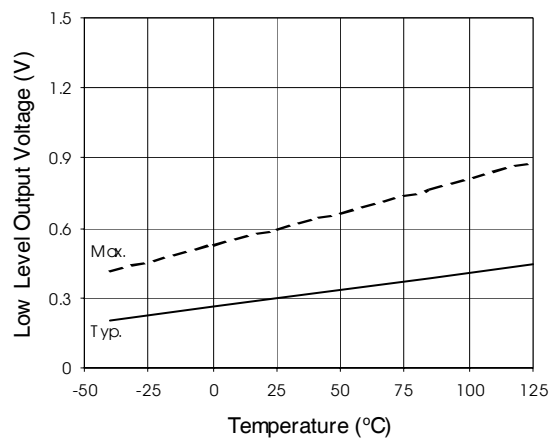


Figure 17A. Low Level Output Voltage vs. Temperature

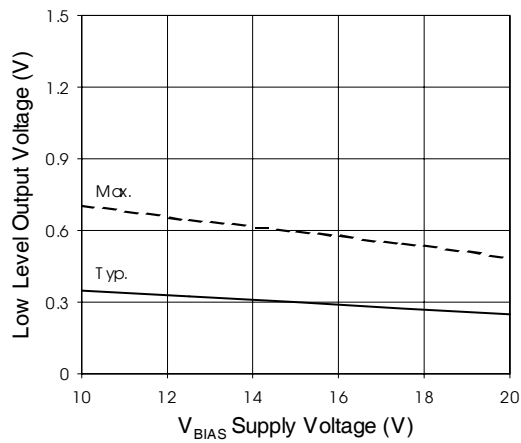


Figure 17B. Low Level Output Voltage vs. Supply Voltage

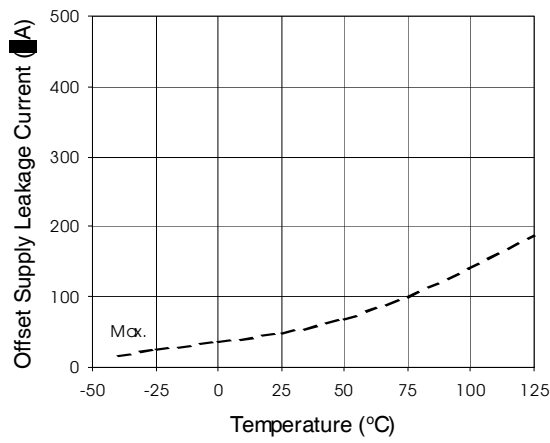


Figure 18A. Offset Supply Leakage Current vs. Temperature

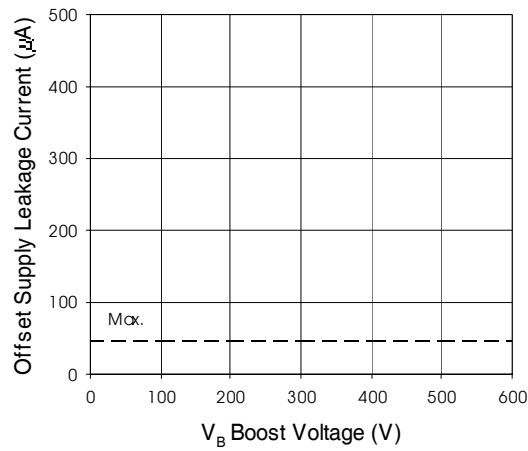


Figure 18B. Offset Supply Leakage Current vs. Boost Voltage

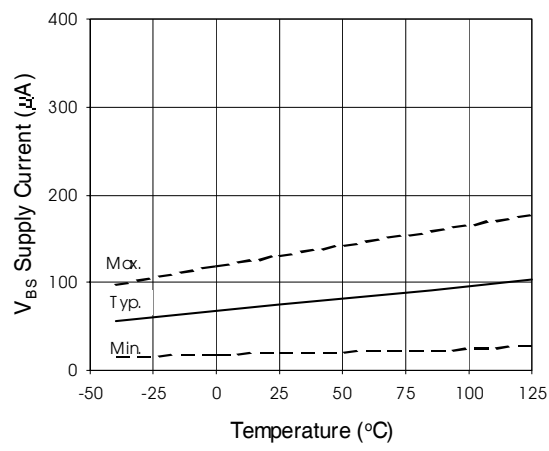


Figure 19A. V_{BS} Supply Current vs. Temperature

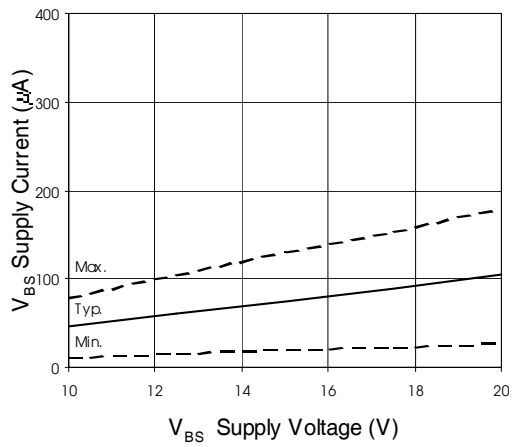


Figure 19B. V_{BS} Supply Current vs. Supply Voltage

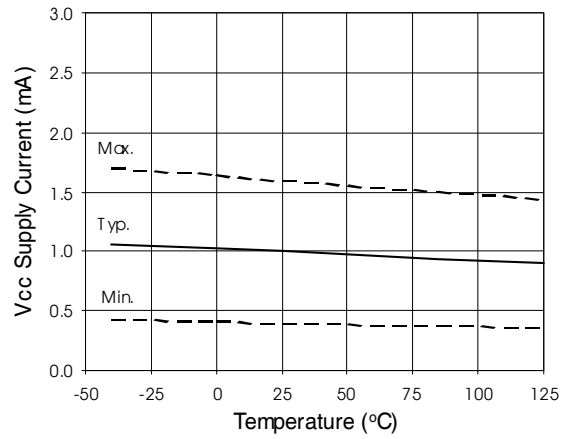


Figure 20A. V_{CC} Supply Current vs. Temperature

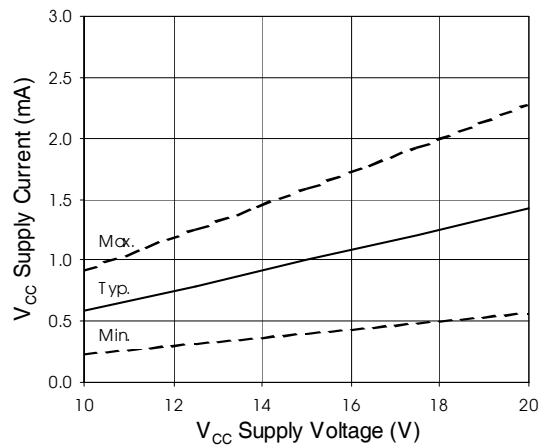


Figure 20B. V_{CC} Supply Current vs. V_{CC} Supply Voltage

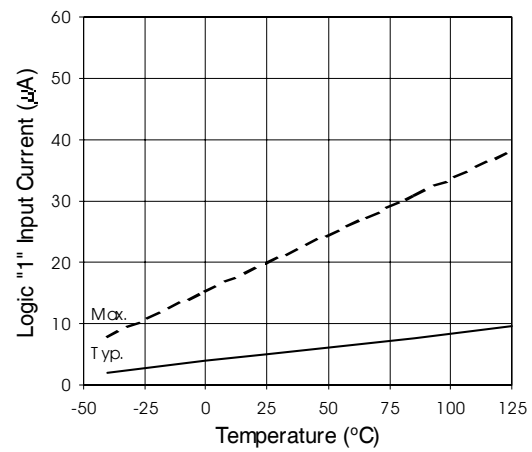


Figure 21A. Logic "1" Input Current vs. Temperature

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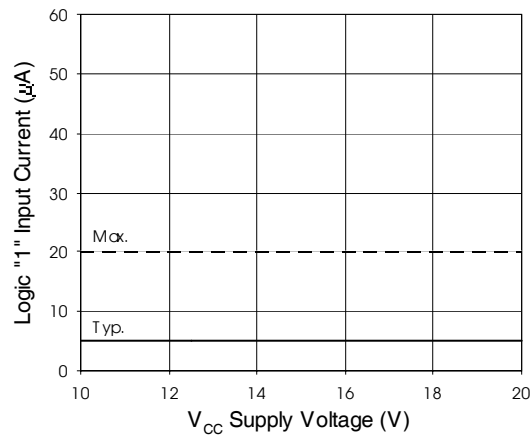


Figure 21B. Logic "1" Input Current vs. Supply Voltage

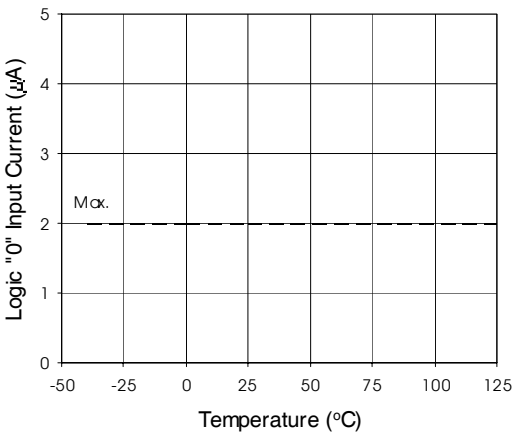


Figure 22A. Logic "0" Input Current vs. Temperature

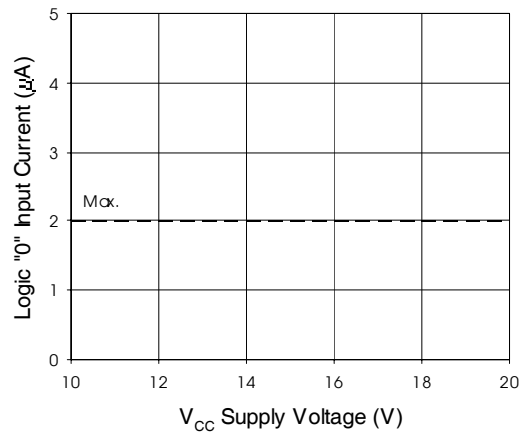


Figure 22B. Logic "0" Input Current vs. Supply Voltage

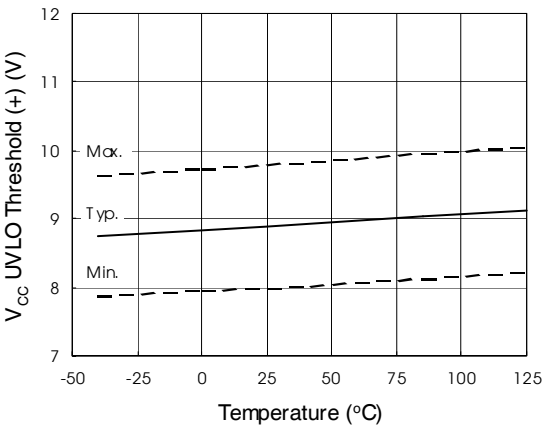


Figure 23. VCC Undervoltage Threshold (+) vs. Temperature

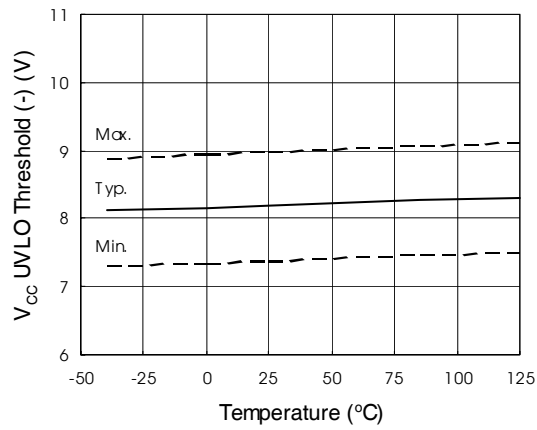


Figure 24. VCC Undervoltage Threshold (-) vs. Temperature

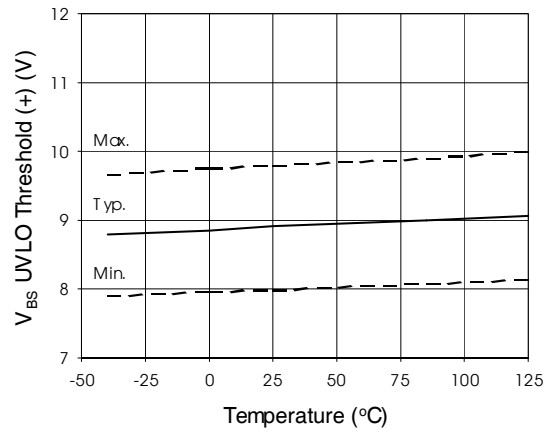


Figure 25. VBS Undervoltage Threshold (+) vs. Temperature

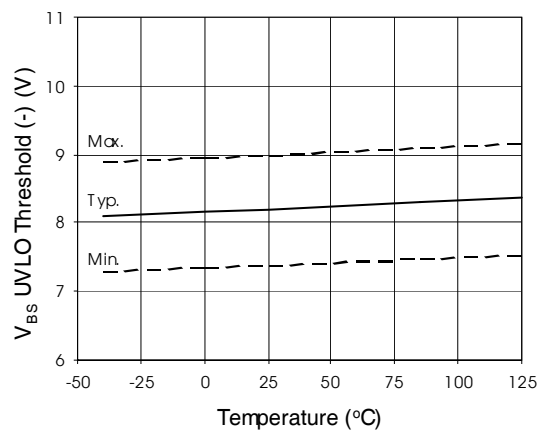


Figure 26. VBS Undervoltage Threshold (-) vs. Temperature

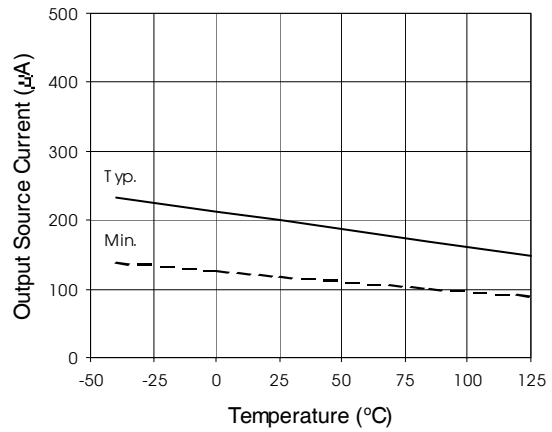


Figure 27A. Output Source Current vs. Temperature

IR2109(4) (s) & (PbF)

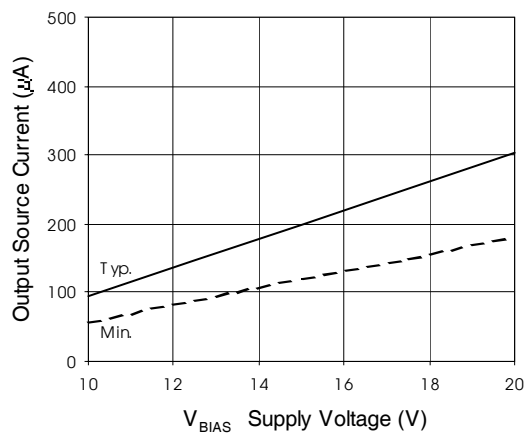


Figure 27B. Output Source Current vs. Supply Voltage

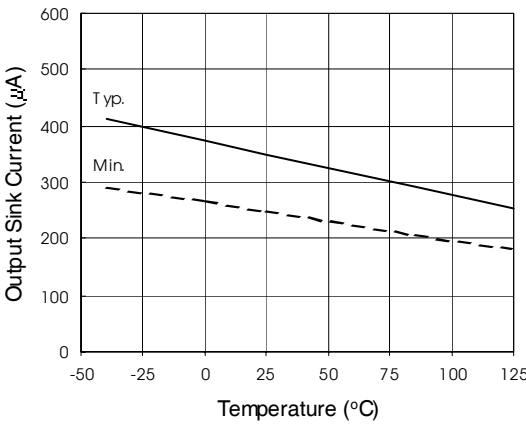


Figure 28A. Output Sink Current vs. Temperature

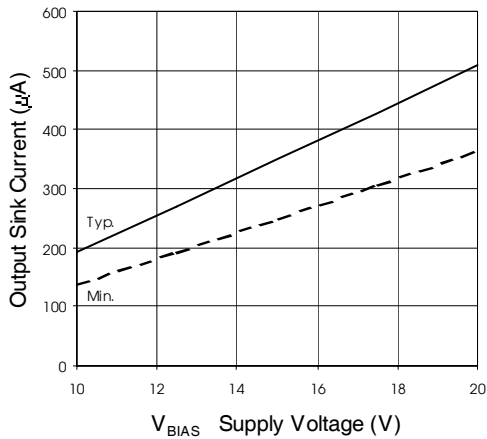


Figure 28B. Output Sink Current vs. Supply Voltage

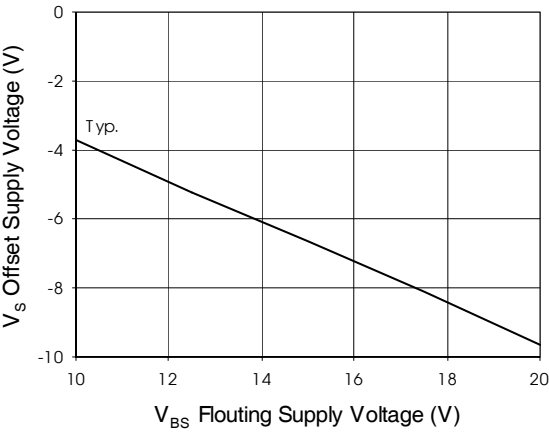


Figure 29. Maximum VS Negative Offset vs. Supply Voltage

IR2109(4) (s) & (PbF)

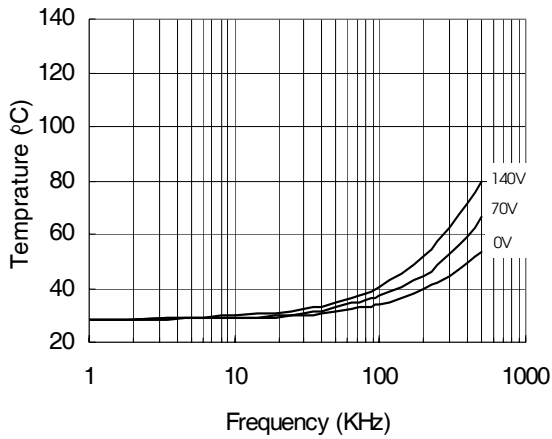


Figure 30. IR2109 vs Frequency (IRFBC20)
 $R_{gate} = 33\Omega$, $V_{CC} = 15V$

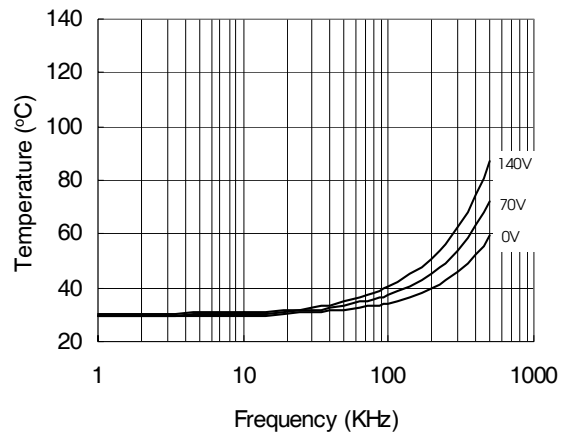


Figure 31. IR2109 vs Frequency (IRFBC30)
 $R_{gate} = 22\Omega$, $V_{CC} = 15V$

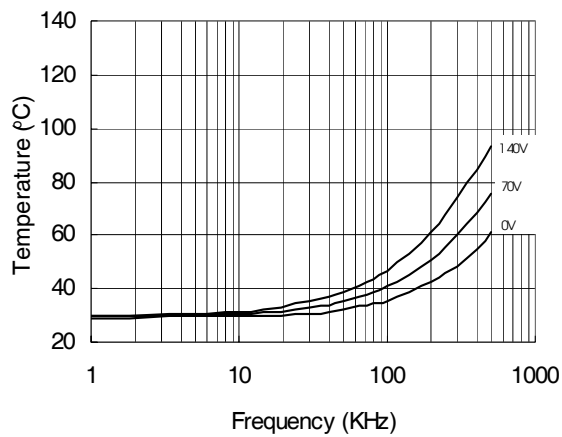


Figure 32. IR2109 vs Frequency (IRFBC40)
 $R_{gate} = 15\Omega$, $V_{CC} = 15V$

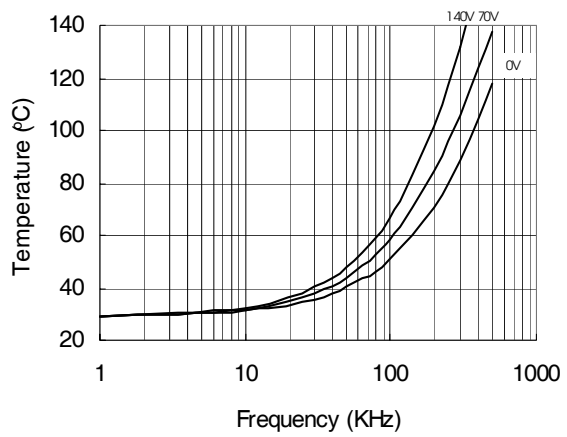


Figure 33. IR2109 vs Frequency (IRFPE50)
 $R_{gate} = 10\Omega$, $V_{CC} = 15V$

IR2109(4) (s) & (PbF)

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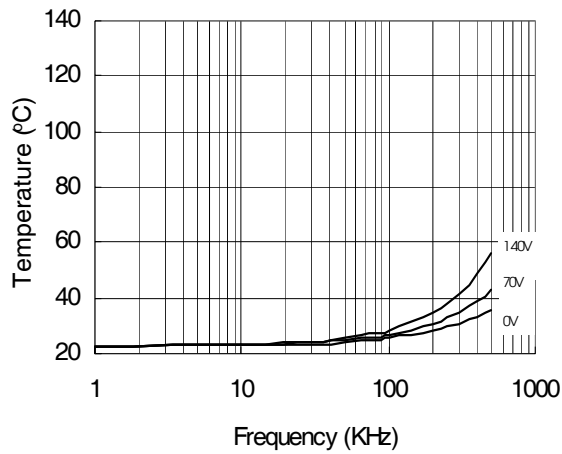


Figure 34. IR21094 vs. Frequency (IRFBC20),
 $R_{gate}=33\Omega$, $V_{CC}=15V$

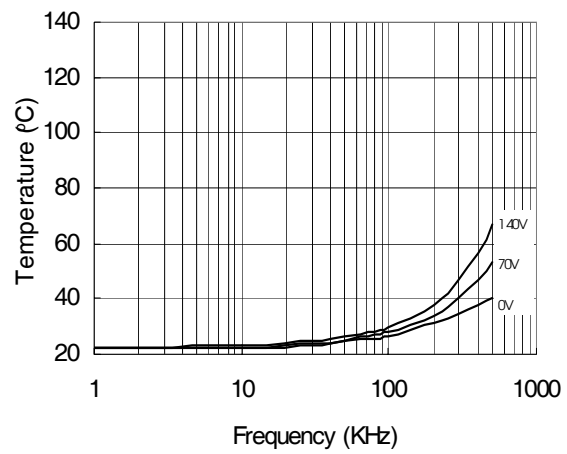


Figure 35. IR21094 vs. Frequency (IRFBC30),
 $R_{gate}=22\Omega$, $V_{CC}=15V$

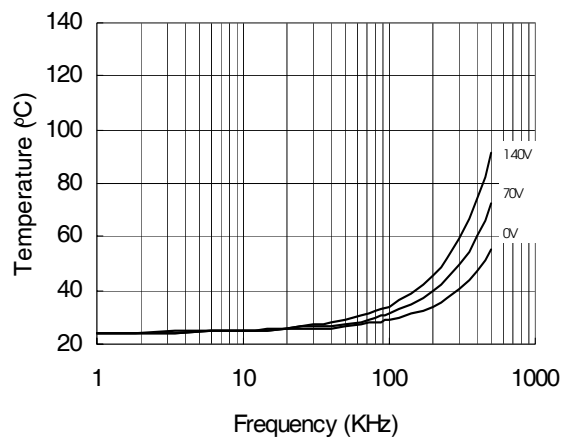


Figure 36. IR21094 vs. Frequency (IRFBC40),
 $R_{gate}=15\Omega$, $V_{CC}=15V$

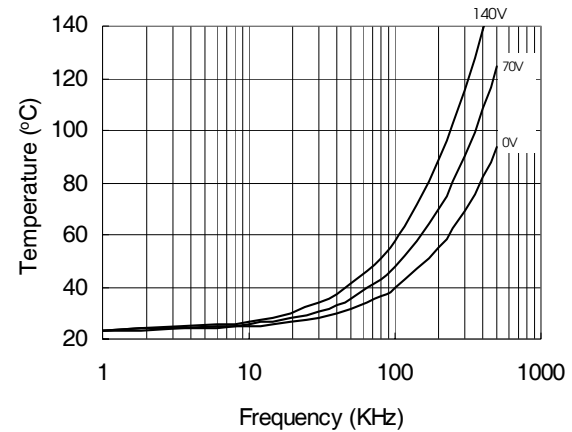


Figure 37. IR21094 vs. Frequency (IRFPE50),
 $R_{gate}=10\Omega$, $V_{CC}=15V$

IR2109(4) (s) & (PbF)

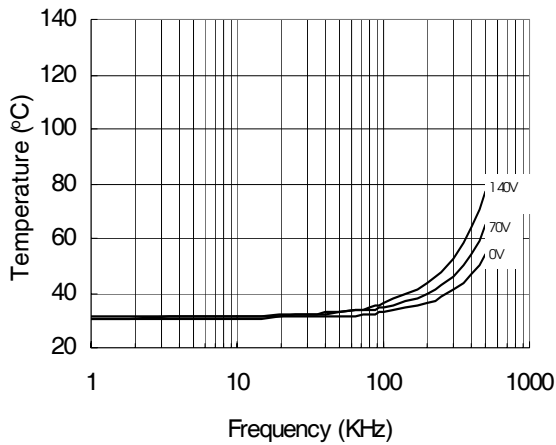


Figure 38. IR2109S vs. Frequency (IRFBC20),
 $R_{gate}=33\Omega$, $V_{CC}=15V$

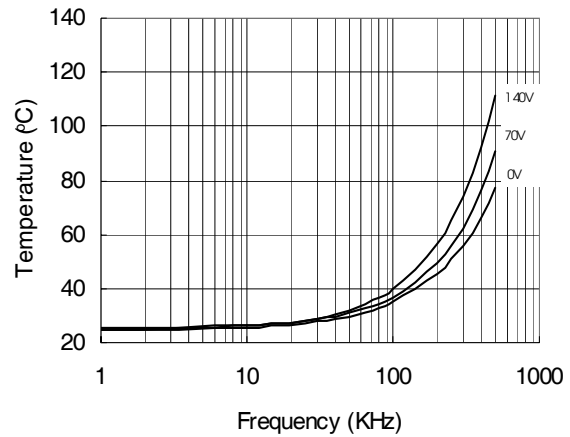


Figure 39. IR2109S vs. Frequency (IRFBC30),
 $R_{gate}=22\Omega$, $V_{CC}=15V$

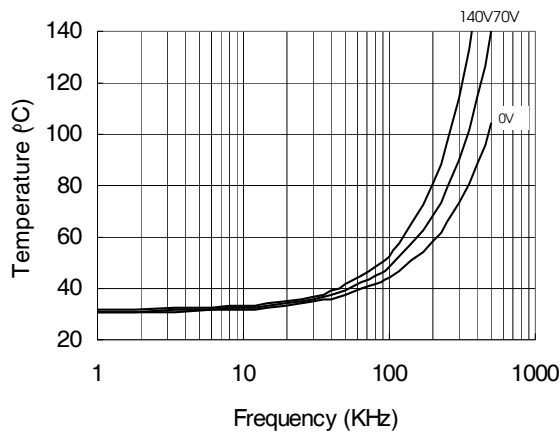


Figure 40. IR2109S vs. Frequency (IRFBC40),
 $R_{gate}=15\Omega$, $V_{CC}=15V$

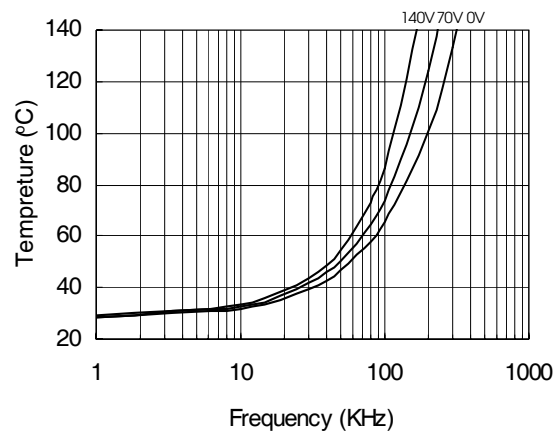


Figure 41. IR2109S vs. Frequency
(IRFPE50), $R_{gate}=10\Omega$, $V_{CC}=15V$

IR2109(4) (s) & (PbF)

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IR Rectifier

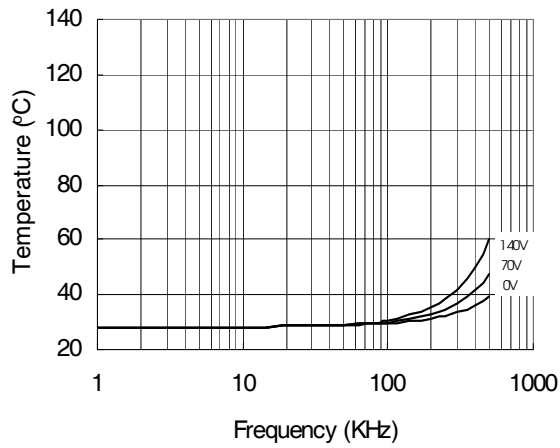


Figure 42. IR21094S vs. Frequency (IRFBC20),
 $R_{gate}=33\Omega$, $V_{CC}=15V$

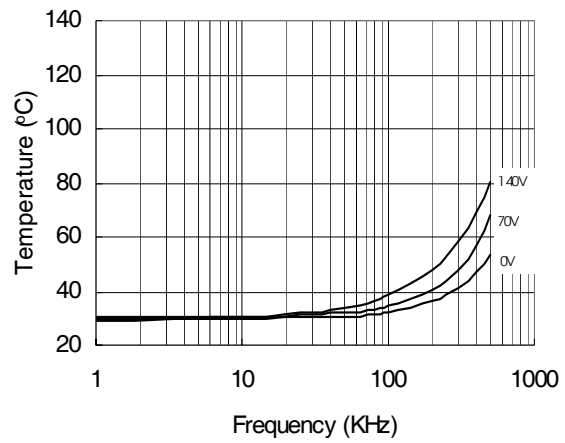


Figure 43. IR21094S vs. Frequency (IRFBC30),
 $R_{gate}=22\Omega$, $V_{CC}=15V$

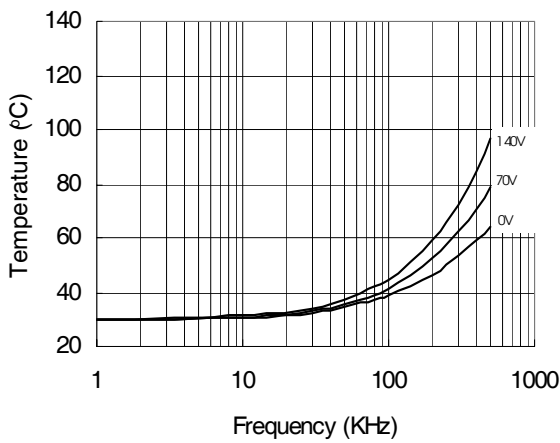


Figure 44. IR21094S vs. Frequency (IRFBC40),
 $R_{gate}=15\Omega$, $V_{CC}=15V$

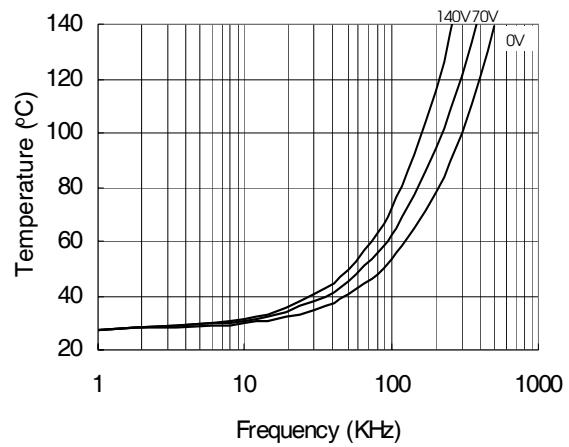
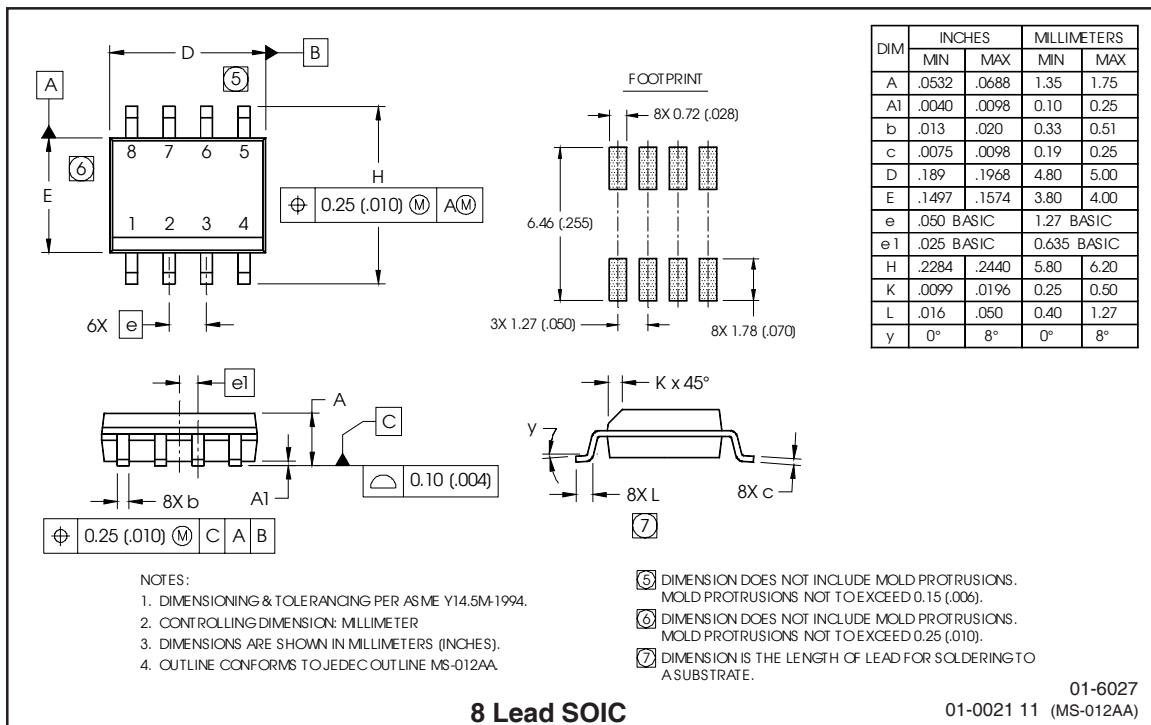
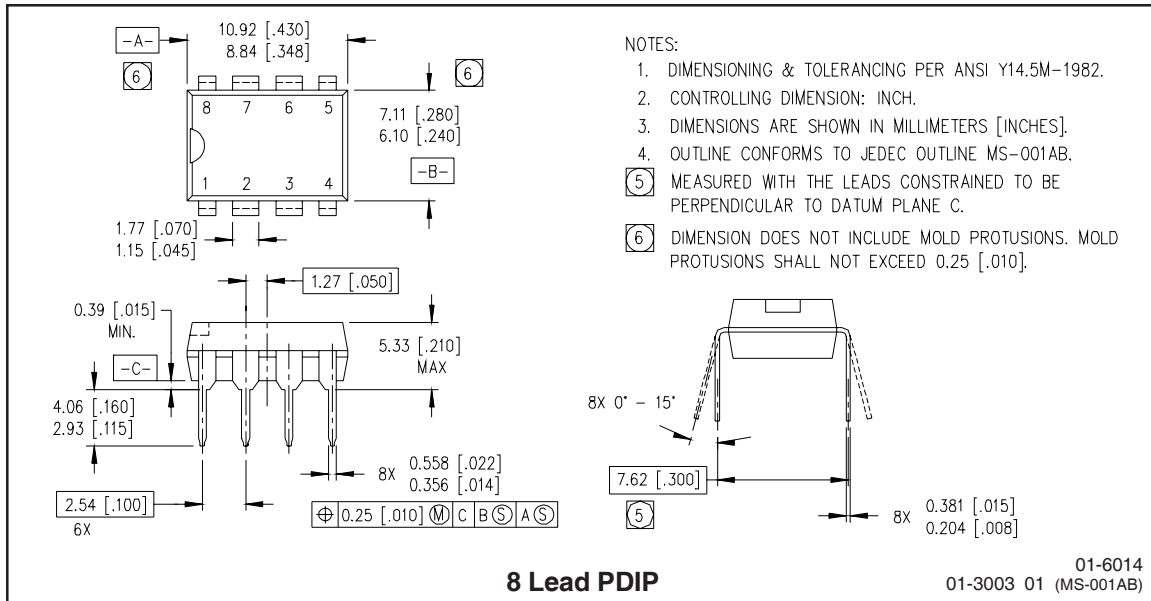


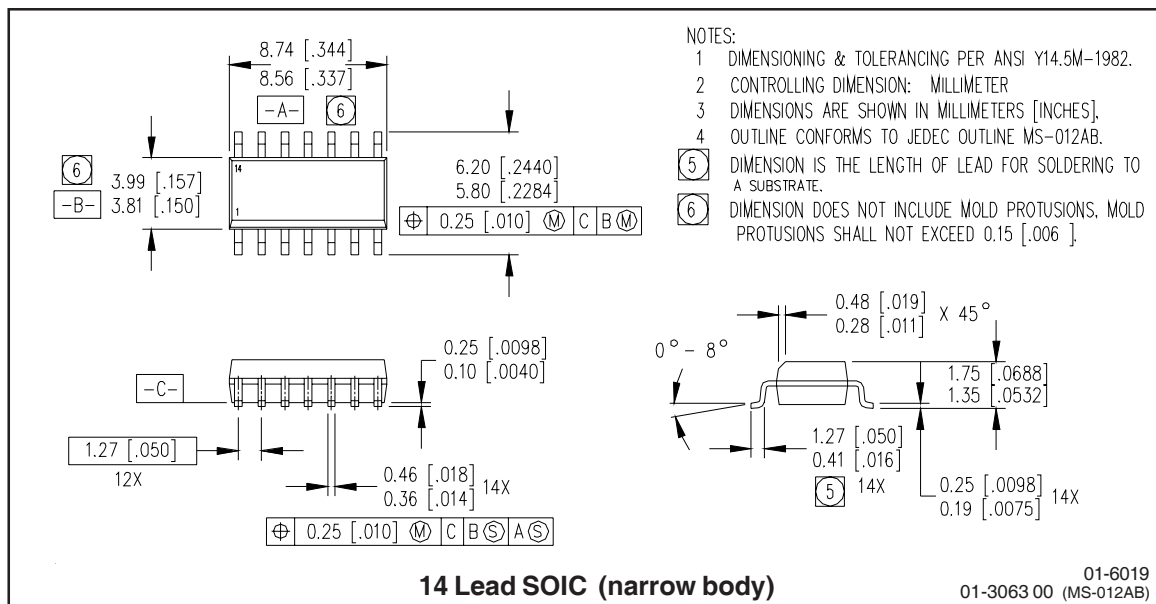
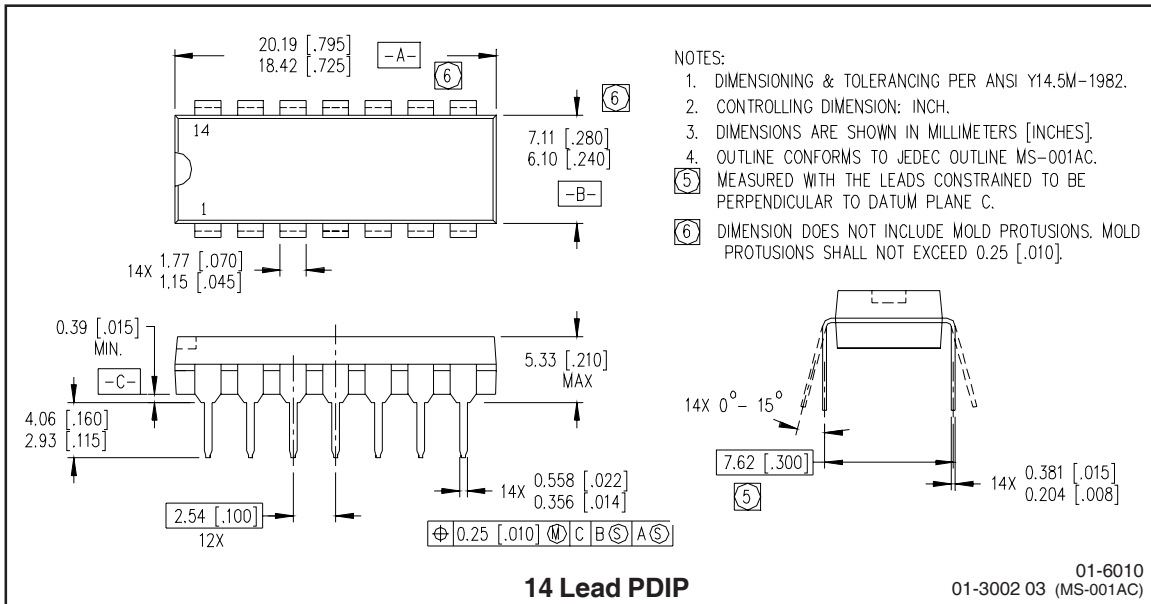
Figure 45. IR21094S vs. Frequency (IRFPE50),
 $R_{gate}=10\Omega$, $V_{CC}=15V$

Case Outlines



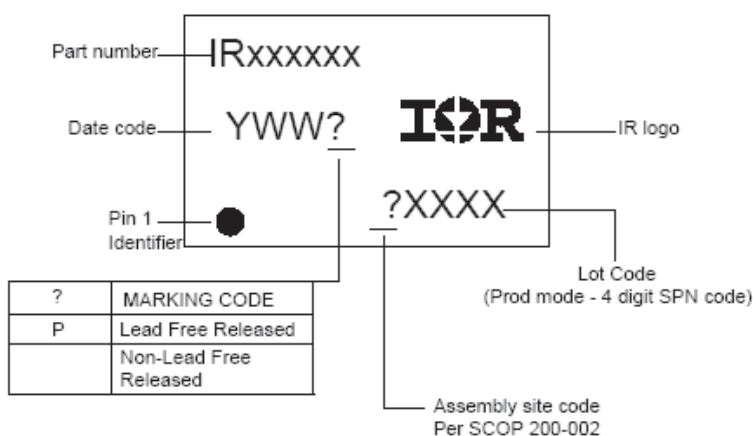
IR2109(4) (s) & (PbF)

International
IR Rectifier



Data and specifications subject to change without notice. 7/11/2003

LEADFREE PART MARKING INFORMATION



Basic Part (Non-Lead Free)

8-Lead PDIP IR2109 order IR2109
 8-Lead SOIC IR2109S order IR2109S
 14-Lead PDIP IR21094 order IR21094
 14-Lead SOIC IR21094S order IR21094S

Lead-Free Part

8-Lead PDIP IR2109 order IR2109PbF
 8-Lead SOIC IR2109S order IR2109SPbF
 14-Lead PDIP IR21094 order IR21094PbF
 14-Lead SOIC IR21094S order IR21094SPbF