

CYM1471 CYM1481

1024K x 8 SRAM Module 2048K x 8 SRAM Module

Features

- High-density 8-/16-megabit SRAM modules
- High-speed CMOS SRAMs
 - Access time of 70 ns
- Low active power
 - 605 mW (max.), 2M x 8
- Double-sided SMD technology
- TTL-compatible inputs and outputs
- Small footprint SIP
 - PCB layout area of 0.72 sq. in.
- 2V data retention (L version)

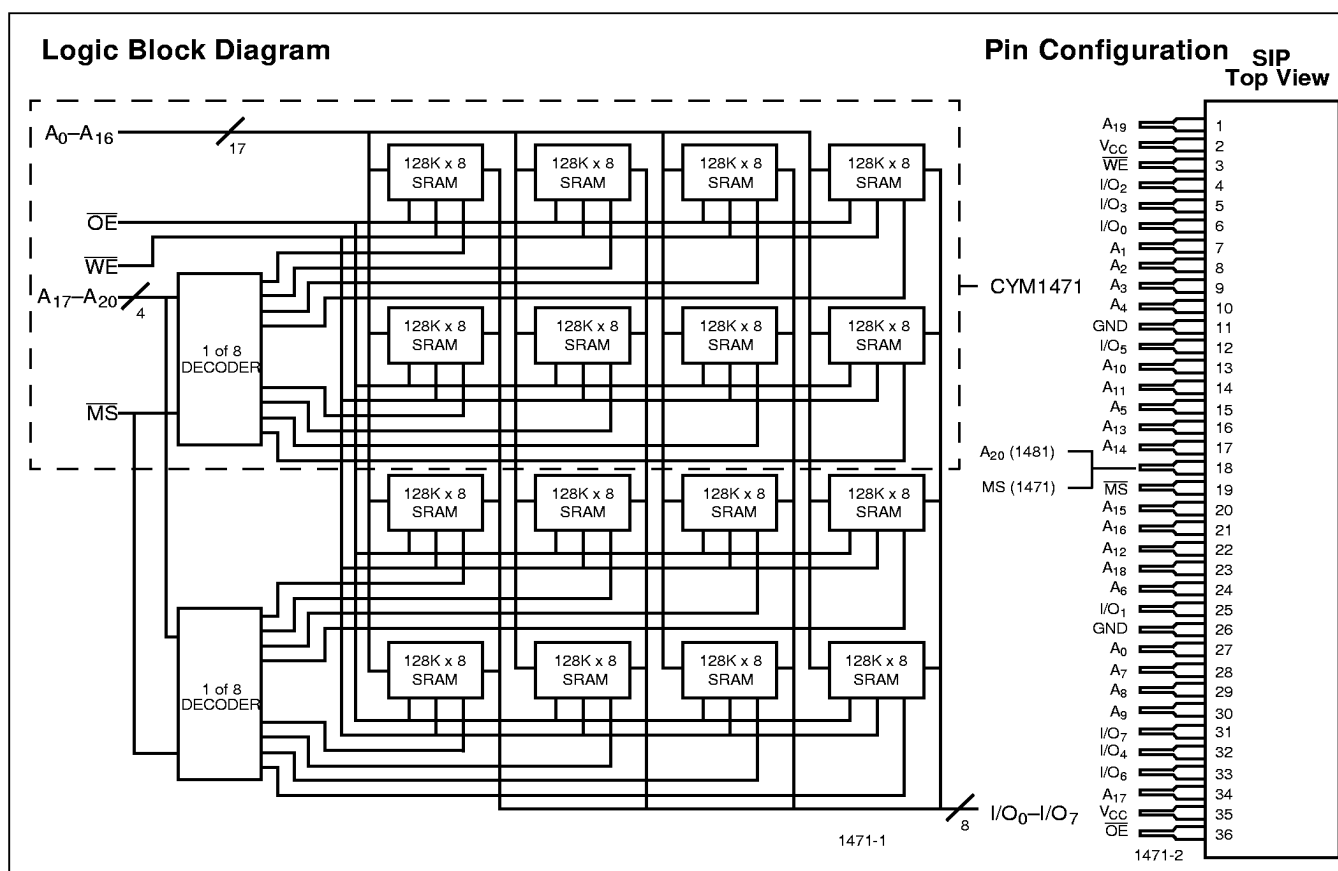
Functional Description

The CYM1471 and CYM1481 are high-performance 8-megabit and 16-megabit static RAM modules organized as 1024K words (1471) or 2048K words (1481) by 8 bits. These modules

are constructed from eight (1471) or sixteen (1481) 128K x 8 SRAMs in plastic surface-mount packages on an epoxy laminate board with pins. On-board decoding selects one of the SRAMs from the high-order address lines, keeping the remaining devices in standby mode for minimum power consumption.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{MS}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins is written into the memory location specified on the address pins. Reading the device is accomplished by selecting the device and enabling the outputs $\overline{MS}$ and $\overline{OE}$ active LOW while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the content of the location addressed by the information on the address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.





Selection Guide

	CYM1471				CYM1481			
Maximum Access Time (ns)	70	85	100	120	70	85	100	120
Maximum Operating Current (mA)	95	95	95	95	110	110	110	110
Maximum Standby Current (mA)	32	32	32	32	64	64	64	64

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature -55°C to +125°C

Ambient Temperature with
Power Applied 0°C to +70°C

Supply Voltage to Ground Potential -0.3V to +7.0V

DC Voltage Applied to Outputs
in High Z State -0.3V to +7.0V

DC Input Voltage -0.3V to +7.0V

Output Current into Outputs (LOW) 20 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1471		1481		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -1.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 2.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage		-0.3	0.8	-0.3	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-20	+20	-20	+20	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-20	+20	-20	+20	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., $\overline{MS} \leq V_{IL}$, I _{OUT} = 0 mA		95		110	mA
I _{SB1}	Automatic $\overline{MS}$ Power-Down Current	Max. V _{CC} , $\overline{MS} \geq V_{IH}$, Min. Duty Cycle = 100%		32		64	mA
I _{SB2}	Automatic $\overline{MS}$ Power-Down Current	Max. V _{CC} , $\overline{MS} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V, or V _{IN} ≤ 0.2V	Standard	16		32	mA
			L Version -100, -120	250		500	μA
			L Version -85	800		1600	μA

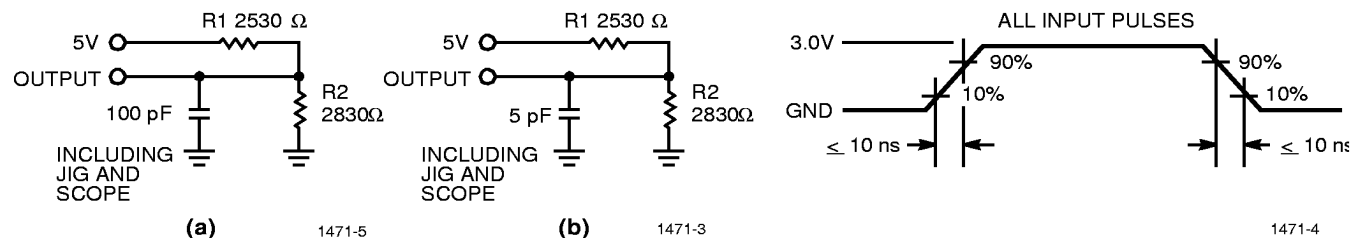
Capacitance^[1]

Parameter	Description	Test Conditions	CYM1471 Max.	CYM1481 Max.	Unit
C _{INA}	Input Capacitance (A ₀₋₁₆ , OE, WE)	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	75	125	pF
C _{INB}	Input Capacitance (A ₁₇₋₂₀ , $\overline{MS}$)		25	25	pF
C _{OUT}	Output Capacitance		95	165	pF

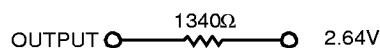
Note:

1. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range^[2]

Parameter	Description	1471-70 1481-70		1471-85 1481-85		1471-100 1481-100		1471-120 1481-120		Unit
		Min	Max	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t _{RC}	Read Cycle Time	70		85		100		120		ns
t _{AA}	Address to Data Valid		70		85		100		120	ns
t _{OHA}	Data Hold from Address Change	5		10		10		10		ns
t _{AMS}	$\overline{MS}$ LOW to Data Valid		70		85		100		120	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		40		45		50		60	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z	5		5		5		5		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[3]		30		30		35		45	ns
t _{LZMS}	$\overline{MS}$ LOW to Low Z ^[4]	5		10		10		10		ns
t _{HZMS}	$\overline{MS}$ HIGH to High Z ^[3, 4]		30		30		35		45	ns
WRITE CYCLE ^[5]										
t _{WC}	Write Cycle Time	70		85		100		120		ns
t _{SMS}	$\overline{MS}$ LOW to Write End	65		75		90		100		ns
t _{AW}	Address Set-Up to Write End	65		75		90		100		ns
t _{HA}	Address Hold from Write End	5		7		7		7		ns
t _{SA}	Address Set-Up to Write Start	0		5		5		5		ns
t _{PWE}	$\overline{WE}$ Pulse Width	65		65		75		85		ns
t _{SD}	Data Set-Up to Write End	30		35		40		45		ns
t _{HD}	Data Hold from Write End	0		5		5		5		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[3]		30		30		35		40	ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		5		ns

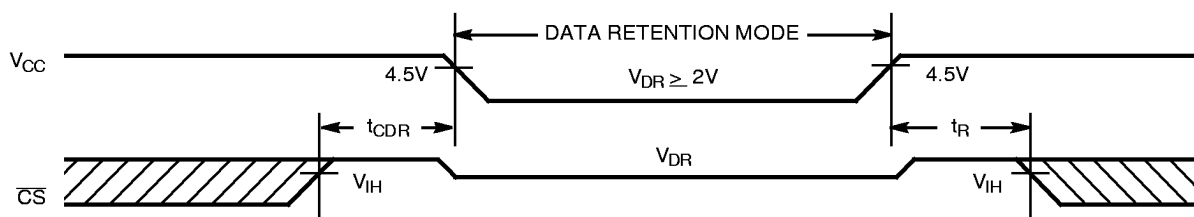
Notes:

- Test conditions assume signal transition time of 10 μs or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, output loading of 1 TTL load, and 100-pF load capacitance.
- t_{HZOE} , t_{HZMS} , and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZMS} is less than t_{LZMS} for any given device. These parameters are guaranteed and not 100% tested.
- The internal write time of the memory is defined by the overlap of $\overline{MS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	1471-70		1471-85		1471-100 1471-120		1481-70		1481-85		1481-100 1481-120		Unit
			Min.	Max	Min.	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V_{DR}	V_{CC} for Retention Data		2		2		2		2		2		2		V
I_{CCDR}	Data Retention Current	$V_{DR} = 3.0V$, $\overline{MS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		400		400		125		800		800		250	μA
$t_{CDR}^{[6]}$	Chip Deselect to Data Retention Time		0		0		0		0		0		0		ns
t_R	Operation Recovery Time		5		5		5		5		5		5		ns

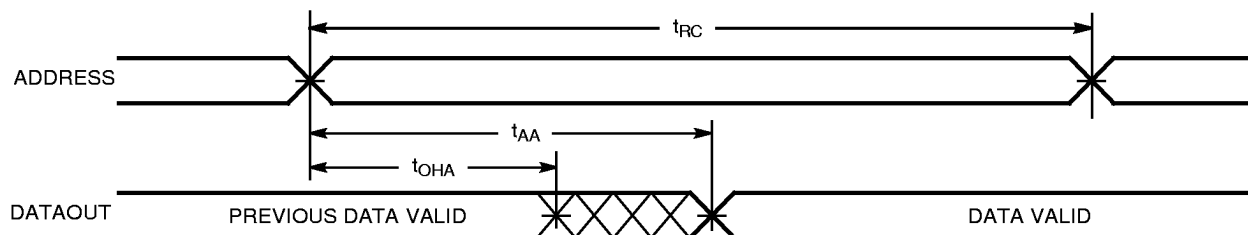
Data Retention Waveform



1471-6

Switching Waveforms

Read Cycle No. 1^[7, 8]



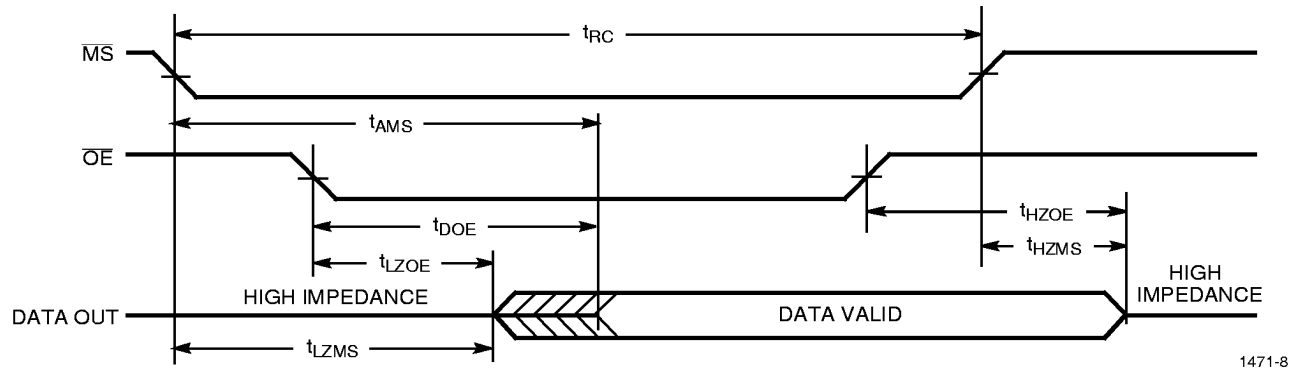
1471-7

Notes:

6. Guaranteed, not tested.
7. Device is continuously selected. $\overline{OE}$, $\overline{MS} = V_{IL}$.
8. Address valid prior to or coincident with $\overline{MS}$ transition LOW

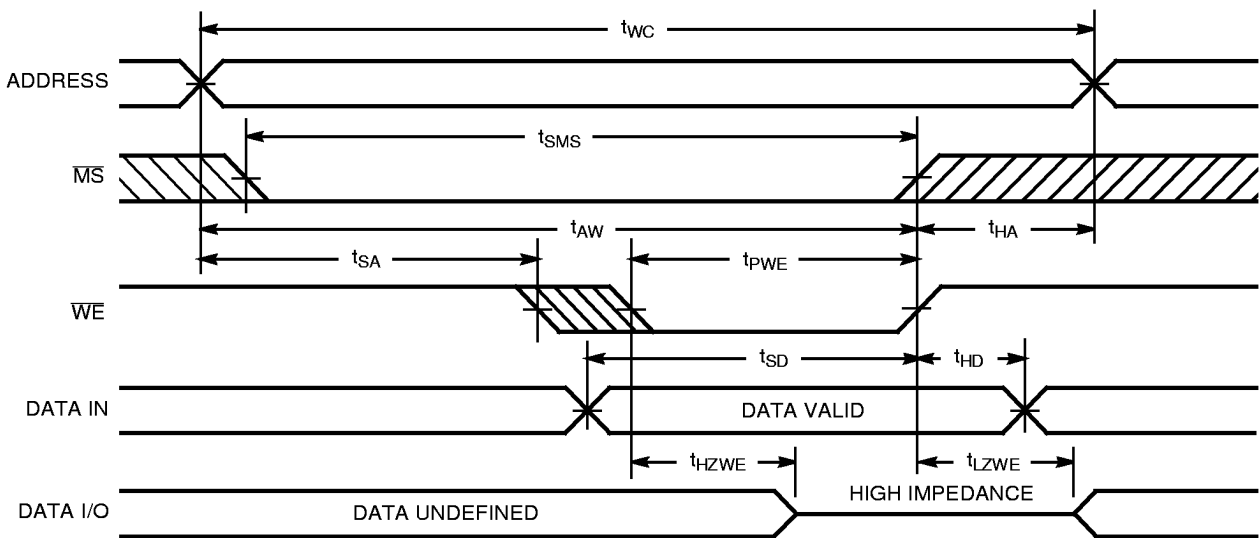
Switching Waveforms (continued)

Read Cycle No. 2^[8, 9]



1471-8

Write Cycle No. 1^[5, 10]



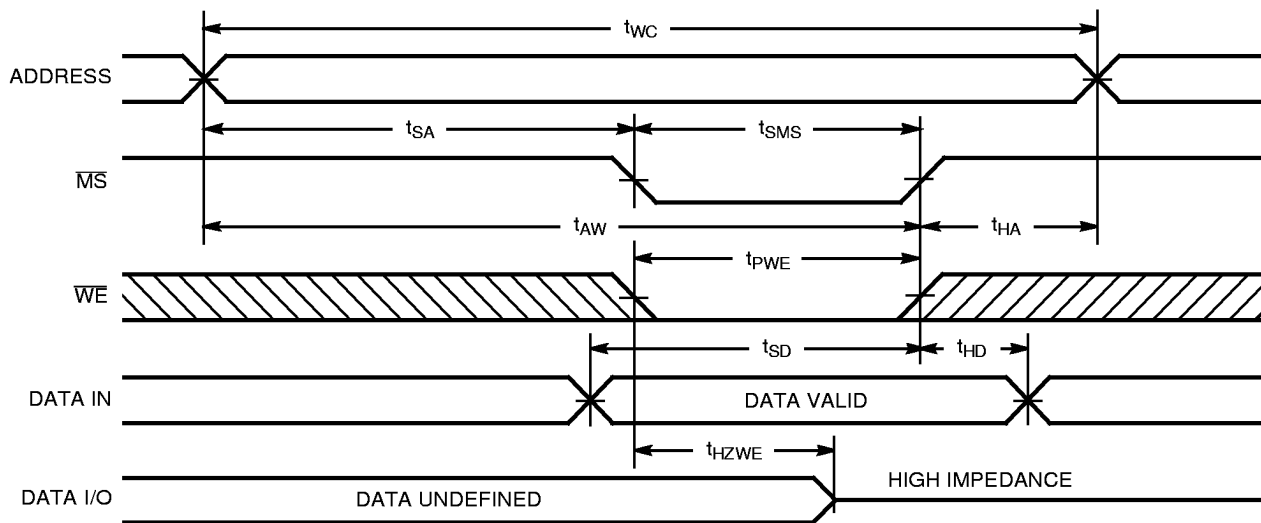
1471-9

Notes:

9. WE is HIGH for read cycle.
10. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

Switching Waveforms (continued)

Write Cycle No. 2^[5, 10, 11]



1471-10

Note:

11. If **MS** goes HIGH simultaneously with **WE** HIGH, the output remains in a high-impedance state.



Truth Table

MS	WE	OE	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

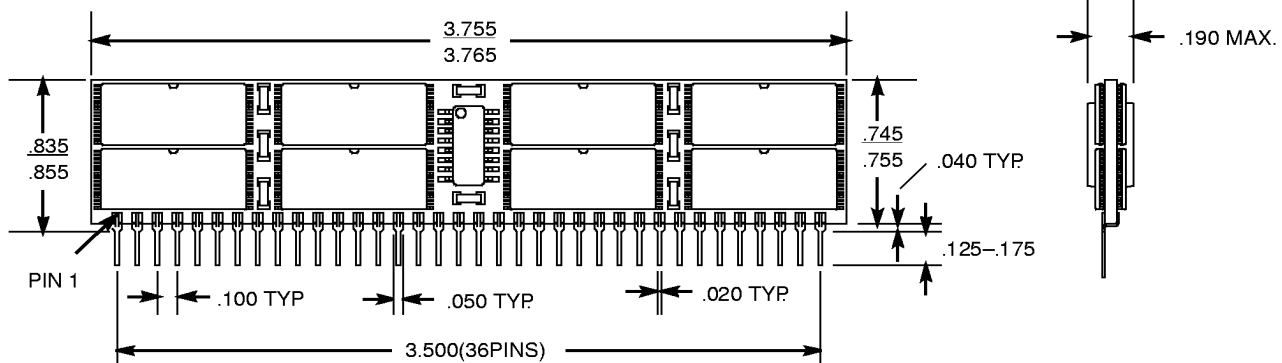
Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
70	CYM1471PS-70C	PS08	36-Pin SIP Module	Commercial
	CYM1471LPS-70C			
85	CYM1471PS-85C	PS08	36-Pin SIP Module	Commercial
	CYM1471LPS-85C			
100	CYM1471PS-100C	PS08	36-Pin SIP Module	Commercial
	CYM1471LPS-100C			
120	CYM1471PS-120C	PS08	36-Pin SIP Module	Commercial
	CYM1471LPS-120C			

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
70	CYM1481PS-70C	PS08	36-Pin SIP Module	Commercial
	CYM1481LPS-70C			
85	CYM1481PS-85C	PS06	36-Pin SIP Module	Commercial
	CYM1481LPS-85C			
100	CYM1481PS-100C	PS06	36-Pin SIP Module	Commercial
	CYM1481LPS-100C			
120	CYM1481PS-120C	PS06	36-Pin SIP Module	Commercial
	CYM1481LPS-120C			

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Package Diagrams

36-Pin SIP Module PS06



36-Pin SIP Module PS08

