Freescale Semiconductor
Data Sheet

MC3PHAC
Rev. 2, 7/2005

MC3PHAC Monolithic Intelligent Motor Controller

Overview

The MC3PHAC is a high-performance monolithic intelligent motor controller designed specifically to meet the requirements for low-cost, variable-speed, 3-phase ac motor control systems. The device is adaptable and configurable, based on its environment. It contains all of the active functions required to implement the control portion of an open loop, 3-phase ac motor drive.

One of the unique aspects of this device is that although it is adaptable and configurable based on its environment, it does not require any software development. This makes the MC3PHAC a perfect fit for customer applications requiring ac motor control but with limited or no software resources available.

The device features are:

- Volts-per-Hertz speed control
- Digital signal processing (DSP) filtering to enhance speed stability
- 32-bit calculations for high-precision operation
- Internet enabled
- No user software development required for operation
- 6-output pulse-width modulator (PWM)
- 3-phase waveform generation
- 4-channel analog-to-digital converter (ADC)
- User configurable for standalone or hosted operation
- Dynamic bus ripple cancellation
- Selectable PWM polarity and frequency
- Selectable 50/60 Hz base frequency
- Phase-lock loop (PLL) based system oscillator
- Serial communications interface (SCI)
- Low-power supply voltage detection circuit

Included in the MC3PHAC are protective features consisting of dc bus voltage monitoring and a system fault input that will immediately disable the PWM module upon detection of a system fault.

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Some target applications for the MC3PHAC include:

- Low horsepower HVAC motors
- Home appliances
- Commercial laundry and dishwashers
- Process control
- Pumps and fans

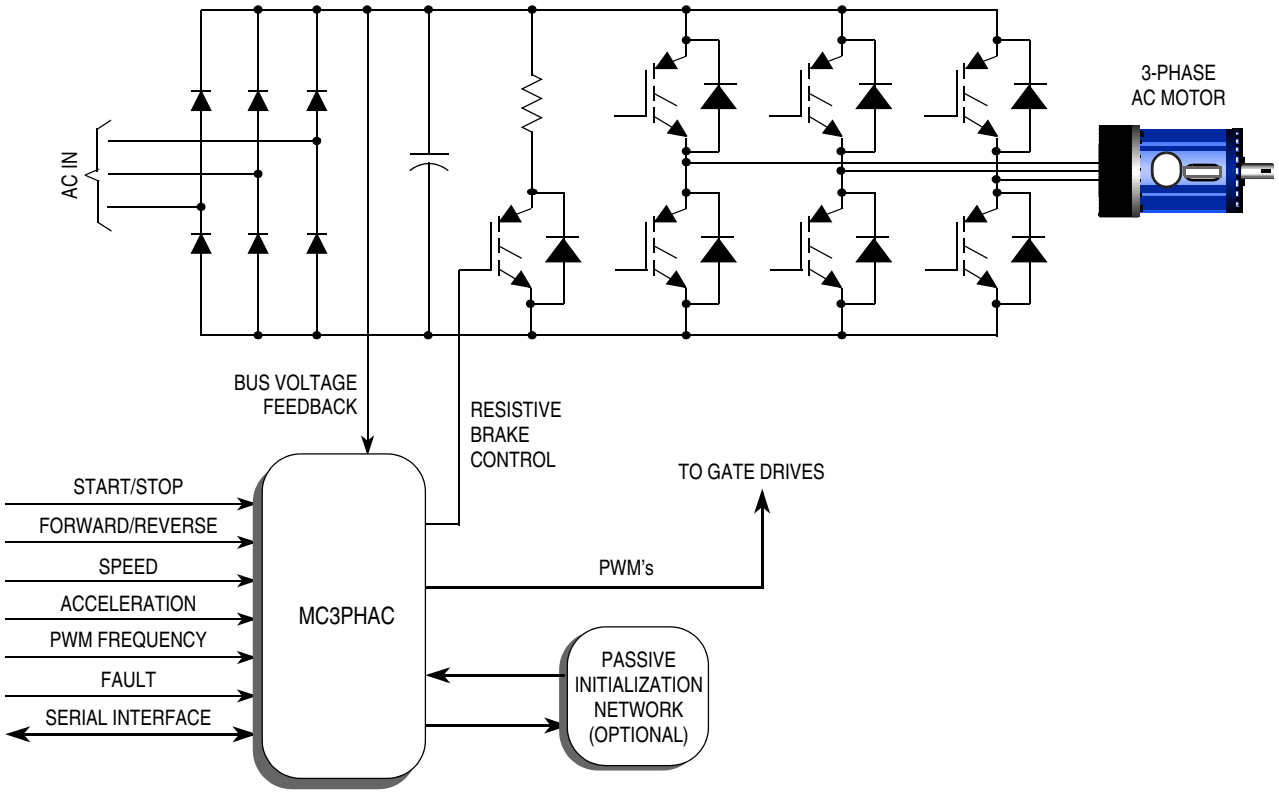


Figure 1. MC3PHAC-Based Motor Control System

As shown in Table 1, the MC3PHAC is offered in these packages:

- Plastic 28-pin dual in-line package (DIP)
- Plastic 28-pin small outline integrated circuit (SOIC)
- Plastic 32-pin quad flat pack (QFP)

Table 1. Ordering Information

Device	Operating Temperature Range	Package
MC3PHACVP	–40°C to +105°C	Plastic 28-pin DIP
MC3PHACVDW	–40°C to +105°C	Plastic 28-pin SOIC
MC3PHACVFA	–40°C to +105°C	Plastic 32-pin QFP

See Figure 2 and Figure 3 for the pin connections.

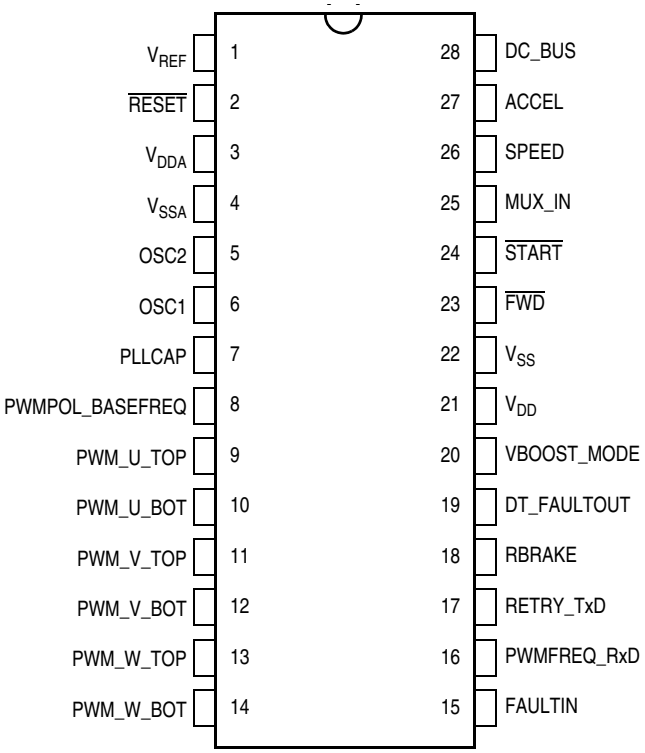


Figure 2. Pin Connections for PDIP and SOIC

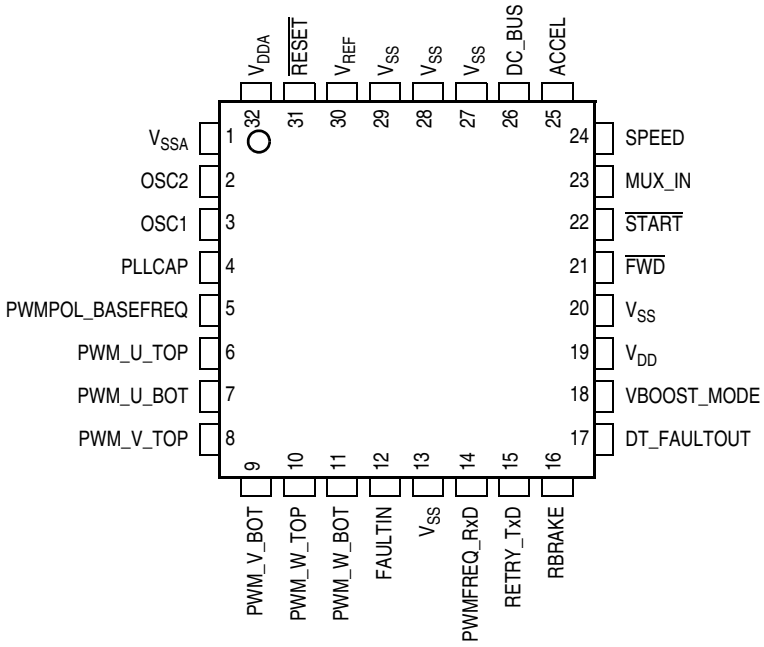


Figure 3. Pin Connections for QFP

Electrical Characteristics

Maximum Ratings

Characteristic[1]	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +6.0	V
Input voltage	V_{In}	–0.3 to V_{DD} +0.3	V
Input high voltage	V_{Hi}	V_{DD} + 0.3	V
Maximum current per pin excluding V_{DD} and V_{SS}	I	± 25	mA
Storage temperature	T_{stg}	–55 to +150	°C
Maximum current out of V_{SS}	IMV_{SS}	100	mA
Maximum current into V_{DD}	IMV_{DD}	100	mA

1. Voltages referenced to V_{SS}

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{In} and V_{Out} be constrained to the range $V_{SS} \le (V_{In}$ or $V_{Out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, either V_{SS} or V_{DD}).

Functional Operating Range

Characteristic	Symbol	Value	Unit
Operating temperature range (see Table 1)	T_A	–40°C to +105°C	°C
Operating voltage range	V_{DD}	5.0 ± 10%	V

Control Timing

Characteristic	Symbol	Value	Unit
Oscillator frequency[1]	F_{osc}	4.00 ± 1%	MHz

1. Follow the crystal/resonator manufacturer's recommendations, as the crystal/resonator parameters determine the external component values required for maximum stability and reliable starting. The load capacitance values used in the oscillator circuit design should include all stray capacitances.

DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Max	Unit
Output high voltage (I_{Load} = –2.0 mA) All I/O pins except RBRAKE	V_{OH}	V_{DD} –0.8	—	V
Output high voltage RBRAKE (I_{RBRAKE} = –15.0 mA)	V_{OHRB}	V_{DD} –1.0	—	V
Output low voltage (I_{Load} = 1.6 mA) All I/O pins except FAULTOUT and RETRY/TxD	V_{OL}	—	0.4	V
Output low voltage (I_{Load} = 15 mA) FAULTOUT and RETRY/TxD	V_{OL1}	—	1.0	V
Input high voltage All ports	V_{Hi}	0.7 x V_{DD}	V_{DD}	V
Input low voltage All ports	V_{IL}	V_{SS}	0.3 x V_{DD}	V
V_{DD} supply current	I_{DD}	—	60	mA
I/O ports high-impedance leakage current	I_{IL}	—	± 5	µA
Input current	I_{In}	—	± 1	µA
Capacitance Ports (as input or output)	C_{Out} C_{In}	— —	12 8	pF
V_{DD} low-voltage inhibit reset	V_{LVR1}	3.80	4.3	V
V_{DD} low-voltage reset/recovery hysteresis	V_{LVH1}	50	150	mV
V_{DD} power-on reset re-arm voltage	V_{POR}	3.85	4.45	V
V_{DD} power-on reset rise time ramp rate	R_{POR}	0.035	—	V/ms
Serial communications interface baud rate	SCI_{BD}	9504	9696	Bits/sec
Voltage Boost[2]	V_{Boost}	0	100	%
Dead time range[3]	DT_{Range}	0	31.875	µs
Retry time[4]	RT_{Time}	0	4.55	Hours
Acceleration rate	AC_{Rate}	0.5	128	Hz/sec
Speed control	SPEED	1	128	Hz
PWM Frequency	PWM_{FREQ}	5.291	21.164	kHz
High side power transistor drive pump-up time	T_{Pump}	99	101	ms

1. V_{DD} = 5.0 Vdc ± 10%
2. Limited in standalone mode to 0 to 35%
3. Limited in standalone mode to 0.5 to 6.0 µs
4. Limited in standalone mode to 0 to ~53 seconds

Pin Descriptions

Table 2 is a pin-by-pin functional description of the MC3PHAC. The pin numbers in the table refer to the 28-pin packages (see Figure 2).

Table 2. MC3PHAC Pin Descriptions (Sheet 1 of 2)

Pin Number	Pin Name	Pin Function
1	V_{REF}	Reference voltage input for the on-chip ADC. For best signal-to-noise performance, this pin should be tied to V_{DDA} (analog).
2	$\overline{\text{RESET}}$	A logic 0 on this pin forces the MC3PHAC to its initial startup state. All PWM outputs are placed in a high-impedance mode. Reset is a bidirectional pin, allowing a reset of the entire system. It is driven low when an internal reset source is asserted (for example, loss of clock or low V_{DD}).
3	V_{DDA}	Provides power for the analog portions of the MC3PHAC, which include the internal clock generation circuit (PLL) and the ADC
4	V_{SSA}	Returns power for the analog portions of the MC3PHAC, which include the internal clock generation circuit (PLL) and the ADC
5	OSC2	Oscillator output used as part of a crystal or ceramic resonator clock circuit.(1)
6	OSC1	Oscillator input used as part of a crystal or ceramic resonator clock circuit. Can also accept a signal from an external canned oscillator.(1)
7	PLLCAP	A capacitor from this pin to ground affects the stability and reaction time of the PLL clock circuit. Smaller values result in faster tracking of the reference frequency. Larger values result in better stability. A value of 0.1 µF is typical.
8	PWMPOL_BASEFREQ	Input which is sampled at specific moments during initialization to determine the PWM polarity and the base frequency (50 or 60 Hz)
9	PWM_U_TOP	PWM output signal for the top transistor driving motor phase U
10	PWM_U_BOT	PWM output signal for the bottom transistor driving motor phase U
11	PWM_V_TOP	PWM output signal for the top transistor driving motor phase V
12	PWM_V_BOT	PWM output signal for the bottom transistor driving motor phase V
13	PWM_W_TOP	PWM output signal for the top transistor driving motor phase W
14	PWM_W_BOT	PWM output signal for the bottom transistor driving motor phase W
15	FAULTIN	A logic high on this input will immediately disable the PWM outputs. A retry timeout interval will be initiated once this pin returns to a logic low state.
16	PWMFREQ_RxD	In standalone mode, this pin is an output that drives low to indicate the parameter mux input pin is reading an analog voltage to specify the desired PWM frequency. In PC master software mode, this pin is an input which receives UART serial data.

Table 2. MC3PHAC Pin Descriptions (Sheet 2 of 2)

Pin Number	Pin Name	Pin Function
17	RETRY_TxD	In standalone mode, this pin is an output that drives low to indicate the parameter mux input pin is reading an analog voltage to specify the time to wait after a fault before re-enabling the PWM outputs. In PC master software mode, this pin is an output that transmits UART serial data.
18	RBRAKE	Output which is driven to a logic high whenever the voltage on the dc bus input pin exceeds a preset level, indicating a high bus voltage. This signal is intended to connect a resistor across the dc bus capacitor to prevent excess capacitor voltage.
19	DT_FAULTOUT	In standalone mode, this pin is an output which drives low to indicate the parameter mux input pin is reading an analog voltage to specify the dead-time between the on states of the top and bottom PWM signals for a given motor phase. In PC master software mode, this pin is an output which goes low whenever a fault condition occurs.
20	VBOOST_MODE	At startup, this input is sampled to determine whether to enter standalone mode (logic high) or PC master software mode (logic low). In standalone mode, this pin is also used as an output that drives low to indicate the parameter mux input pin is reading an analog voltage to specify the amount of voltage boost to apply to the motor.
21	V_{DD}	+5-volt digital power supply to the MC3PHAC
22	V_{SS}	Digital power supply ground return for the MC3PHAC
23	$\overline{FWD}$	Input which is sampled to determine whether the motor should rotate in the forward or reverse direction
24	$\overline{START}$	Input which is sampled to determine whether the motor should be running.
25	MUX_IN	In standalone mode, during initialization this pin is an output that is used to determine PWM polarity and base frequency. Otherwise, it is an analog input used to read several voltage levels that specify MC3PHAC operating parameters.
26	SPEED	In standalone mode, during initialization this pin is an output that is used to determine PWM polarity and base frequency. Otherwise, it is an analog input used to read a voltage level corresponding to the desired steady-state speed of the motor.
27	ACCEL	In standalone mode, during initialization this pin is an output that is used to determine PWM polarity and base frequency. Otherwise, it is an analog input used to read a voltage level corresponding to the desired acceleration of the motor.
28	DC_BUS	In standalone mode, during initialization this pin is an output that is used to determine PWM polarity and base frequency. Otherwise, it is an analog input used to read a voltage level proportional to the dc bus voltage.

1. Correct timing of the MC3PHAC is based on a 4.00 MHz crystal or ceramic resonator. Follow the crystal/resonator manufacturer's recommendations, as the crystal/resonator parameters determine the external component values required for maximum stability and reliable starting. The load capacitance values used in the oscillator circuit design should include all stray capacitances.

Introduction

The MC3PHAC is a high-performance intelligent controller designed specifically to meet the requirements for low-cost, variable-speed, 3-phase ac motor control systems. The device is adaptable and configurable, based on its environment. Constructed with high-speed CMOS (complementary metal-oxide semiconductor) technology, the MC3PHAC offers a high degree of performance and ruggedness in the hostile environments often found in motor control systems.

The device consists of:

- 6-output pulse-width modulator (PWM)
- 4-channel analog-to-digital converter (ADC)
- Phase-lock loop (PLL) based system oscillator
- Low-power supply voltage detection circuit
- Serial communications interface (SCI)

The serial communications interface is used in a mode, called PC master software mode, whereby control of the MC3PHAC is from a host or master personal computer executing PC master software or a microcontroller emulating PC master software commands. In either case, control via the internet is feasible.

Included in the MC3PHAC are protective features consisting of dc bus monitoring and a system fault input that will immediately disable the PWM module upon detection of a system fault.

Included motor control features include:

- Open loop volts/Hertz speed control
- Forward or reverse rotation
- Start/stop motion
- System fault input
- Low-speed voltage boost
- Internal power-on reset (POR)

Features

3-Phase Waveform Generation — The MC3PHAC generates six PWM signals which have been modulated with variable voltage and variable frequency information in order to control a 3-phase ac motor. A third harmonic signal has been superimposed on top of the fundamental motor frequency to achieve full bus voltage utilization. This results in a 15 percent increase in maximum output amplitude compared to pure sine wave modulation.

The waveform is updated at a 5.3 kHz rate (except when the PWM frequency is 15.9 kHz), resulting in near continuous waveform quality. At 15.9 kHz, the waveform is updated at 4.0 kHz.

DSP Filtering — A 24-bit IIR digital filter is used on the SPEED input signal in standalone mode, resulting in enhanced speed stability in noisy environments. The sampling period of the filter is 3 ms (except when the PWM frequency is 15.9 kHz) and it mimics the response of a single pole analog filter having a pole at 0.4 Hz. At a PWM frequency of 15.9 kHz, the sampling period is 4 ms and the pole is located at 0.3 Hz.

High Precision Calculations — Up to 32-bit variable resolution is employed for precision control and smooth performance. For example, the motor speed can be controlled with a resolution of 4 mHz.

Smooth Voltage Transitions — When the commanded speed of the motor passes through ±1 Hz, the voltage is gently applied or removed depending on the direction of the speed change. This eliminates any pops or surges that may occur, especially under conditions of high-voltage boost at low frequencies.

High-Side Bootstrapping — Many motor drive topologies (especially high-voltage drives) use optocouplers to supply the PWM signal to the high-side transistors. Often, the high-side transistor drive circuitry contains a charge pump circuit to create a floating power supply for each high-side transistor that is dependent on low-side PWMs to develop power. When the motor has been off for a period of time, the charge on the high-side power supply capacitor is depleted and must be replenished before proper PWM operation can resume.

To accommodate such topologies, the MC3PHAC will always provide 100 ms of 50 percent PWM drive to only the low-side transistors each time the motor is turned on. Since the top transistors remain off during this time, it has the effect of applying zero volts to the motor, and no motion occurs. After this period, motor waveform modulation begins, with PWM drive also being applied to the high-side transistors.

Fast Velocity Updating — During periods when the motor speed is changing, the rate at which the velocity is updated is critical to smooth operation. If these updates occur too infrequently, a ratcheting effect will be exhibited on the motor, which inhibits smooth torque performance. However, velocity profiling is a very calculation intensive operation to perform, which runs contrary to the previous requirement.

In the MC3PHAC, a velocity pipelining technique is employed which allows linear interpolation of the velocity values, resulting in a new velocity value every 189 μs (252 μs for 15.9 kHz PWMs). The net result is ultra smooth velocity transitions, where each velocity step is not perceivable by the motor.

Dynamic Bus Ripple Cancellation — The dc bus voltage is sensed by the MC3PHAC, and any deviations from a predetermined norm (3.5 V on the dc bus input pin) result in corrections to the PWM values to counteract the effect of the bus voltage changes on the motor current. The frequency of this calculation is sufficiently high to permit compensation for line frequency ripple, as well as slower bus voltage changes resulting from regeneration or brown out conditions. See Figure 4.

Selectable Base Frequency — Alternating current (ac) motors are designed to accept rated voltage at either 50 or 60 Hz, depending on what region of the world they were designed to be used. The MC3PHAC can accommodate both types of motors by allowing the voltage profile to reach maximum value at either 50 or 60 Hz. This parameter can be specified at initialization in standalone mode, or it can be changed at any time in PC master software mode.

Selectable PWM Polarity — The polarity of the PWM outputs may be specified such that a logic high on a PWM output can either be the asserted or negated state of the signal. In standalone mode, this parameter is specified at initialization and applies to all six PWM outputs. In PC master software mode, the polarity of the top PWM signals can be specified separately from the polarity of the bottom PWM signals.

This specification can be done at any time, but once it is done, the polarities are locked and cannot be changed until a reset occurs. Also, any commands from PC master software that would have the effect of enabling PWMs are prevented by the MC3PHAC until the polarity has been specified.

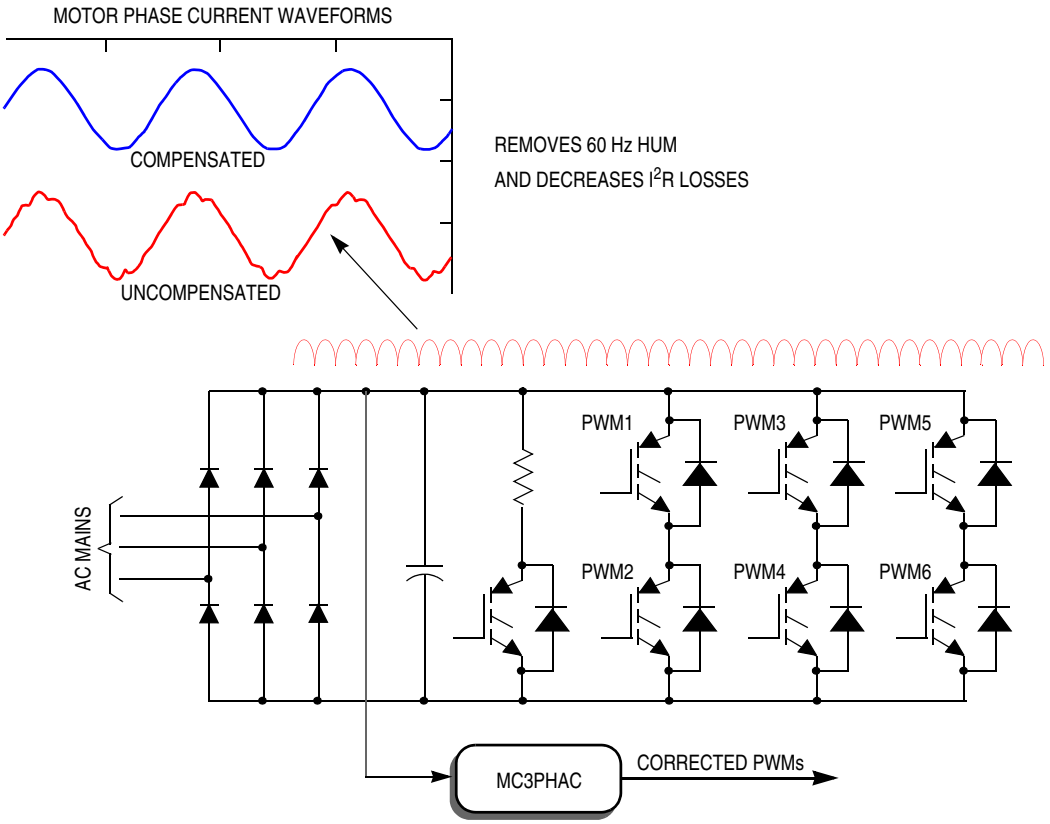


Figure 4. Dynamic Bus Ripple Cancellation

In standalone mode, the base frequency and PWM polarity are specified at the same time during initialization by connecting either pin 25, 26, 27, or 28 exclusively to the PWMPOL_BASEFREQ input. During initialization, pins 25, 26, 27, and 28 are cycled one at a time to determine which one has been connected to the PWMPOL_BASEFREQ input.

Table 3 shows the selected PWM polarity and base frequency as a function of which pin connection is made. Refer to the standalone mode schematic, Figure 8. Only one of these jumpers (JP1–JP4) can be connected at any one time.

NOTE

It is not necessary to break this connection once the initialization phase has been completed. The MC3PHAC will function properly while this connection is in place.

Table 3. PWM Polarity and Base Frequency Specification in Standalone Mode

Pin Connected to PWMPOL_BASEFREQ Pin	PWM Polarity	Base Frequency
MUX_IN (JP1)	Logic low = on	50 Hz
SPEED (JP2)	Logic high = on	50 Hz
ACCEL (JP3)	Logic low = on	60 Hz
DC_BUS (JP4)	Logic high = on	60 Hz

Selectable PWM Frequency — The MC3PHAC accommodates four discrete PWM frequencies and can be changed dynamically while the motor is running. This resistor can be a potentiometer or a fixed resistor in the range shown in Table 4. In standalone mode, the PWM frequency is specified by applying a voltage to the MUX_IN pin while the PWMFREQ_RxD pin is being driven low. Table 4 shows the required voltage levels on the MUX_IN pin and the associated PWM frequency for each voltage range.

NOTE

The PWM frequencies are based on a 4.00 MHz frequency applied to the oscillator input.

Table 4. MUX_IN Resistance Ranges and Corresponding PWM Frequencies

Voltage Input	PWM Frequency
0 to 1 V	5.291 kHz
1.5 to 2.25 V	10.582 kHz
2.75 to 3.5 V	15.873 kHz
4 to 5 V	21.164 kHz

Selectable PWM Dead Time — Besides being able to specify the PWM frequency, the blanking time interval between the on states of the complementary PWM pairs can also be specified. Refer to the graph in Figure 9 for the resistance value versus dead time. Figure 9 assumes a 6.8 kΩ ±5% pullup resistor. In standalone mode, this is done by

supplying a voltage to the MUX_IN pin while the DT_FAULTOUT pin is being driven low. In this way, dead time can be specified with a scaling factor of 2.075 µs per volt, with a minimum value of 0.5 µs. In PC master software mode, this value can be selected to be anywhere between 0 and 32 µs.

In both standalone and PC master software modes, the dead time value can be written only once. Further updates of this parameter are locked out until a reset condition occurs.

Speed Control — The synchronous motor frequency can be specified in real time to be any value from 1 Hz to 128 Hz by the voltage applied to the SPEED pin. The scaling factor is 25.6 Hz per volt. This parameter can also be controlled directly from PC master software in real time.

The SPEED pin is processed by a 24-bit digital filter to enhance the speed stability in noisy environments. This filter is only activated in standalone mode.

Acceleration Control — Motor acceleration can be specified in real time to be in the range from 0.5 Hz/second, ranging to 128 Hz/second, by the voltage applied to the ACCEL pin. The scaling factor is 25.6 Hz/second per volt. This parameter can also be controlled directly from PC master software in real time.

Voltage Profile Generation — The MC3PHAC controls the motor voltage in proportion to the specified frequency, as indicated in Figure 5.

An ac motor is designed to draw a specified amount of magnetizing current when supplied with rated voltage at the base frequency. As the frequency decreases, assuming no stator losses, the voltage must decrease in exact proportion to maintain the required magnetizing current. In reality, as the frequency decreases, the voltage drop in the series stator resistance increases in proportion to the voltage across the magnetizing inductance. This has the effect of further reducing the voltage across the magnetizing inductor, and consequently, the magnetizing current. A schematic representation of this effect is

illustrated in Figure 6. To compensate for this voltage loss, the voltage profile is boosted over the normal voltage curve in Figure 5, so that the magnetizing current remains constant over the speed range.

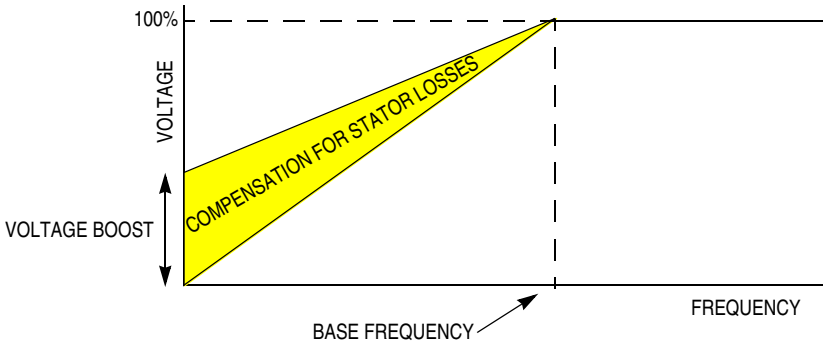


Figure 5. Voltage Profiling, Including Voltage Boost

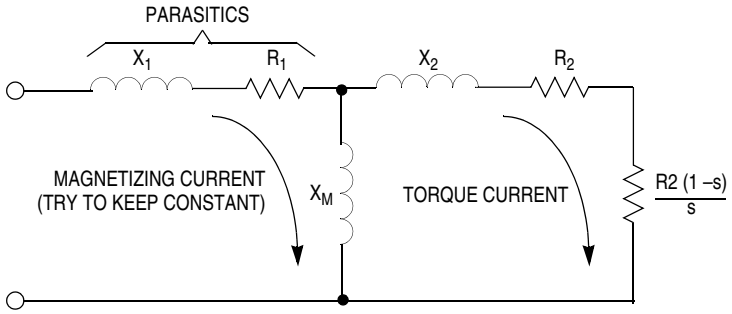


Figure 6. AC Motor Single Phase Model Showing Parasitic Stator Impedances

The MC3PHAC allows the voltage boost to be specified as a percentage of full voltage at 0 Hz, as shown in Figure 5. In standalone mode, voltage boost is specified during the initialization phase by supplying a voltage to the MUX_IN pin while the VBOOST_MODE pin is being driven low. Refer to the graph in Figure 11 for the resistance value versus voltage boost. Figure 11 assumes a 6.8 kΩ pullup resistor. In this way, voltage boost can be specified from 0 to 40 percent, with a scaling factor of 8 percent per volt. In PC master software mode, the voltage boost can be specified from 0 to 100 percent and can be changed at anytime.

By using the voltage boost value, and the specified base frequency, the MC3PHAC has all the information required to generate a voltage profile automatically based on the generated waveform frequency. An additional feature exists in PC master software mode whereby this voltage value can be overridden and controlled in real time. Specifying a voltage lower than the normal volts-per-hertz profile permits a softer torque response in certain ergonomic situations. It also allows for load power factor control and higher operating efficiencies with high inertia loads or other loads where instantaneous changes in torque demand are not permitted. Details of this feature are discussed in the PC Master Software Operation with the MC3PHAC.

PLL Clock Generation — The OSC1 pin signal is used as a reference clock for an internal PLL clocking circuit, which is used to drive the internal clocks of the MC3PHAC. This provides excellent protection against noise spikes that may occur on the OSC1 pin. In a clocking circuit that does not incorporate a PLL, a noise spike on the clock input can create a clock edge, which violates the setup times of the clocking

logic, and can cause the device to malfunction. The same noise spike applied to the input of a PLL clock circuit is perceived by the PLL as a change in its reference frequency, and the PLL output frequency begins to change in an attempt to lock on to the new frequency. However, before any appreciable change can occur, the spike is gone, and the PLL settles back into the true reference frequency.

Fault Protection — The MC3PHAC supports an elaborate range of fault protection and prevention features. If a fault does occur, the MC3PHAC immediately disables the PWMs and waits until the fault condition is cleared before starting a timer to re-enable the PWMs. Refer to the graph in Figure 10 for the resistance value versus retry time. Figure 10 assumes a 6.8 kΩ pullup resistor. In standalone mode, this timeout interval is specified during the initialization phase by supplying a voltage to the MUX_IN pin while the RETRY_TxD pin is being driven low. In this way, the retry time can be specified from 1 to 60 seconds, with a scaling factor of 12 seconds per volt. In PC master software mode, the retry time can be specified from 0.25 second to over 4.5 hours and can be changed at any time.

The fault protection and prevention features are:

- **External Fault Monitoring** — The FAULTIN pin accepts a digital signal that indicates a fault has been detected via external monitoring circuitry. A high level on this input results in the PWMs being immediately disabled. Typical fault conditions might be a dc bus over voltage, bus over current, or over temperature. Once this input returns to a logic low level, the fault retry timer begins running, and PWMs are re-enabled after the programmed timeout value is reached.
- **Lost Clock Protection** — If the signal on the OSC1 pin is lost altogether, the MC3PHAC will immediately disable the PWM outputs to protect the motor and power electronics. This is a special fault condition in that it will also cause the MC3PHAC to be reset. Lost clock detection is an important safety consideration, as many safety regulatory agencies are now requiring a dead crystal test be performed as part of the certification process.
- **Low V_{DD} Protection** — Whenever V_{DD} falls below V_{LVR1}, an on-board power supply monitor will reset the MC3PHAC. This allows the MC3PHAC to operate properly with 5 volt power supplies of either 5 or 10 percent tolerance.
- **Bus Voltage Integrity Monitoring** — The DC_BUS pin is monitored at a 5.3 kHz frequency (4.0 kHz when the PWM frequency is set to 15.9 kHz), and any voltage reading outside of an acceptable window constitutes a fault condition. In standalone mode, the window thresholds are fixed at 4.47 volts (128 percent of nominal), and 1.75 volts (50 percent of nominal), where nominal is defined to be 3.5 volts. In PC master software mode, both top and bottom window thresholds can be set independently to any value between 0 volts (0 percent of nominal), and greater than 5 volts (143 percent of nominal), and can be changed at any time. Once the DC_BUS signal level returns to a value within the acceptable window, the fault retry timer begins running, and PWMs are re-enabled after the programmed timeout value is reached.

  During power-up, it is possible that V_{DD} could reach operating voltage before the dc bus capacitor charges up to its nominal value. When the dc bus integrity is checked, an under voltage would be detected and treated as a fault, with its associated timeout period. To prevent this, the MC3PHAC monitors the dc bus voltage during power-up in standalone mode, and waits until it is higher than the under voltage threshold before continuing. During this time, all MC3PHAC functions are suspended. Once this threshold is reached, the MC3PHAC will continue normally, with any further under voltage conditions treated as a fault.

  If dc bus voltage monitoring is not desired, a voltage of 3.5 volts ± 5 percent should be supplied to the DC_BUS pin through an impedance of between 4.7 kΩ and 15 kΩ.

- **Regeneration Control** — Regeneration is a process by which stored mechanical energy in the motor and load is transferred back into the drive electronics, usually as a result of an aggressive deceleration operation. In special cases where this process occurs frequently (for example, elevator motor control systems), it is economical to incorporate special features in the motor drive to allow this energy to be supplied back to the ac mains. However, for most low cost ac drives, this energy is stored in the dc bus capacitor by increasing its voltage. If this process is left unchecked, the dc bus voltage can rise to dangerous levels, which can destroy the bus capacitor or the transistors in the power inverter.

  The MC3PHAC incorporates two techniques to deal with regeneration before it becomes a problem:

  – **Resistive Braking** — The DC_BUS pin is monitored at a 5.3 kHz frequency (4.0 kHz when the PWM frequency is set to 15.9 kHz), and when the voltage reaches a certain threshold, the RBRAKE pin is driven high. This signal can be used to control a resistive brake placed across the dc bus capacitor, such that mechanical energy from the motor will be dissipated as heat in the resistor versus being stored as voltage on the capacitor. In standalone mode, the DC_BUS threshold required to assert the RBRAKE signal is fixed at 3.85 volts (110 percent of nominal) where nominal is defined to be 3.5 volts. In PC master software mode, this threshold can be set to any value between 0 volts (0 percent of nominal) and greater than 5 volts (143 percent of nominal) and can be changed at any time.

  – **Automatic Deceleration Control** — When decelerating the motor, the MC3PHAC attempts to use the specified acceleration value for deceleration as well. If the voltage on the DC_BUS pin reaches a certain threshold, the MC3PHAC begins to moderate the deceleration as a function of this voltage, as shown in Figure 7. The voltage range on the DC_BUS pin from when the deceleration begins to decrease, to when it reaches 0, is 0.62 volts. In standalone mode, the DC_BUS voltage where deceleration begins to decrease is fixed at 3.85 volts (110 percent of nominal) where nominal is defined to be 3.5 volts. In PC master software mode, this threshold can be set to any value between 0 volts (0 percent of nominal) and greater than 5 volts (143 percent of nominal) and can be changed at any time.

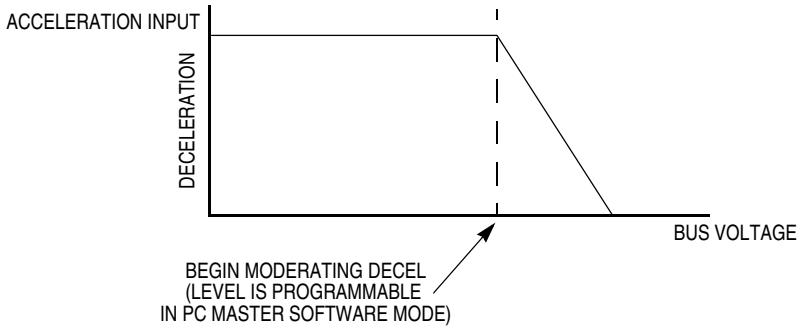


Figure 7. Deceleration as a Function of Bus Voltage

Digital Power Supply Bypassing

V_{DD} and V_{SS} are the digital power supply and ground pins for the MC3PHAC.

Fast signal transitions connected internally on these pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the V_{DD} and V_{SS} pins. Place the bypass capacitors as close as possible to the MC3PHAC. Use a high-frequency-response ceramic capacitor, such as a 0.1 μF, paralleled with a bulk capacitor in the range of 1 μF to 10 μF for bypassing the digital power supply.

Analog Power Supply Bypassing

V_{DDA} and V_{SSA} are the power supply pins for the analog portion of the clock generator and analog-to-digital converter (ADC). On the schematics in this document, analog ground is labeled with an A and other grounds are digital grounds. Analog power is labeled as +5 A. It is good practice to isolate the analog and digital +5 volt power supplies by using a small inductor or a low value resistor less than 5 ohms in series with the digital power supply, to create the +5 A supply. ADC V_{REF} is the power supply pin used for setting the ADC's voltage reference.

Decoupling of these pins should be per the digital power supply bypassing, described previously. ADC V_{REF} (pin 1) and V_{DDA} (pin 3) shall be connected together and connected to the same potential as V_{DD}.

Grounding Considerations

Printed circuit board layout is an important design consideration. In particular, ground planes and how grounds are tied together influence noise immunity. To maximize noise immunity, it is important to get a good ground plane under the MC3PHAC. It is also important to separate analog and digital grounds. That is why, shown on the schematics, there are two ground designations, analog ground is marked with an A and other grounds are digital grounds. GND is the digital ground plane and power supply return. GNDA is the analog circuit ground. They are both the same reference voltage, but are routed separately, and tie together at only one point.

Power-Up/Power-Down

When power is applied or removed, it is important that the inverter's top and bottom output transistors in the same phase are not turned on simultaneously. Since logic states are not always defined during power-up, it is important to ensure that all power transistors remain off when the controller's supply voltage is below its normal operating level. The MC3PHAC's PWM module outputs make this easy by switching to a high impedance configuration whenever the 5-volt supply is below its specified minimum.

The user should use pullup or pulldown resistors on the output of the MC3PHAC's PWM outputs to ensure during power-up and power-down, that the inverter's drive inputs are at a known, turned off, state.

Operation

The MC3PHAC motor controller will operate in two modes. The first is standalone operation, whereby the MC3PHAC can be used without any intervention from an external personal computer. In standalone mode, the MC3PHAC is initialized by passive devices connected to the MC3PHAC and input to the system at power-up/reset time. In standalone mode, some parameters continue to be input to the system as it operates. Speed, PWM frequency, bus voltage, and acceleration parameters are input to the system on a real-time basis.

The second mode of operation is called PC master software mode.That operational mode requires the use of a personal computer and PC master software executing on the personal computer, communicating with the MC3PHAC, or a microcontroller emulating PC master software commands. All command and setup information is input to the MC3PHAC via the PC host.

Standalone Operation

If the VBOOST_MODE pin is high when the MC3PHAC is powered up, or after a reset, the MC3PHAC enters standalone mode. In this mode of operation, the functionality of many of the MC3PHAC pins change so that the device can control a motor without requiring setup information from an external master. When operated in standalone mode, the MC3PHAC will drive certain pins corresponding to parameters which must be specified, while simultaneously monitoring the response on other pins.

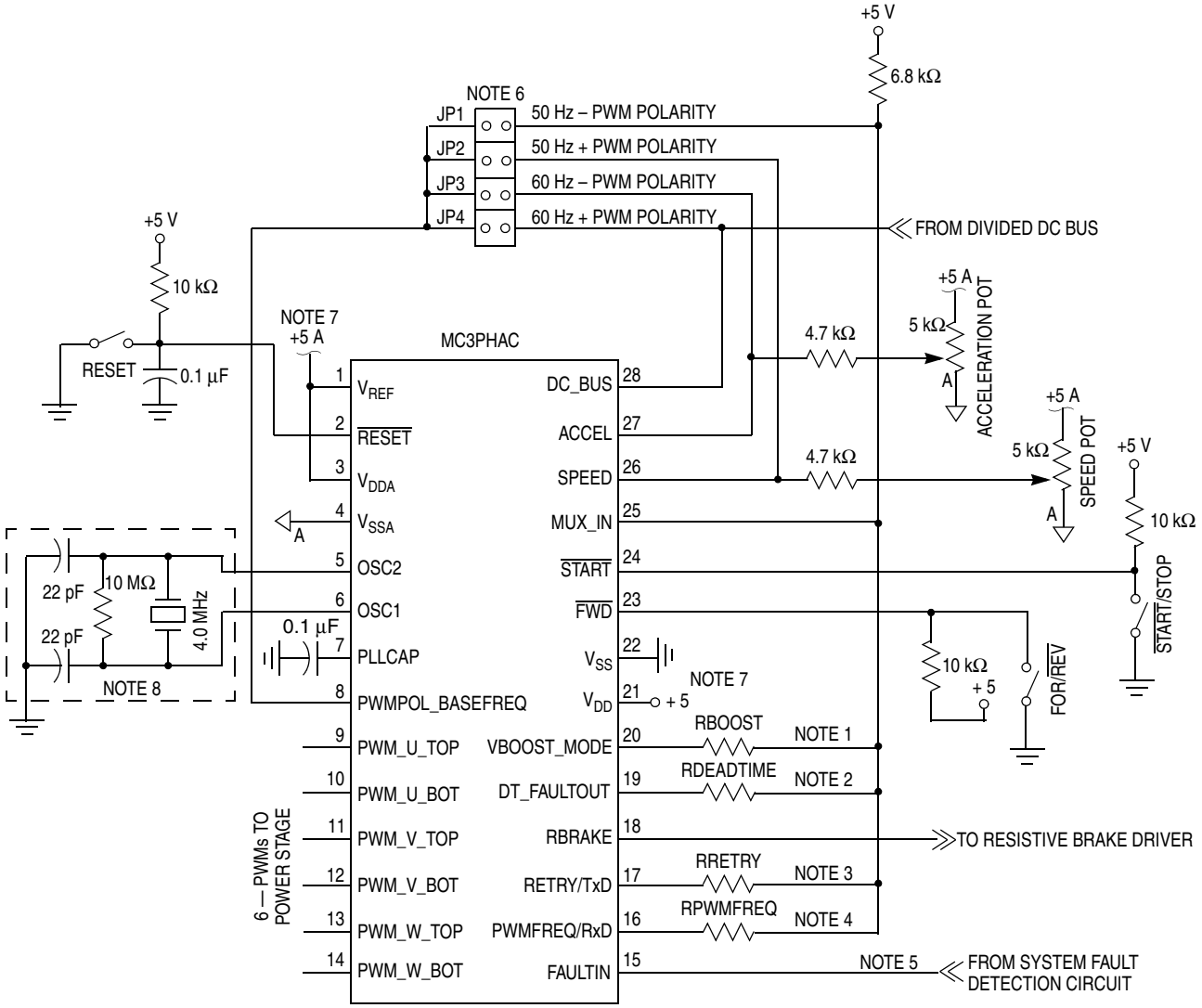
In many cases, the parameter to be specified is represented as an analog voltage presented to the MUX_IN pin, while certain other pins are driven low. In so doing, the MC3PHAC can accommodate an external analog mux which will switch various signals on the MUX_IN pin when the signal select line goes low. All signals must be in a range between 0 V and V_{REF}. As an economical alternative, an external passive network can be connected to each of the parameter select output pins and the MUX_IN pin, as shown in Figure 8.

The Thevenin equivalent impedance of this passive network as seen by the MUX_IN pin is very important and should be in the range of 5 kΩ to 10 kΩ. If the resistance is too high, leakage current from the input/output (I/O) pins will cause an offset voltage that will affect the accuracy of the reading. If the resistance is too low, the parameter select pins will not be able to sink the required current for an accurate reading. Using a pullup resistor value of 6.8 kΩ (as indicated in Figure 8), the resulting value for each parameter as a function of the corresponding pulldown resistor value is shown in Figure 9, Figure 10, Figure 11, and Table 4.

The START input pin is debounced internally and a switch can be directly accommodated on this pin. The input is level sensitive, but a logic 1 level must exist on the pin before a logic 0 level will be processed as a start signal. This will prevent an accidental motor startup in the event of the MC3PHAC being powered up, where the switch was left in the start position.

The $\overline{\text{FWD}}$ input pin is debounced internally and can directly accommodate a switch connection. The input is also level sensitive.

Figure 8 shows the jumper arrangement connected to the PWMPOL_BASEFREQ input pin. For proper operation, one and only one jumper connection can be made at any given time. Table 3 shows the polarity and base frequency selections as a function of the jumper connection.



Notes:
1. See Figure 11.
2. See Figure 9.
3. See Figure 10.
4. See Table 4.
5. If no external fault circuit is provided, connect to V_{SS}.
6. Connect only one jumper.
7. Use bypass capacitors placed close to the MC3PHAC.
8. Consult crystal/resonator manufacturer for component values.

Figure 8. Standalone MC3PHAC Configuration

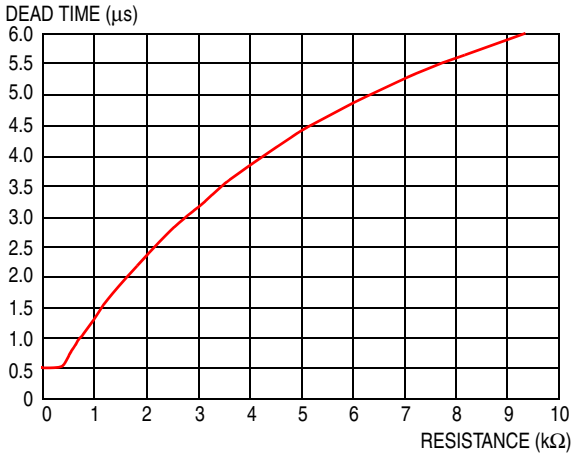


Figure 9. Dead Time as a Function of the RDEADTIME Resistor

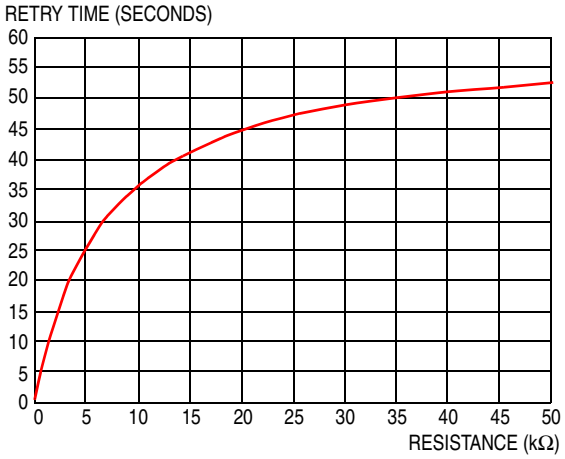


Figure 10. Fault Retry Time as a Function of the RRETRY Resistor

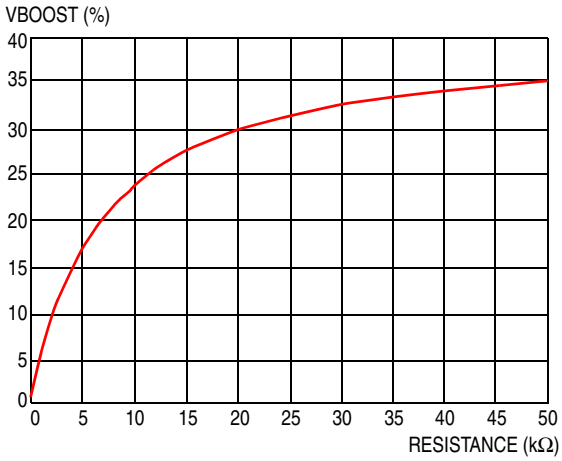


Figure 11. Voltage Boost as a Function of the RBOOST Resistor

Standalone Application Example

Figure 12 shows an application example of the MC3PHAC, configured in standalone mode. Resistor values and jumpers have been selected to provide the following performance:

1. Base frequency of 60 Hz and positive PWM polarity (from Table 3)
2. PWM frequency resistor 3.9 kΩ, which implies 10.582 kHz from Table 4). (5v/(3.9k + 6.8k))*3.9k = 1.82 volts
3. Dead-time resistor = 5.1 kΩ, which implies 4.5 µs (from Figure 9)
4. Fault retry time resistor = 8.2 kΩ, which implies 32.8 seconds (from Figure 10).
5. Voltage boost resistor = 12 kΩ, which implies 25.5 percent (from Figure 11).
6. The wiper of the acceleration potentiometer is set at 2.5 V = 64 Hz/second acceleration rate (from the Acceleration Control description on page 11.) The potentiometer, in this case, could have been a resistor divider. If a resistor divider is used in place of the acceleration potentiometer, keep the total resistance of the two resistors less than 10 kΩ. Always use 4.7kΩ in series with the center of the acceleration voltage divider resistors, connected to the ACCEL (pin 27) as shown in the application example, Figure 12.
7. Crystal/resonator capacitor values are typical values from the manufacturer. Refer to the manufacturers data for actual values.

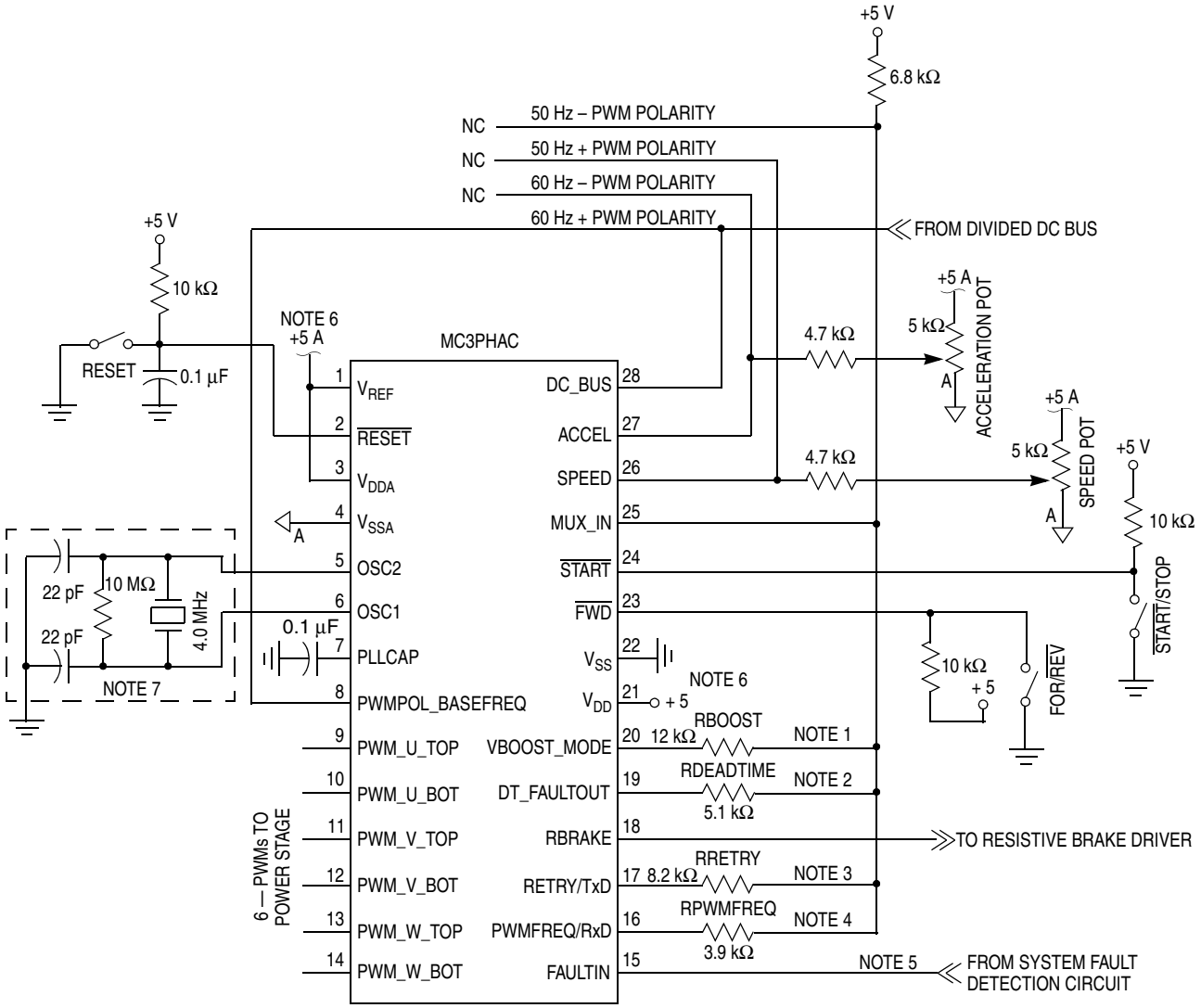
PC Master Software Operation

Introduction to PC Master Host Software

The MC3PHAC is compatible with Freescale's PC master host software serial interface protocol. Communication occurs over an on-chip UART, on the MC3PHAC at 9600 baud to an external master device, which may be a microcontroller that also has an integrated UART or a personal computer via a COM port. With PC master software, an external controller can monitor and control all aspects of the MC3PHAC operation.

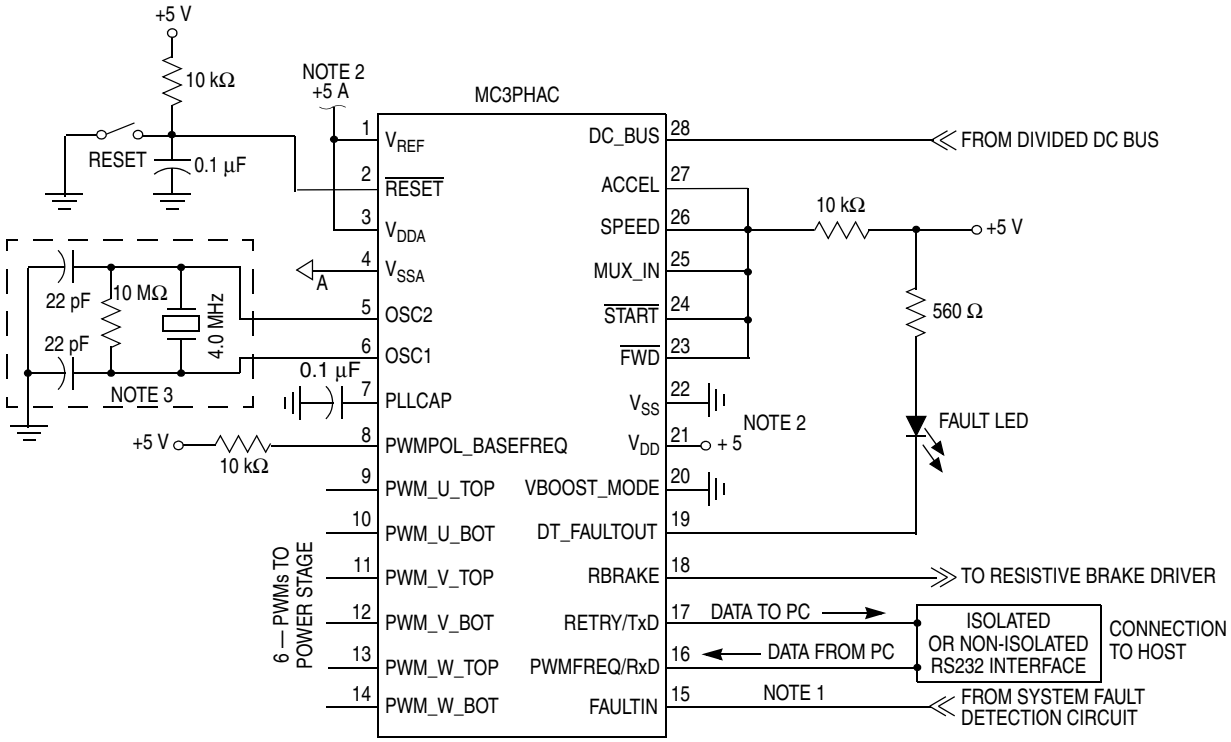
When the MC3PHAC is placed in PC master software mode, all control of the system is provided through the integrated UART, resident on the MC3PHAC. Inputs such as START, $\overline{\text{FWD}}$, SPEED, ACCEL, MUX_IN, and PWMPOL_BASEFREQ have no controlling influence over operation of the system. Even though the SPEED, START, and $\overline{\text{FWD}}$ inputs are disabled while the system is in PC master software mode, through PC master software, it is possible to monitor the state of those inputs.

The most popular master implementation is a PC, where a graphical user interface (GUI) has been layered on top of the PC master software command protocol, complete with a graphical data display, and an ActiveX interface. Figure 13 shows the MC3PHAC configured in PC master software mode. It is beyond the scope of this document to describe the PC master software protocol or its implementation on a personal computer. For further information on these topics, refer to other Freescale documents relating to the PC master software protocol and availability of PC master host software.



Notes:
1. See Figure 11.
2. See Figure 9.
3. See Figure 10.
4. See Table 4.
5. If no external fault circuit is provided, connect to V_{SS}.
6. Use bypass capacitors placed close to the MC3PHAC.
7. Consult crystal/resonator manufacturer for component values.

Figure 12. MC3PHAC Application Example in Standalone Mode



Notes:
1. If no external fault circuit is provided, connect to V_{SS}.
2. Use bypass capacitors placed close to the MC3PHAC.
3. Consult crystal/resonator manufacturer for component values.

Figure 13. MC3PHAC Configuration for Using a PC as a Master

PC Master Software Operation with the MC3PHAC

When power is first applied to the MC3PHAC, or if a logic low level is applied to the $\overline{\text{RESET}}$ pin, the MC3PHAC enters PC master software mode if the VBOOST_MODE pin is low during the initialization phase. The MC3PHAC recognizes a subset of the PC master software command set, which is listed in Table 5.

Table 5. Recognized PC Host Software Commands

Command	Description
GETINFOBRIEF	MC3PHAC responds with brief summary of hardware setup and link configuration information
READVAR8	MC3PHAC reads an 8-bit variable at a specified address and responds with its value
READVAR16	MC3PHAC reads a 16-bit variable at a specified address and responds with its value
READVAR32	MC3PHAC reads a 32-bit variable at a specified address and responds with its value
WRITEVAR8	MC3PHAC writes an 8-bit variable at a specified address
WRITEVAR16	MC3PHAC writes a 16-bit variable at a specified address

With the READVARx commands, the addresses are checked for validity, and the command is executed only if the address is within proper limits. In general, a read command with an address value below $0060 or above $EE03 will not execute properly, but instead will return an invalid operation response. An

exception to this rule is that PC master software allows reading locations $0001, $0036 and $FE01, which are PORTB data register, Dead Time register and SIM Reset Status registers respectively. The addresses for the WRITEVARx commands are checked for validity, and the data field is also limited to a valid range for each variable. See Table 6 for a list of valid data values and valid write addresses.

User interface variables and their associated PC master software addresses within the MC3PHAC are listed in Table 6.

Table 6. User Interface Variables for Use with PC Master Software

Name	Address	Read/ Write	Size (Bytes)	Description	Valid Data
Commanded direction	$1000	W	1	Determines whether the motor should go forward, reverse, or stop	Forward — $10 Reverse — $11 Stop — $20
Command reset	$1000	W	1	Forces the MC3PHAC to perform an immediate reset	$30
Commanded PWM frequency(1)	$1000	W	1	Specifies the frequency of the MC3PHAC PWM frequency	5.3 kHz — $41 10.6 kHz — $42 15.9 kHz — $44 21.1 kHz — $48
Measured PWM period	$00A8	R	2	The modulus value supplied to the PWM generator used by the MC3PHAC — value is multiplied by 250 ns to obtain PWM period	$00BD–$05E8
Commanded PWM polarity(2), (3), (4)	$1000	W	1	Specifies the polarity of the MC3PHAC PWM outputs. This is a write once parameter after reset. Example: $50 = Bottom and top PWM outputs are positive polarity.	B + T + $50 B + T – $54 B – T + $58 B – T – $5C
Dead time(2), (3), (4)	$0036	R/W	1	Specifies the dead time used by the PWM generator. Dead time = Value * 125 ns. This is a write-once parameter.	$00–$FF
Base frequency(3)	$1000	W	1	Specifies the motor frequency at which full voltage is applied	60 Hz — $60 50 Hz — $61
Acceleration(3)	$0060	R/W	2	Acceleration in Hz/sec (7.9 format)(8)	$0000–$7FFF
Commanded motor frequency(3)	$0062	R/W	2	Commanded frequency in Hz. (8.8 format)(9)	$0000–$7FFF
Actual frequency	$0085	R	2	Actual frequency in Hz. (8.8 format)(9)	$0000–$7FFF
Status(7)	$00C8	R	1	Status byte	$00–$FF
Voltage boost	$006C	R/W	1	0 Hz voltage. %Voltage boost = Value/$FF	$00–$FF
Modulation index	$0091	R	1	Voltage level (motor waveform amplitude percent assuming no bus ripple compensation) Modulation index = value/$FF	$00–$FF

Table 6. User Interface Variables for Use with PC Master Software (Continued)

Name	Address	Read/ Write	Size (Bytes)	Description	Valid Data
Maximum voltage	$0075	R/W	1	Maximum allowable modulation index value %Maximum voltage = value/$FF	$00–$FF
V_{Bus} voltage(5), (10)	$0079	R	2	DC bus voltage reading	$000–$3FF
Fault timeout	$006A	R/W	2	Specifies the delay time after a fault condition before re-enabling the motor. Fault timeout = value * 0.262 sec	$0000–$FFFF
Fault timer	$006D	R	2	Real-time display of the fault timer Elapsed fault time = value * 0.262 sec	$0000–$FFFF
V_{Bus} decel value(10)	$00C9	R/W	2	V_{Bus} readings above this value result in reduced deceleration.	$0000–$03FF
V_{Bus} RBRAKE value(10)	$0064	R/W	2	V_{Bus} readings above this value result in the RBRAKE pin being asserted.	$0000–$03FF
V_{Bus} brownout value(10)	$0066	R/W	2	V_{Bus} readings below this value result in an under voltage fault.	$0000–$03FF
V_{Bus} over voltage value(10)	$0068	R/W	2	V_{Bus} readings above this value result in an over voltage fault.	$0000–$03FF
Speed in ADC value(5)	$0095	R	2	Left justified 10-bit ADC reading of the SPEED input pin.	$0000–$FFC0
Setup(7)	$00AE	R	1	Bit field indicating which setup parameters have been initialized before motion is permitted	$E0–$FF
Switch in(7)	$0001	R	1	Bit field indicating the current state of the start/stop and forward/reverse switches	$00–$FF
Reset status(6), (7)	$FE01	R	1	Indicates cause of the last reset	$00–$FF
Version	$EE00	R	4	MC3PHAC version	ASCII field

1. The commanded PWM frequency cannot be written until the PWM outputs exit the high-impedance state. The default PWM frequency is 15.873 kHz.
2. The PWM output pins remain in a high-impedance state until this parameter is specified.
3. This parameter must be specified before motor motion can be initiated by the MC3PHAC.
4. This is a write-once parameter. The first write to this address will execute normally. Further attempts at writing this parameter will result in an illegal operation response from the MC3PHAC.
5. The value of this parameter is not valid until the PWM outputs exit the high-impedance state.
6. The data in this field is only valid for one read. Further reads will return a value of $00.
7. See register bit descriptions following this table.
8. Acceleration is an unsigned value with the upper seven bits range of $00 to $7F = acceleration value of 0 to 127 Hertz/second. The lower nine bits constitute the fractional portion of the acceleration parameter. Its range is $000 to $1FF which equals 0 to ~1. Therefore, the range of acceleration is 0 to 127.99 Hertz/second.
9. Commanded motor frequency and actual frequency are signed values with the upper byte range of $00 to $7F = frequency of 0 to 127 Hz. The lower byte is the fractional portion of the frequency. Its range is $00 to $FF which equals 0 to ~1.
10. V_{Bus} is the voltage value applied to the DC_BUS analog input pin. The analog-to-digital converter is a 10-bit converter with a 5 volt full scale input. The value is equal to the voltage applied to the DC_BUS input pin/V_{REF} * $03FF.

Each bit variable listed in Table 6 is defined in Figure 14, Figure 15, Figure 16, and Figure 17.

Address: $00C8

	7	6	5	4	3	2	1	0
R		SPEED CHANGING	FORWARD MOTION	MOTOR ENERGIZED	RESISTIVE BRAKE	EXTERNAL FAULT TRIP	OVER VOLTAGE TRIP	UNDER VOLTAGE TRIP
W								
Reset	U	0	1	0	0	U	0	0

= Unimplemented or Reserved U = Unaffected

Figure 14. Status Register

Table 7. Status Register Field Descriptions

Field	Description
6 SPEED CHANGING	**SPEED CHANGING Bit** — This read-only bit indicates if the motor is at a steady speed or if it is accelerating or declerating. 0 Motor is at a steady speed. 1 Motor is accelerating or decelerating.
5 FORWARD MOTION	**FORWARD MOTION Bit** — This read-only bit indicates the direction of the motor. It also indicates if the motor is stopped. 0 Motor is rotating in the reverse direction. 1 Motor is rotating in the forward direction. If this bit is a logic 1 and the actual frequency (location $0085 and $0086) is 0, the motor is stopped.
4 MOTOR ENERGIZED	**MOTOR ENERGIZED Bit** — This read-only bit indicates PWM output activity 0 The PWM outputs are inactive or the bottom PWM outputs are in the pre-charge cycle. 1 All PWM outputs are active.
3 RESISTIVE BRAKE	**RESISTIVE BREAK Bit** — This read-only bit indicates the state of the RBRAKE output pin 0 The RBRAKE output pin is inactive and no braking is in progress. 1 The RBRAKE output pin is active. Braking is in progress.
2 EXTERNAL FAULT TRIP	**EXTERNAL FAULT TRIP Bit** — This read-only bit indicates a FAULT has occurred resulting from a logic 1 applied to the FAULTIN pin. 0 A logic 0 is applied to the FAULTIN pin and no FAULT timeout is in progress. 1 A logic 1 was applied to the FAULTIN pin and a FAULT timeout is still in progress.
1 OVER VOLTAGE TRIP	**OVER-VOLTAGE TRIP Bit** — This read-only bit indicates if the voltage at the DC_BUS pin exceeds the preset value of V_{Bus} over voltage located at address $0068 and $0069. 0 The voltage applied to the DC_BUS pin is less than the preset value of V_{Bus} over voltage and a FAULT timeout is not in progress. 1 The voltage applied to the DC_BUS pin has exceeded the preset value of V_{Bus} over voltage and a FAULT timeout is still in progress.
0 UNDER VOLTAGE TRIP	**UNDER-VOLTAGE Bit** — This read-only bit indicates if the voltage at the DC_BUS pin is less than the present value of V_{Bus} brownout located at address $0066 and $0067. 0 The voltage applied to the DC-BUS pin is greater than the preset value of V_{Bus} under voltage and a FAULT timeout is not in progress. 1 The voltage applied to the DC_BUS pin is less than the present value of V_{Bus} under voltage and a FAULT timeout is still in progress.

Address: $00AE

	7	6	5	4	3	2	1	0
R				BASE FREQUENCY SET	SPEED SET	ACCELERATION SET	POLARITY SET	DEAD TIME SET
W								
Reset	1	1	1	0	0	0	0	0

= Unimplemented or Reserved

Figure 15. Setup Register

Table 8. Setup Register Field Descriptions

Field	Description
4 BASE FREQUENCY SET	**BASE FREQUENCY SET Bit** — This read-only bit indicates if the base frequency parameter has been set. 0 Base frequency parameter has not been set. 1 Base frequency parameter has been set.
3 SPEED SET	**SPEED SET Bit** — This read-only bit indicates if the speed parameter has been set. 0 Speed parameter has not been set. 1 Speed parameter has been set.
2 ACCELERA-TION SET	**ACCELERATION SET Bit** — This read-only bit indicates if the acceleration rate parameter has been set. 0 Acceleration rate parameter has not been set. 1 Acceleration rate parameter has been set.
1 POLARITY SET	**POLARITY SET Bit** — This read-only bit indicates if the PWM polarity parameters has been set. 0 PWM polarity parameters has not been set. 1 PWM polarity parameters has been set.
0 DEAD TIME SET	**DEAD TIME SET Bit** — This read-only bit indicates if the dead time parameter has been set. 0 Dead time parameter has not been set. 1 Dead time parameter has been set.

Address: $0001

	7	6	5	4	3	2	1	0
R		$\overline{\text{START}}$/ STOP	$\overline{\text{FWD}}$/ REVERSE		FAULT OUT	RESISTOR BRAKE		
W								
Reset	U	U	U	U	U	0	U	U

= Unimplemented or Reserved U = Unaffected

Figure 16. Switch In Register

Table 9. Switch In Register Field Descriptions

Field	Description
6 $\overline{\text{START}}$/ STOP	**$\overline{\text{START}}$/STOP Bit** — This read-only bit indicates the state of the $\overline{\text{START}}$ input pin. 0 The $\overline{\text{START}}$ input pin is at a logic 0. 1 The $\overline{\text{START}}$ input pin is at a logic 1.
5 $\overline{\text{FWD}}$/ REVERSE	**$\overline{\text{FWD}}$/REVERSE Bit** — This read-only bit indicates the state of the $\overline{\text{FWD}}$ input pin. 0 The $\overline{\text{FWD}}$ input pin is at a logic 0 1 The $\overline{\text{FWD}}$ input pin is at a logic 1
3 FAULT OUT	**FAULT OUT Bit** — This read-only bit indicates the state of the DT_FAULTOUT output pin. 0 The DT_FAULTOUT output pin is indicating a fault condition. 1 The DT_FAULTOUT output pin is indicating no fault condition.
2 RESISTOR BRAKE	**RESISTIVE BRAKE Bit** — This read-only bit indicates the state of resistive brake pin (RBRAKE). 0 The RBRAKE output pin in inactive and no braking is in progress. 1 The RBRAKE output pin in active. Braking is in progress.

Address: $FE01

	7	6	5	4	3	2	1	0
R	POWER UP	RESET PIN	MC3PHAC FUNCTIONAL FAULT	MC3PHAC FUNCTIONAL FAULT	PC MASTER SOFTWARE RESET COMMAND		LOW V_{DD} VOLTAGE	
W								
Reset	1	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 17. Reset Status Register

Table 10. Reset Status Register Field Descriptions

Field	Description
7 POWER UP	**POWER UP Bit** — This read-only bit indicates the last system reset was caused by the power-up reset detection circuit. 0 Power-up reset was not the source of the reset or a read of the reset status register after the first read. 1 The last reset was caused by an initial power-up of the MC3PHAC.
6 RESET PIN	**RESET PIN Bit** — This read-only bit indicates the last system reset was caused from the $\overline{\text{RESET}}$ input pin. 0 The $\overline{\text{RESET}}$ pin was not the source of the reset or a read of the reset status register after the first read. 1 Last reset was caused by an external reset applied to the $\overline{\text{RESET}}$ input pin.
5–4 MC3PHAC FUNCTIONAL FAULT BITS	**MC3PHAC FUNCTIONAL FAULT Bits** — This read-only bit indicates if the last system reset was the result of an internal system error. 0 The FUNCTIONAL FAULT was not the source of the reset or a read of the reset status register after the first read. 1 MC3PHAC internal system error
PC MASTER SOFTWARE RESET COMMAND	**PC MASTER SOFTWARE RESET COMMAND Bit** — This read-only bit indicates the last system reset was the result of a PC master software reset command. 0 The PC master software RESET COMMAND was not the source of the reset or a read of the reset status register after the first read. 1 The MC3PHAC was reset by the PC master software command reset as the result of a write of $30 to location $1000
1 LOW V_{DD} VOLTAGE	**LOW V_{DD} VOLTAGE Bit** — This read-only bit indicates if the last reset was the result of low V_{DD} applied to the MC3PHAC. 0 The LOW V_{DD} was not the source of the reset or a read of the reset status register after the first read. 1 The last reset was caused by the low power supply detection circuit.

Command State Machine

When using the PC master software mode of operation, the command state machine governs behavior of the device depending upon its current state, system parameters, any new commands received via the communications link, and the prevailing conditions of the system. The command state diagram is in Figure 18. It illustrates the sequence of commands which are necessary to bring the device from the reset condition to running the motor in a steady state and depicts the permissible state transitions. The device will remain within a given state unless the conditions shown for a transition are met.

Some commands only cause a temporary state change to occur. While they are being executed, the state machine will automatically return to the state which existed prior to the command being received. For example, the motor speed may be changed from within any state by using the WRITEVAR16 command to write to the "Speed In" variable. This will cause the "Set Speed" state to be momentarily entered, the "Speed In" variable will be updated and then the original state will be re-entered. This allows the motor speed, acceleration or base frequency to be modified whether the motor is already accelerating, decelerating, or in a steady state.

Each state is described here in more detail.

- **Reset** — This state is entered when a device power-on reset (POR), pin reset, loss of crystal, internally detected error, or reset command occurs from within any state. In this state, the device is initialized and the PWM outputs are configured to high impedance. This state is then automatically exited.
- **PWMHighZ** — This state is entered from the reset state. This state is also re-entered after one and only one of the PWM dead-time or polarity parameters have been initialized. In this state the PWM outputs are configured to a high-impedance state as the device waits for both the PWM dead time and polarity to be initialized.
- **SetDeadTime** (write once) — This state is entered from the PWMHighZ state the first time that a write to the PWM dead-time variable occurs. In this state, the PWM dead time is initialized and the state is then automatically exited. This state cannot be re-entered, and hence the dead time cannot be modified, unless the reset state is first re-entered.
- **SetPolarity** (write once) — This state is entered from the PWMHighZ state the first time that the PWM polarity command is received. In this state, the PWM polarity is initialized and the state is then automatically exited. This state cannot be re-entered, and hence the polarity cannot be modified, unless the reset state is first re-entered.
- **PWMOFF** — This state is entered from the PWMHighZ state if both the PWM dead time *and* polarity have been configured. In this state, the PWM is activated and all the PWM outputs are driven off for the chosen polarity. The device then waits for the PWM base frequency, motor speed, and acceleration to be initialized.
- **PWM0RPM** — This state is entered from the PWMOFF state when the PWM base frequency, motor speed, and acceleration have been initialized. This state can also be entered from the FwdDecel or RevDecel states if a CmdStop command has been received, and the actual motor speed has decelerated to 0 r.p.m. In this state, the PWM pins are driven to the off state for the chosen polarity. The only exit of this state is to the PWMPump state, which occurs when a CmdFwd or CmdRev command is received.

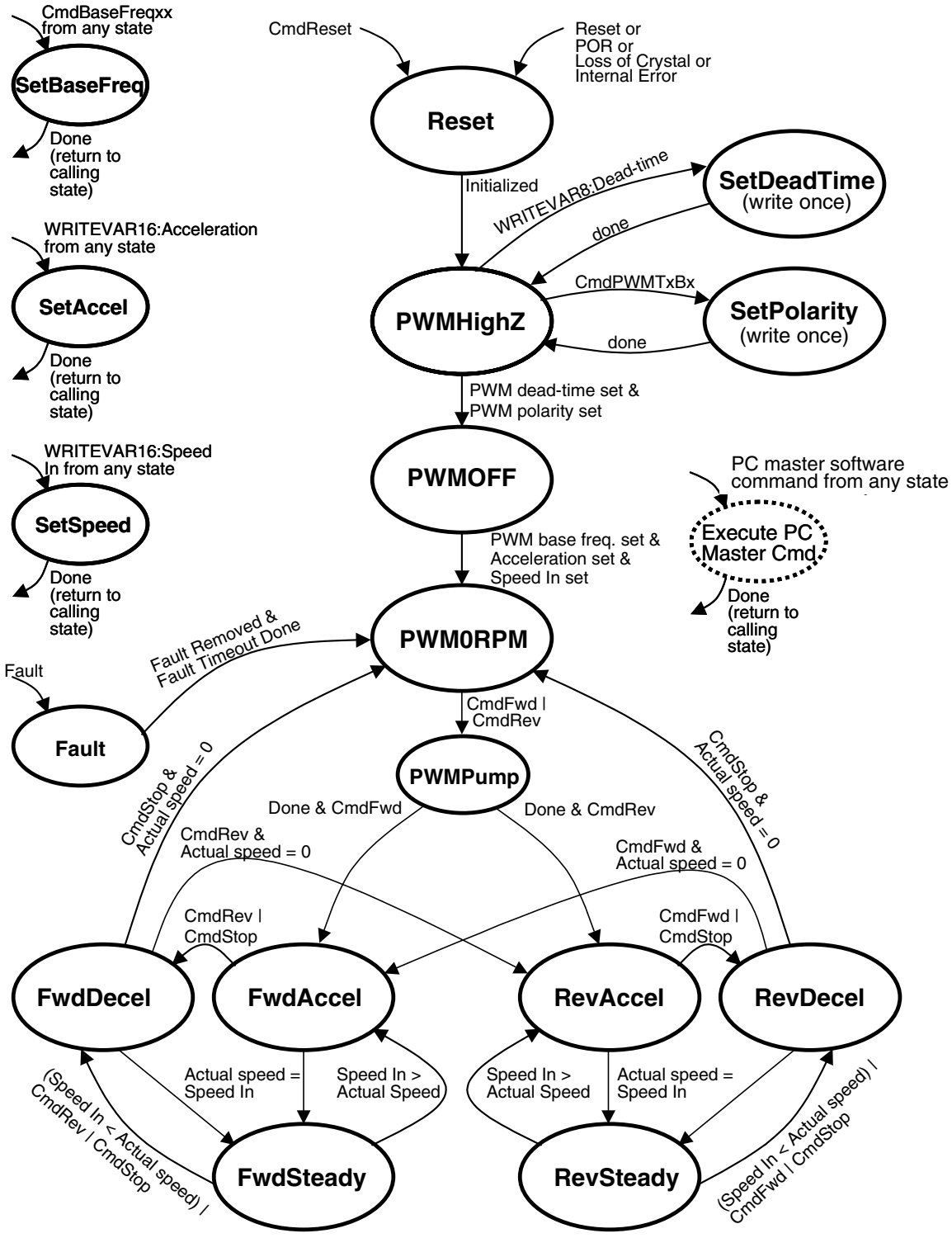


Figure 18. PC Host Software Command State Diagram

- **PWMPump** — This state is entered from the PWM0RPM state when a CmdFwd or CmdRev command is received. In this state the top PWM outputs are driven off while the bottom PWM outputs are driven with a 50 percent duty cycle. This allows high side transistor gate drive circuits which require charge pumping from the lower transistors to be charged up prior to applying full PWMs to energize the motor. This state is automatically exited after the defined amount of time t_{Pump} (see Electrical Characteristics).
- **FwdAccel** — This state is entered from the PWMPump state after a CmdFwd command is received and the timeout interval from the PWMPump state is completed. This state can also be entered from the FwdSteady state if the Speed In variable is increased above the actual current speed and the RevDecel state if the actual motor speed equals 0 r.p.m. when a CmdFwd command has been received. In this state the motor is accelerated forward according to the chosen parameters.
- **FwdSteady** — This state is entered from the FwdAccel state after the actual motor speed has reached the requested speed defined by the Speed In variable. In this state, the motor is held at a constant forward speed.
- **FwdDecel** — This state is entered from the FwdAccel or FwdSteady states whenever a CmdStop or CmdRev command is received. This state can also be entered from the FwdSteady state if the Speed In variable is decreased below the actual current speed. In this state, the motor is decelerated forward according to the chosen parameters.
- **RevAccel** — This state is entered from the PWMPump state. After a CmdRev command is received and the timeout interval from the PWMPump state is completed. This state can also be entered from the RevSteady state if the Speed In variable is increased above the actual current speed and the FwdDecel state if the actual motor speed equals 0 r.p.m. when a CmdRev command has been received. In this state, the motor is accelerated in reverse according to the chosen parameters.
- **RevSteady** — This state is entered from the RevAccel state after the actual motor speed has reached the requested speed defined by the Speed In variable. In this state, the motor is held at a constant reverse speed.
- **RevDecel** — This state is entered from the RevAccel or RevSteady states whenever a CmdStop or CmdFwd command is received. This state can also be entered from the RevSteady state if the Speed In variable is decreased below the actual current speed. In this state, the motor is decelerated in reverse according to the chosen parameters.
- **SetBaseFreq** — This state is entered from any state whenever a CmdBaseFreqxx command is received. In this state, the motor frequency at which full voltage is applied is configured and the state is then automatically exited and the original state is re-entered.
- **SetAccel** — This state is entered from any state whenever a write to the Acceleration variable occurs. In this state, the motor acceleration is configured and the state is then automatically exited and the original state is re-entered.
- **SetSpeed** — This state is entered from any state whenever a write to the Speed In variable occurs. In this state, the requested motor speed is configured and the state is then automatically exited and the original state is re-entered.
- **Fault** — This state is entered from any state whenever a fault condition occurs (see Fault Protection on page 13). In this state, the PWM outputs are driven off (unless the fault state was entered from the PWMHighZ state, in which case, the PWM outputs remain in the High Z state). When the problem causing the fault condition is removed, a timer is started which will wait a specified amount of time (which is user programmable) before exiting this state. Under normal

operating conditions, this timeout will cause the Fault state to be automatically exited to the PWM0RPM state, where motion will once again be initiated if a CmdFwd or CmdRev has been received. The exceptions to this rule are the cases when the Fault state was entered from the PWMHighZ or PWMOFF states, in which case, exiting from the Fault state will return back to these states.

Optoisolated RS232 Interface Application Example

Some motor control systems have the control electronics operating at the same potential as the high voltage bus. Connecting a PC to that system could present safety issues, due to the high voltage potential between the motor control system and the PC. Figure 19 is an example of a simple circuit that can be used with the MC3PHAC to isolate the serial port of the PC from the motor control system.

The circuit in Figure 19 is the schematic of a half-duplex optoisolated RS232 interface. This isolated terminal interface provides a margin of safety between the motor control system and a personal computer. The EIA RS232 specification states the signal levels can range from ±3 to ±25 volts. A Mark is defined by the EIA RS232 specification as a signal that ranges from –3 to –25 volts. A Space is defined as a signal that ranges from +3 to +25 volts. Therefore, to meet the RS232 specification, signals to and from a terminal must transition through 0 volts as it changes from a Mark to a Space. Breaking the circuit down into an input and output section simplifies the explanation of the circuit.

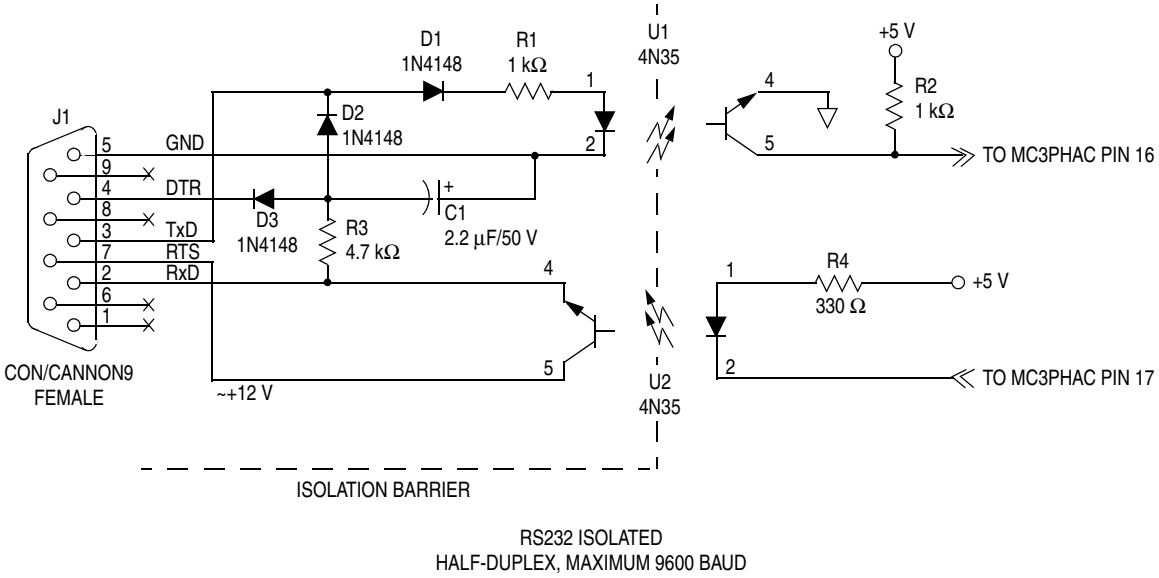


Figure 19. Optoisolated RS232 Circuit

To send data from a PC to the MC3PHAC, it is necessary to satisfy the serial input of the MC3PHAC. In the idle condition, the serial input of the MC3PHAC must be at a logic 1. To accomplish that, the transistor in U1 must be turned off. The idle state of the transmit data line (TxD) from the PC serial port is a Mark (–3 to –25 volts). Therefore, the diode in U1 is off and the transistor in U1 is off, yielding a logic 1 to the MC3PHAC's serial input. When the start bit is sent to the MC3PHAC from the PC's serial port, the PC's TxD transitions from a Mark to a Space (+3 to +25 volts), thus forward biasing the diode in U1. Forward biasing the diode in D1 turns on the transistor in U1, providing a logic 0 to the serial input of the MC3PHAC. Simply stated, the input half of the circuit provides input isolation, signal inversion, and level

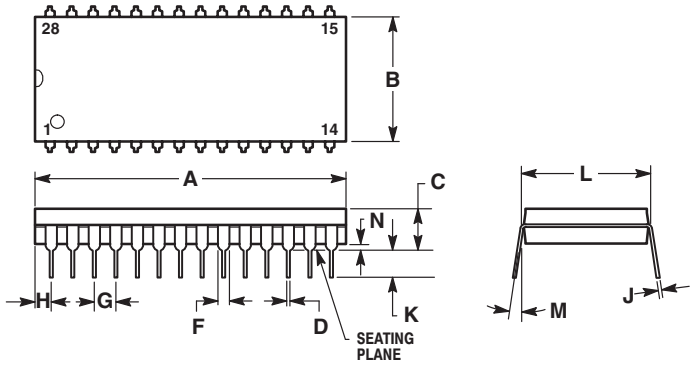
shifting from the PC to the MC3PHAC's serial port. An RS-232 line receiver, such as an MC1489, serves the same purpose without the optoisolation function.

To send data from the MC3PHAC to the PC's serial port input, it is necessary to satisfy the PC's receive data (RxD) input requirements. In an idle condition, the RxD input to the PC must be at Mark (–3 to –25 volts). The data terminal ready output (DTR) on the PC outputs a Mark when the port is initialized. The request to send (RTS) output is set to a Space (+3 to +25 volts) when the PC's serial port is initialized. Because the interface is half-duplex, the PC's TxD output is also at a Mark, as it is idle. The idle state of the MC3PHAC's serial port output is a logic 1. The logic 1 out of the MC3PHAC's serial port output port forces the diode in U2 to be turned off. With the diode in U2 turned off, the transistor in U2 is also turned off. The junction of D2 and D3 are at a Mark (–3 to –25 volts). With the transistor in U2 turned off, the input is pulled to a Mark through current limiting resistor R3, satisfying the PC's serial input in an idle condition. When a start bit is sent from the MC3PHAC's serial port, it transitions to a logic 0. That logic 0 turns on the diode in U2, thus turning on the transistor in U2. The conducting transistor in U2 passes the voltage output from the PC's RTS output, that is now at a Space (+3 to +25 volts), to the PC's receive data (RxD) input. Capacitor C1 is a bypass capacitor used to stiffen the Mark signal. The output half of the circuit provides output isolation, signal inversion, and level shifting from the MC3PHAC's serial output port to the PC's serial port. An RS-232 line driver, such as a MC1488, serves the same purpose without the optoisolation function.

Mechanical Data

This subsection provides case outline drawings for:

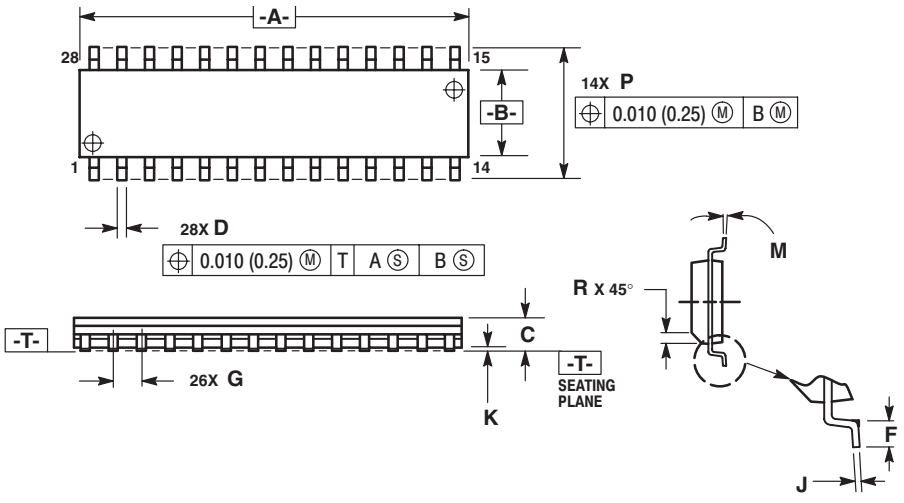
- Plastic 28-pin DIP, Figure 20
- Plastic 28-pin SOIC, Figure 21
- Plastic 32-pin QFP, Figure 22



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

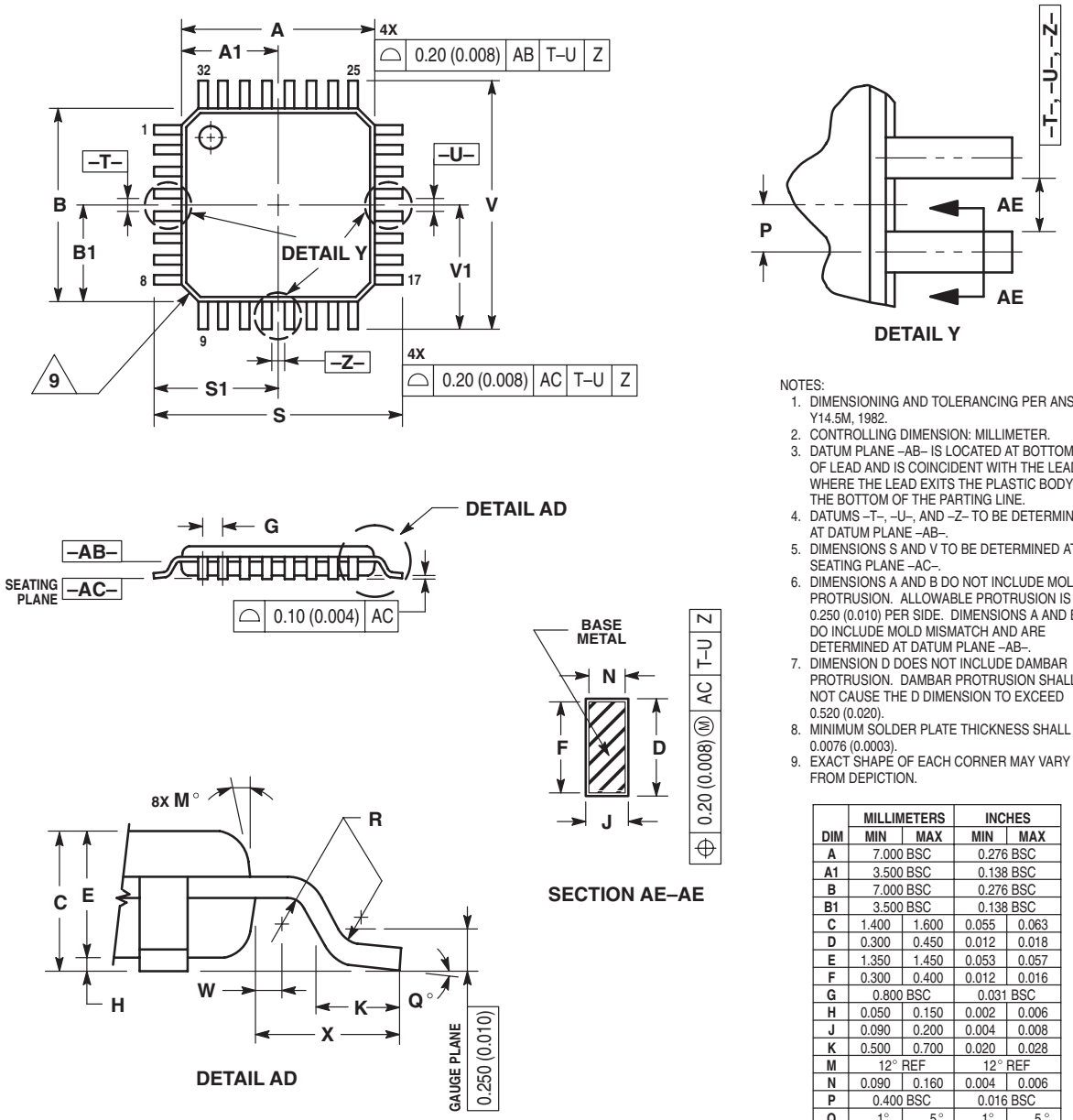
Figure 20. Plastic 28-Pin DIP (Case 710)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

Figure 21. Plastic 28-Pin SOIC (Case 751F)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

Figure 22. Plastic 32-Pin QFP (Case 873A)

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