

DESIGN
FEARLESSLY



FPGA + ARM® Cortex™-M3 + Programmable Analog



Microsemi
SoC Products Group

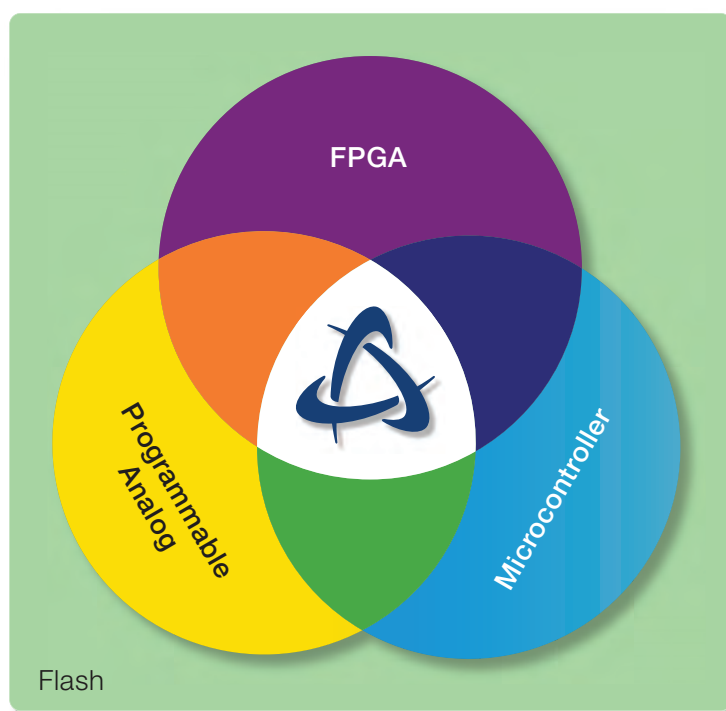
Innovative Intelligent Integration

SmartFusion intelligent mixed signal FPGAs are the only devices that integrate an FPGA, an ARM Cortex-M3 processor and programmable analog, offering full customization, IP protection and ease-of-use. Based on Microsemi's proprietary flash process, SmartFusion devices are ideal for hardware and embedded designers who need a true system-on-chip (SoC) that gives more flexibility than traditional fixed-function microcontrollers, without the excessive cost of soft processor cores on traditional FPGAs.

Hard 32-Bit ARM
Cortex-M3 Processor

Proven ProASIC®3
FPGA Fabric

Full-Featured
Programmable Analog



KEY BENEFITS OF SMARTFUSION FPGAS

Full Design Customization

- Create a product with exactly the features you need
- Innovate and differentiate for a competitive edge
- Incorporate last-minute changes with an on-chip FPGA
- In-application programming (IAP) capability for field upgrades
- Experiment with hardware acceleration for select algorithms in FPGA fabric

Intellectual Property (IP) Protection

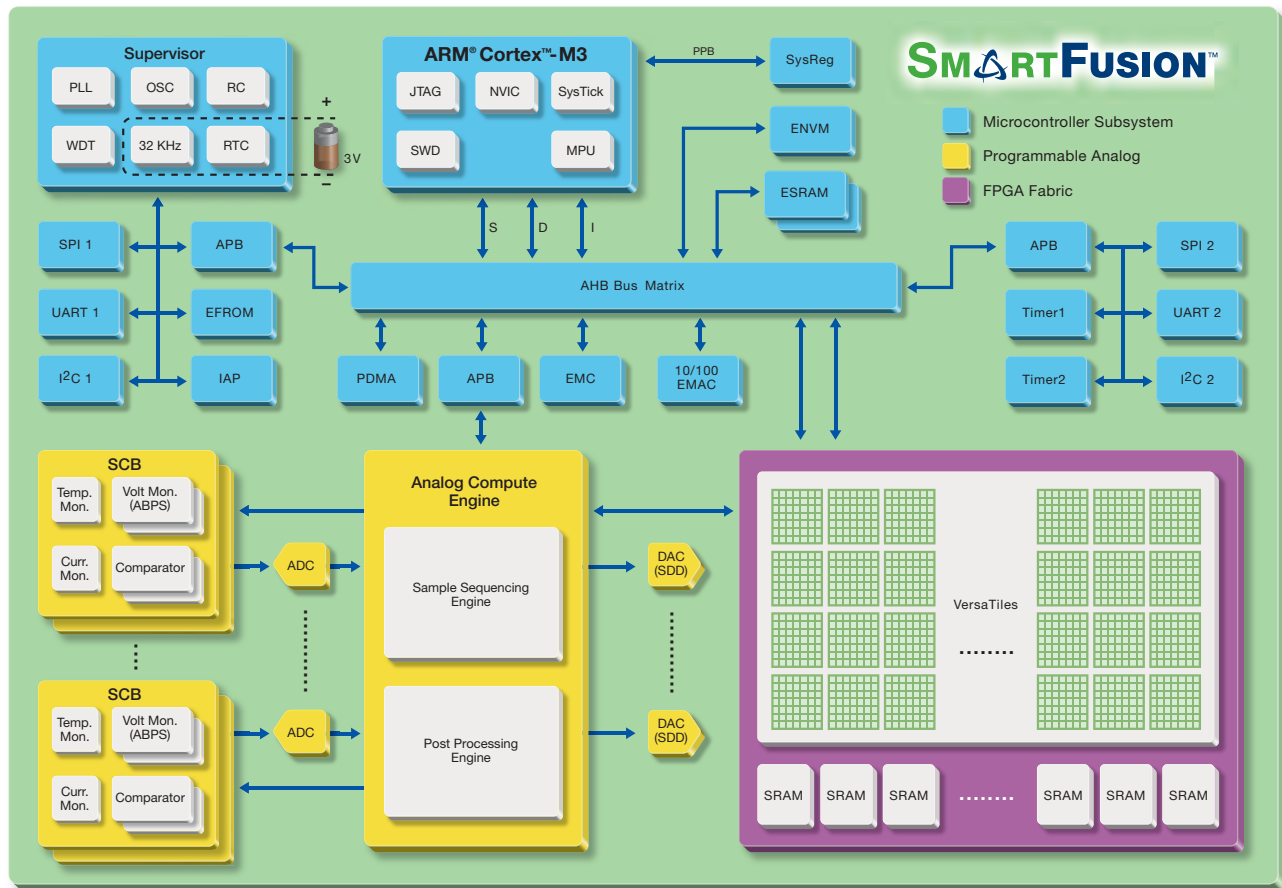
- Interface between microcontroller and FPGA not exposed at board level
- No bitstream exposed at power-up
- Encrypted in-system programming (ISP) with 128-bit AES via JTAG
- FlashLock® controls access to the security setting on the device
- Protection against overbuilding with customer programmable device key

Ease-of-Use Increases Productivity

- A single platform for your entire line of products
- Integrated design environment for both FPGA and embedded designers
- Simple GUI-based configuration of complex programmable analog
- Industry leading compile and debug from Keil, IAR and GNU
- Real-time operating system (RTOS) and middleware components from Micrium, RoweBots, Emcraft and more

SmartFusion Architecture

Along with microcontroller (MCU), FPGA and analog, SmartFusion intelligent mixed signal FPGAs integrate substantial flash and SRAM memory and comprehensive clock generation and management circuitry. SmartFusion architecture enables data storage and execution of code from a single monolithic device. In addition, in-application programming (IAP) enables real-time updates and reprogramming of the complete chip. Design compromises that were inevitable with traditional fixed-function microcontrollers and FPGAs are eliminated when designing with SmartFusion devices.



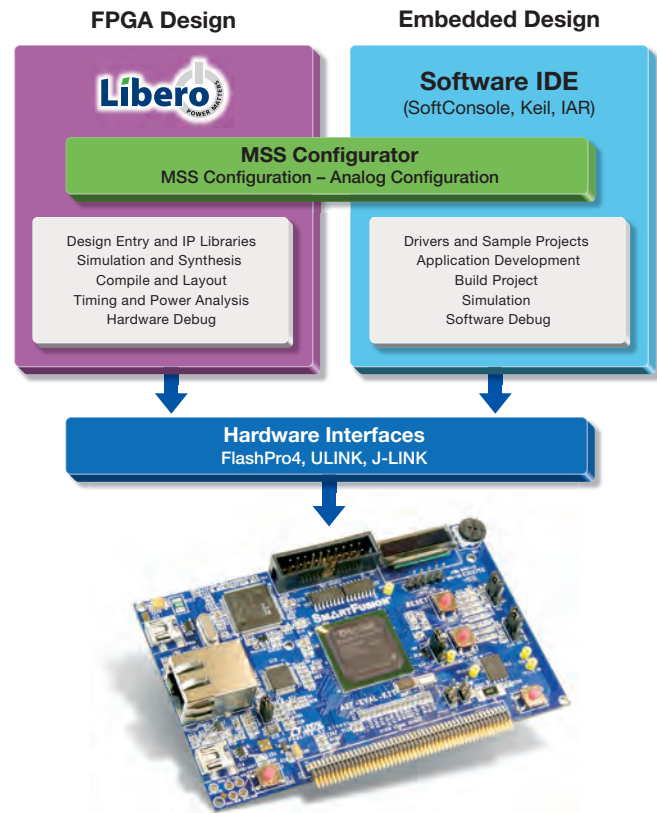
NO-COMPROMISE MICROCONTROLLER SUBSYSTEM (MSS)	PROGRAMMABLE ANALOG	NO COMPROMISE FPGA FABRIC
- Hardware industry-standard 100 MHz, 32-bit ARM Cortex-M3 CPU - Multi-layer AHB communication matrix with up to 16 Gbps throughput 10/100 Ethernet MAC with RMII interface - Two of each: SPI, I2C, UART, 32-bit timers - Up to 512 KB flash and 64 KB of SRAM - External memory controller (EMC) 8-channel DMA controller - Up to 41 MSS I/Os with Schmitt trigger inputs — 25 I/Os can be used as FPGA I/Os	- High-performance analog signal conditioning blocks (SCB) with voltage, current and temperature monitors - Analog compute engine (ACE) offloads CPU from analog initialization and processing of analog-to-digital conversion (ADC), digital-to-analog conversion (DAC) and SCBs - Integrated ADCs and DACs with 1 percent accuracy 12-/10-/8-bit mode ADCs with 500/550/600 Ksps sampling rate - Up to ten 15 ns high-speed comparators - Up to 32 analog inputs and 3 outputs	- Based on Microsemi's proven ProASIC3 architecture 60,000 to 500,000 system gates with 350 MHz system performance - Embedded SRAMs and FIFOs — Variable aspect ratio 4,608-bit SRAM blocks — x1, x2, x4, x9 and x18 organizations — True dual-port SRAM (including x18) - Up to 128 FPGA I/Os supporting LVDS, PCI, PCI-X and LVTTTL/LVCMOS standards

Designing with SmartFusion

Designing with SmartFusion involves three different types of design: FPGA design, embedded design and analog design. These roles can be filled by three different designers, two designers or even a single designer, depending on company structure and project complexity. Microsemi has developed design tools and flows to meet the needs of these three types of designers so they can work together smoothly on a single project.

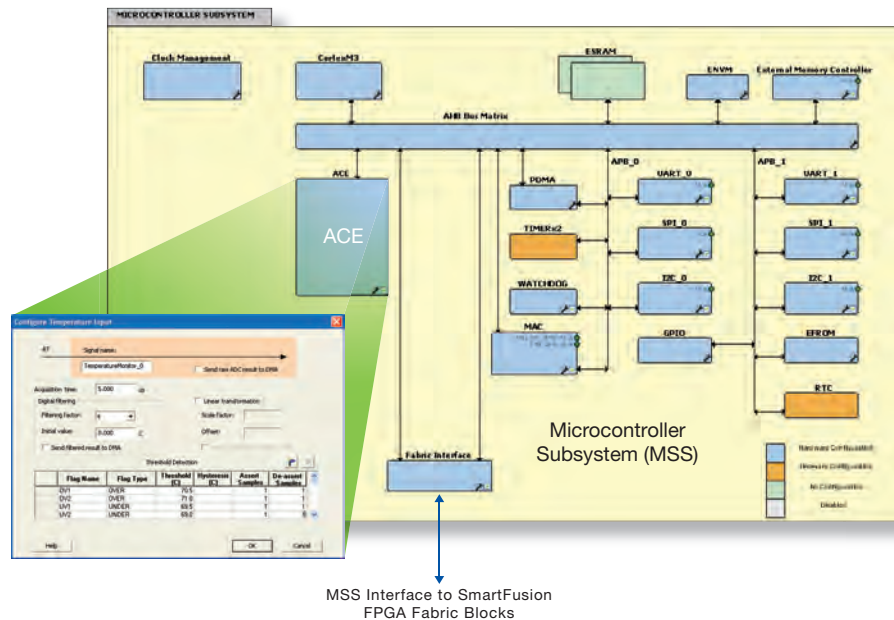
- **FPGA Design**—Libero® Integrated Design Environment (IDE) is Microsemi's comprehensive software toolset for designing with all Microsemi FPGAs. Libero IDE includes industry-leading synthesis, simulation and debug tools from Synopsys® and Mentor Graphics®, as well as innovative timing and power optimization and analysis.
- **Embedded Design**—Microsemi offers FREE SoftConsole Eclipse-based IDE, which includes the GNU C/C++ compiler and GDB debugger. Microsemi also offers evaluation versions of software from Keil and IAR, with full versions available from respective suppliers.
- **Analog Design**—The MSS configurator provides graphical configuration for current, voltage and temperature monitors, sample sequencing setup and post-processing configuration, as well as DAC output.

The MSS configurator creates a bridge between the FPGA and embedded designers so device configuration can be easily shared between multiple developers.



MSS CONFIGURATOR

- Configure the MSS peripherals and I/Os during embedded system design.
- Create or view hardware configuration in FPGA design flow.
- Create or import hardware configuration in embedded design flow.
- Automatically generate drivers for peripherals or soft IP.
- Configure programmable analog components.
- Connect FPGA fabric designs and IP to MSS.

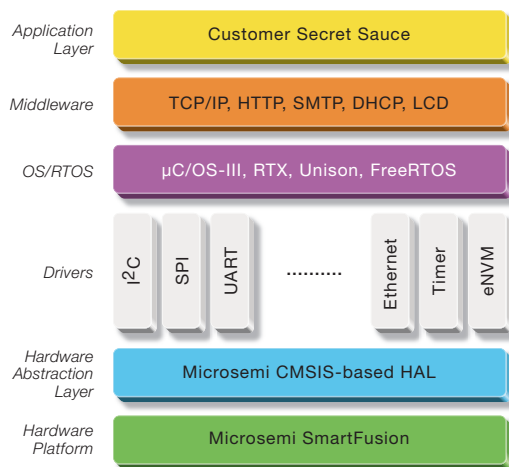


SmartFusion Ecosystem

The Microsemi SoC Products Group (formerly Actel) has a long history of supplying comprehensive FPGA development tools and recognizes the benefit of partnering with industry leaders to deliver the optimum usability and productivity to customers. Taking the same approach with processor development, Microsemi has partnered with key industry leaders in the microcontroller space to provide the robust SmartFusion ecosystem.

Microsemi is partnering with Keil and IAR to provide Software IDE support to SmartFusion system designers. The result is a robust solution that can be easily adopted by existing embedded developers. The learning path is straightforward for FPGA designers.

Because an ARM processor was chosen for SmartFusion FPGAs, Microsemi's customers can benefit from the extensive ARM ecosystem. By building on Microsemi supplied HAL and drivers, third party vendors can easily port RTOS and middleware for the SmartFusion devices.



The diagram above shows the SmartFusion stack with examples of drivers, RTOS and middleware from Microsemi and partners. By leveraging the SmartFusion stack, designers can decide at which level to add their own customization to their design, thus speeding time to market and reducing overhead in the design.

OPERATING SYSTEMS

Micrium

Offers their μC/OS-III™ and μC/OS-II™ to support SmartFusion devices and includes a TCP/IP stack.

Keil

Includes the RTX Kernel in their standard MDK software and sources can also be purchased in an additional module along with TCP/IP.

RoweBots

Delivers their ultra tiny Linux™ - compatible RTOS Unison, consisting of a set of modular software components.

Emcraft

Developed the first uCLinux™ offering for SmartFusion, along with their own embedded development platform.

FreeRTOS

Microsemi has ported the FreeRTOS Kernel to SmartFusion and demonstrates this as a webserver reference design, included with both the SmartFusion evaluation and development kits.

Details of these and other solutions can be found on the SmartFusion Ecosystem pages.

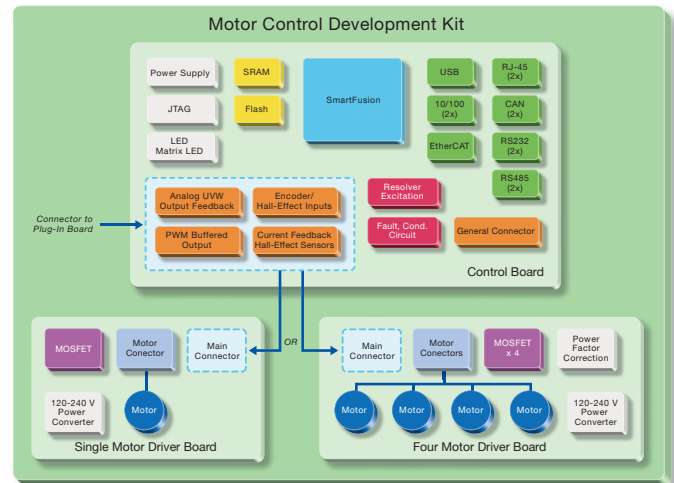
			
Software IDE	SoftConsole	Keil MDK	IAR Embedded Workbench®
Free Versions from Microsemi	Free with Libero IDE	32 K Code Limited	32 K Code Limited
Available from Vendor	N/A	Full version	Full Version
Compiler	GNU GCC	RealView® C/C++	IAR ARM Compiler
Debugger	GDB Debug	μVision Debugger	C-SPY® Debugger
Instruction Set Simulator	No	μVision Simulator	Yes
Debug Hardware	FlashPro4	ULINK®2 or ULINK-ME	J-LINK™ or J-LINK Lite

Motor Control

SmartFusion devices are uniquely suited for active control of permanent magnet motors, servo motors, AC induction motors and stepper motors. A single SmartFusion FPGA can manage control of multiple electric motors in real-time, including start and stop, rotational direction, speed and torque, protection against motor overloads or faults and use of closed-loop performance algorithms.

The ARM Cortex-M3 based MSS manages high-level tasks such as communication and interface; the on-chip analog resources convert voltage and current readings to digital format for computation; the FPGA fabric provides flexibility in custom logic implementation and hardware acceleration for complex motor control algorithms. The presence of an MCU and FPGA in this integrated device enables easy partitioning of software and hardware, resulting in higher performance, lower power and efficient silicon usage.

Microsemi's SmartFusion Motor Control Development Kit enables demonstration and benchtop development of your world-class motor control products, including support for a state-of-the-art field-oriented control (FOC) algorithm. The kit includes five reference designs with source files:



- Trapezoidal using Hall effect sensor feedback
- Sinusoidal using Hall effect sensor feedback
- Sinusoidal with encoder feedback
- Sensorless trapezoidal with back-EMF feedback
- Ethernet interactive control of motors

Industrial Automation

The range of peripherals offered for the Cortex-M3 processor and the flexibility of SmartFusion FPGA fabric make the device ideal for industrial automation. The SmartFusion Development Kit supports Ethernet, EtherCAT, CAN, UART, I²C and SPI hardware, while firmware can be used for various other interface standards such as Modbus[®] and PROFIBUS for industrial networking. With the availability of programmable analog for sensing and analog outputs, SmartFusion can also be used in industrial control applications, including gateways, sensing, actuators and I/O devices. The list below describes how the various sections of the device could be used in industrial automation.

Microcontroller Subsystem

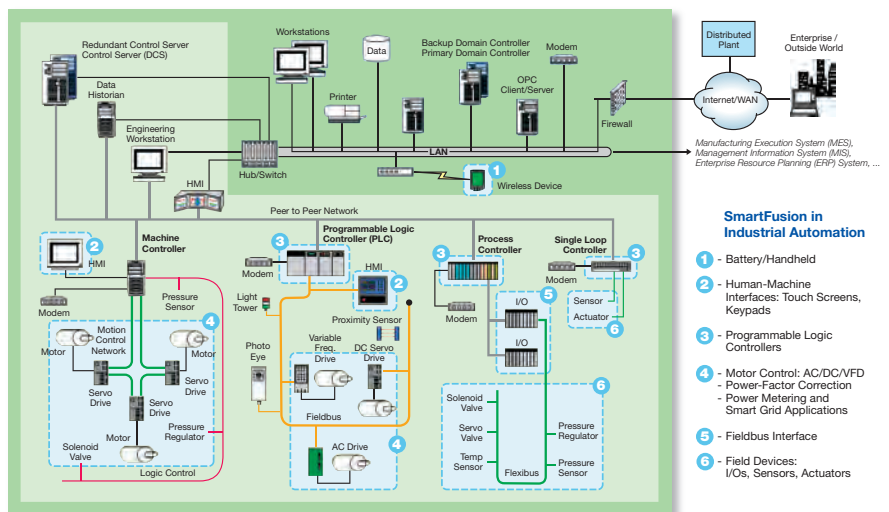
- ARM Cortex-M3 running Fieldbus protocol stack
- Ethernet MAC – standard protocols

FPGA Fabric

- Multiple RS485 capable UARTs
 - PROFIBUS, Modbus, WorldFIP, P-NET
- High speed Manchester encoding/decoding
- CAN

Analog

- ADC for sensing
- DAC for excitation



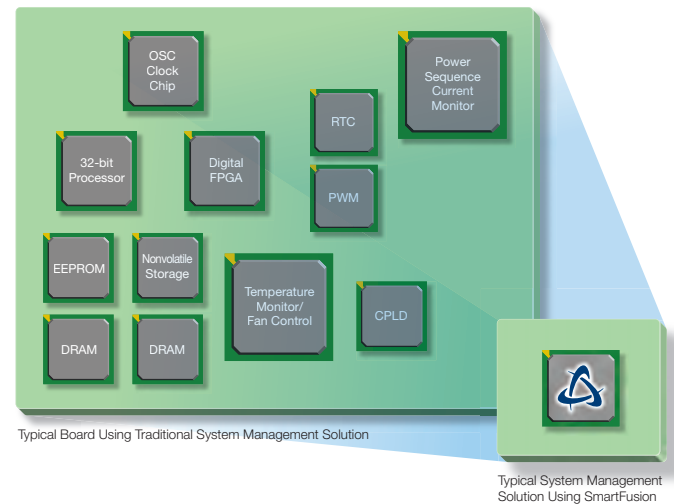
Source: NIST

System Management

System management continues to gain importance in the design of all electronic systems, since smaller process geometries drive more multi-volt devices and are more susceptible to voltage and temperature fluctuations. System management tasks focus on maximizing system uptime, identifying and communicating alert conditions and logging data and alarm conditions. This can be combined with in-system diagnostics and prognostics, not only to help debug systems that have failed, but also to identify potential failures before they arise. Thus, using a SmartFusion device as a system manager provides the designer maximum implementation flexibility.

- Use the sample sequence engine in the ACE to manage system health data collection.
- Use the post-processing engine in the ACE to manage alert condition flag generation.
- Cortex-M3 only needs to make requests to the ACE and respond to interrupts; no processing cycles needed.
- Use FPGA gates for control algorithms when needed.
- Communicate through I²C, UART, SPI or Ethernet for updates and reporting.

Leveraging the considerable processing power of the ACE leaves the Cortex-M3 and FPGA gates available for running the actual application or communicating with the outside world. This not only eliminates the need for multiple ASSP devices to perform system management, but prevents system management from being an unnecessary burden on the bill-of-materials (BOM) cost. Selecting SmartFusion devices for system management provides flexibility and reliability at the lowest total cost of ownership (TCO).

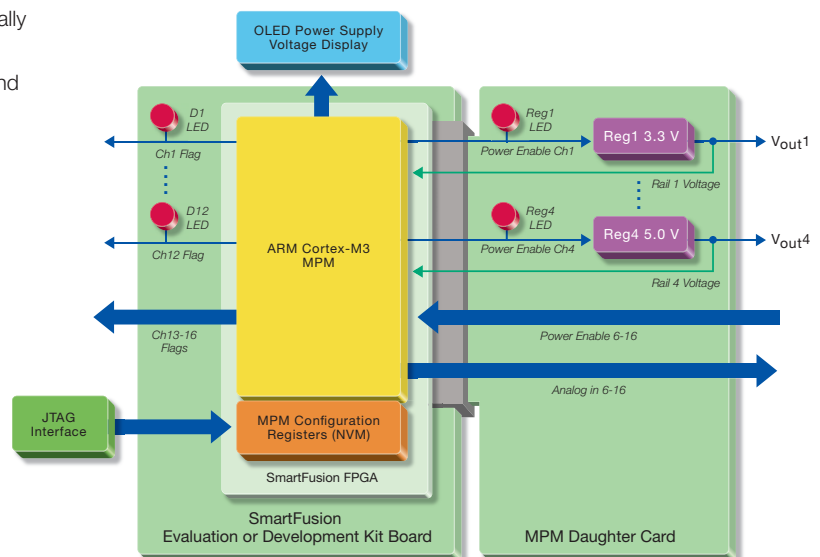


Power Management

SmartFusion Mixed Signal Power Manager (MPM) offers a graphically configurable power management solution that performs power rail monitoring, power sequencing, closed-loop trimming, power-up and power-down control and event data logging.

- Manages up to 32 power regulators
- 8 configurable PWM trimming outputs
- 32 general purpose digital outputs
- Data logging to eNVM of critical events
- I²C and JTAG configuration updates

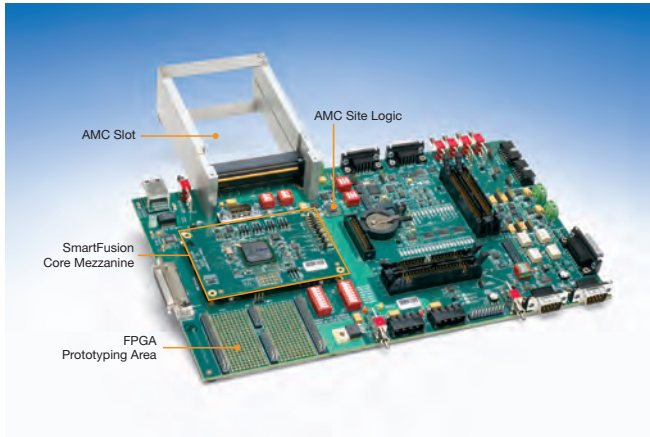
With complete PC-based GUI, source code and a fully implemented reference design available for use with the MPM Daughtercard to evaluate the full solution, the MPM reference design also enables designers to integrate intelligent configurable power management with their own Cortex-M3 firmware and FPGA design using SmartFusion devices.



Hardware Platform Management



Pigeon Point Systems, a Microsemi partner, helped refine the architecture of SmartFusion devices for hardware platform management. The following SmartFusion-based Board Management Reference (BMR) solutions for the ATCA and μ TCA board and module controller are examples of offerings from Pigeon Point Systems:



Benchtop Board for SmartFusion IPMC and Carrier IPMC

- BMR-A2F-ATCA: IPM Controllers (IPMCs) for ATCA boards
- BMR-A2F-AMCc: Carrier IPMCs for ATCA AMC carrier boards
- BMR-A2F-AMCm: Module Management Controllers for AMC modules
- BMR-A2F-MCMC: MicroTCA Carrier Management Controllers

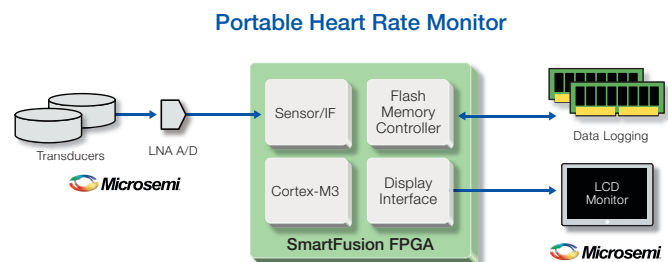
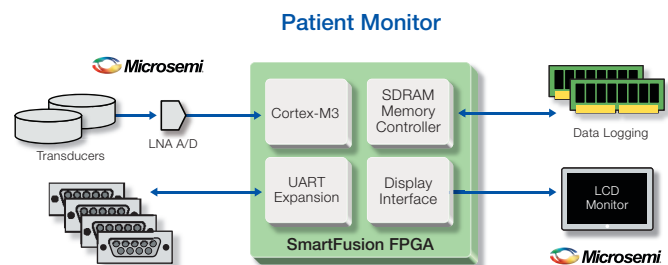
Pigeon Point Systems is the dominant supplier of hardware and firmware solutions for the mandatory hardware platform management controllers that are part of every Telecommunications Computing Architecture (xTCA) board or module. Key features of these solutions include:

- Advanced Ethernet attachment via built-in Ethernet MAC, supporting serial port access and fast firmware upgrades over LAN
- Optimizations for xTCA management via the flash FPGA fabric, with the option to integrate additional board- and module-specific functionality
- Advanced analog monitoring using SmartFusion's programmable analog
- Complete off-loading from the Cortex-M3 of xTCA-aware analog threshold processing via ACE
- Integration of flexible power management functions eliminating the use of external power devices
- Benchtop implementations for familiarization and as a known good reference during bring-up of a new xTCA board or module

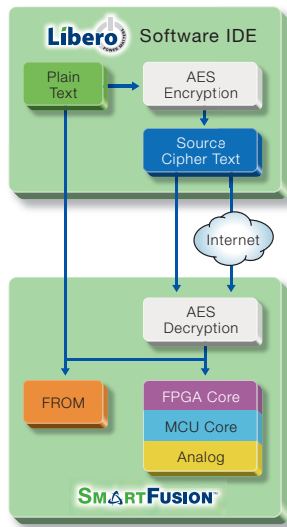
Medical Systems

The trend towards miniaturization and portability for home, clinical, and imaging medical devices demands highly reliable integrated components with product longevity and very low power consumption. Components must meet space constraints while extending battery life. SmartFusion FPGAs can integrate the functions typically served by several discrete components into a single reliable, low power, programmable chip. Data management functions, such as serial-to-parallel data conversion, level shifting, and interfaces to LCD, microprocessor, sensor and memory controllers, can be easily accomplished with SmartFusion FPGAs. System management activities are handled equally well: power supply supervision and control, voltage and temperature monitoring, positioning and angle steering. Key benefits include the following:

- Security against counterfeit and reverse engineering
- No obsolescence concerns. The lifespan of Microsemi FPGAs is measured in decades.
- Unparalleled reliability. SmartFusion FPGAs are immune to neutron-induced configuration loss from single-event errors (SEEs) and maintain system integrity without the need for mitigation techniques.



Design and Data Security



Microsemi's flash FPGAs have always been known for their design security and IP protection. SmartFusion devices bring an even higher level of security to embedded systems.

- Microcontroller and FPGA interface not exposed at board level
- No bitstream to transfer at boot-up
- FlashLock protects against tampering and reprogramming
- AES-encrypted in-system programming
- Protects against overbuilding with programmable device key

Microsemi is the first major FPGA company to address the threats caused by side-channel analysis. Side-channel attacks such as differential power analysis (DPA) can endanger the security of the design IP configured into an FPGA and the security of the end application itself.



Microsemi has obtained a license from Cryptograph Research, Inc. (CRI) for the DPA patent portfolio, consisting of more than fifty patents. Contact Microsemi sales to order devices that include a license to implement IP based on these patents.

For a more complete description of Microsemi's security solutions and partner IP blocks related to DPA and design security, refer to: www.actel.com/products/solutions/security.

Intellectual Property for SmartFusion

SmartFusion devices are composed of hard intellectual property (IP) blocks, such as an ARM Cortex-M3 processor, UART, SPI, I²C and 10/100 Ethernet interface, as well as standard peripherals, such as ADC, DAC, timers, watchdog timer and RTC. Beyond these hard cores you can select from Microsemi's IP Catalog within SmartDesign to add additional free IP to the FPGA fabric of your SmartFusion device, or choose from a wide range of partner cores. Microsemi has more than 180 intellectual property products designed and optimized to support communications, consumer, military, industrial, automotive and aerospace markets. Microsemi IP solutions streamline your designs, enable faster time-to-market and minimize design costs and risk. The table below shows some examples of the IP available. A complete list of cores is available on the Microsemi SoC Products Group website.

General Purpose		Cryptography	Communication	MIL-STD-1553B	DSP IP Core
Core16550	CoreUART	CoreAES128	CorePCIF	Core1553BRM	CoreFFT
CoreGPIO	CoreI2C	CoreDES	CoreSDR/DDR	Core1553BRT	CoreFIR
CoreTimer	CoreSPI	Core3DES	Core429	Core1553BRT-EBR	CoreDDS
CoreSDR	CorePWM	Fast SHA-256 Hash ¹	IniCAN ²	Core1553BBC	—

Notes:

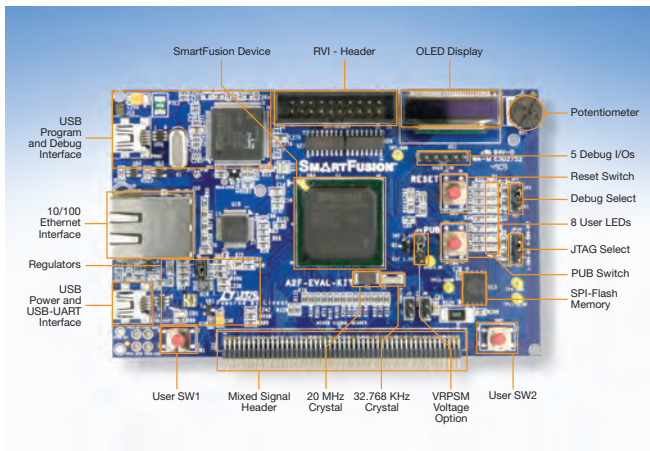
1. For more information, see the Helion Technology partner page: www.actel.com/products/partners/companioncore/helion.aspx.
2. For more information, see the Inicore partner page: www.actel.com/products/partners/companioncore/inicore.aspx.

Microsemi IP cores can be accessed through Libero IDE via the SmartDesign IP catalog. Drivers for the processor supported IP cores are available through the Firmware Catalog and are extracted automatically for SmartFusion designs through the MSS Configurator dialog.

Libero IDE Licenses	Gold (FREE)	Platinum	Platinum Evaluation	Standalone
Device Support	Up to 1,500,000 gates	All devices	All devices	All devices
Microsemi IP	Obfuscated	RTL	Obfuscated	RTL

For a complete list of Microsemi IP cores and partner CompanionCores, refer to: www.actel.com/products/ip.

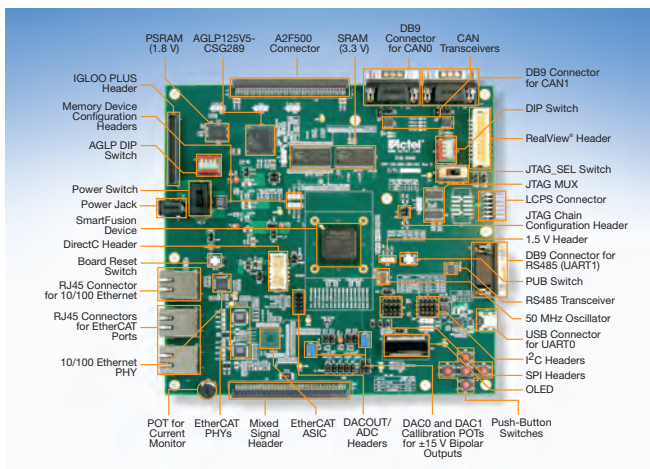
SmartFusion Evaluation Kit



- Supports SmartFusion evaluation, including ARM Cortex-M3, FPGA and programmable analog
- Free one-year Libero Integrated Design Environment (IDE) software and Gold license with SoftConsole for embedded design
- Two USB cables
- Online user's guide, tutorial and design examples
- Printed circuit board (PCB) schematics, layout files and bill-of-materials (BOM)
- Board features
 - Ethernet interface
 - USB port for power and HyperTerminal
 - USB port for programming and debug
 - J-Link header for debug
 - Mixed signal header
 - SPI flash – off-chip memory
 - Reset and 2 user switches, 8 LEDs
 - POT for voltage / current monitor
 - Temperature monitor
 - Organic light-emitting diode (OLED)

Ordering Code	Supported Device	Price
A2F-EVAL-KIT	A2F200M3F-FGG484	\$ 99

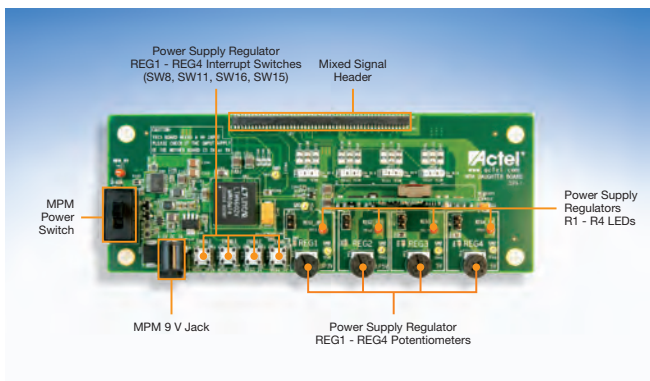
SmartFusion Development Kit



- Supports SmartFusion development, including ARM Cortex-M3, FPGA and programmable analog
- Free one-year Libero IDE software and Gold license with SoftConsole for embedded design
- 5 V power supply and international adapters
- Two USB cables
- Online user's guide, tutorial and design examples
- PCB schematics, layout files and BOM
- Board features
 - Ethernet, CAN, UART, i2C and SPI interfaces
 - USB port for HyperTerminal
 - USB port for programming and debug
 - J-Link header for debug
 - Mixed signal and A2F500 digital expansion header
 - Extensive off-chip memory
 - See the Microsemi SoC Products Group website for a full list of features

Ordering Code	Supported Device	Price
A2F500-DEV-KIT	A2F500M3G-FGG484	\$ 999

MPM Daughter Card



- Supports power management design with the SmartFusion Evaluation Kit and SmartFusion Development Kit
- MPM design example implements configurable power management in SmartFusion
- Graphical configuration dialog
- In-system reconfigurable
- 9 V power supply
- Board features
 - 4 power supply regulators
 - 4 potentiometers to control regulators
 - 4 power supply regulator interrupt switches
 - 4 power supply regulator status LEDs
 - Mixed signal header connector connects to SmartFusion board

Ordering Code	Supported Device	Price
MPM-DC-KIT	No Microsemi Device on Daughtercard	\$ 299

SmartFusion Family Product Table

SmartFusion Devices		A2F060	A2F200	A2F500
FPGA Fabric	System Gates	60,000	200,000	500,000
	Tiles (D-flip-flops)	1,536	4,608	11,520
	RAM Blocks (4,608 bits)	8	8	24
Microcontroller Subsystem (MSS)	Flash (Kbytes)	128	256	512
	SRAM (Kbytes)	16	64	64
	Cortex-M3 with Memory Protection Unit (MPU)	Yes	Yes	Yes
	10/100 Ethernet MAC	No	Yes	Yes
	External Memory Controller (EMC)	24-bit address, 16-bit data	24-bit address, 16-bit data	24-bit address, 16-bit data
	DMA	8 Ch	8 Ch	8 Ch
	I ² C	2	2	2
	SPI	2	2	2
	16550 UART	2	2	2
	32-Bit Timer	2	2	2
	PLL	1	1	2
	32 KHz Low Power Oscillator	1	1	1
	100 MHz On-Chip RC Oscillator	1	1	1
	Main Oscillator (32 KHz to 20 MHz)	1	1	1
Programmable Analog	ADCs (8-/10-/12-bit SAR)	1	2	3
	DACs (12-bit sigma-delta)	1	2	3
	Signal Conditioning Blocks (SCBs)	1	4	5
	Comparators ¹	2	8	10
	Current Monitors ¹	1	4	5
	Temperature Monitors ¹	1	4	5
	Bipolar High Voltage Monitors ¹	2	8	10

Note:

1. These functions share I/O pins and may not all be available at the same time.

Package I/Os: MSS + FPGA I/Os

Device	A2F060		A2F200				A2F500			
	CS288	FG256	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
Direct Analog Inputs	6	6	8	8	8	8	8	8	8	12
Shared Analog Inputs ¹	4	4	16	16	16	16	16	16	16	20
Total Analog Inputs	10	10	24	24	24	24	24	24	24	32
Total Analog Outputs	1	1	1	2	2	2	1	2	2	3
MSS I/Os ^{2,3}	28 ⁴	25 ⁴	22	31	25	41	22	31	25	41
FPGA I/Os	68	66	66	78	66	94	66	78	66	128
Total I/Os	107	102	113	135	117	161	113	135	117	204

Notes:

1. These pins are shared between direct analog inputs to the ADCs and voltage/current/temperature monitors.

2. 16 MSS I/Os are multiplexed and can be used as FPGA I/Os, if not needed for the MSS. These I/Os support Schmitt triggers and support only LVTTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V) standards.

3. 9 MSS I/Os are primarily for 10/00 Ethernet MAC and are also multiplexed and can be used as FPGA I/Os if Ethernet MAC is not used in a design. These I/Os support Schmitt triggers and support only LVTTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V) standards.

4. 10/100 Ethernet MAC is not available on A2F060.

For detailed device information, refer to the SmartFusion datasheet: www.actel.com/products/smartfusion/docs.aspx.

SmartFusion—Award Winning Design



Electronic Designs

2010 Best Electronic Design Award



Electronic Products China

2010 Product of the Year Award



Electronic Products

2010 Product of the Year Award



Military Embedded Systems

2010 Editor's Choice Award



Elektra 2010

Embedded System
Product of the Year Award



VDC Research

2010 Embeddy Award for
Best in Show, Hardware



EDN

2010 China Leading Product Award

Learn more about Microsemi SoC Products Group low power and mixed signal FPGAs at www.actel.com.

Microsemi SoC Products Group: 2061 Stierlin Court, Mountain View, CA, 94043-4655 USA, Phone 650.318.4200, Fax 650.318.4600



Microsemi

Microsemi Corporate Headquarters
2381 Morse Avenue, Irvine, CA 92614
Phone: 949.221.7100 Fax: 949.756.0308
www.microsemi.com

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