Integrated Device Technology, Inc.

CMOS STATIC RAMS 16K (4K x 4-BIT)

Separate Data Inputs and Outputs

IDT71681SA/LA
IDT71682SA/LA

FEATURES:

- Separate data inputs and outputs
- IDT71681SA/LA: outputs track inputs during write mode
- IDT71682SA/LA: high-impedance outputs during write mode
- High speed (equal access and cycle time)
  - — Military: 15/20/25/35/45/55/70/85/100ns (max.)
  - — Commercial: 15/20/25/35/45ns (max.)
- Low power consumption
- Battery backup operation—2V data retention (LA version only)
- High-density 24-pin 300-mil Ceramic or Plastic DIP, 24-pin CERPACK, and 28-pin leadless chip carrier
- Produced with advanced CMOS high-performance technology
- CMOS process virtually eliminates alpha particle soft-error rates
- Military product compliant to MIL-STD-883, Class B

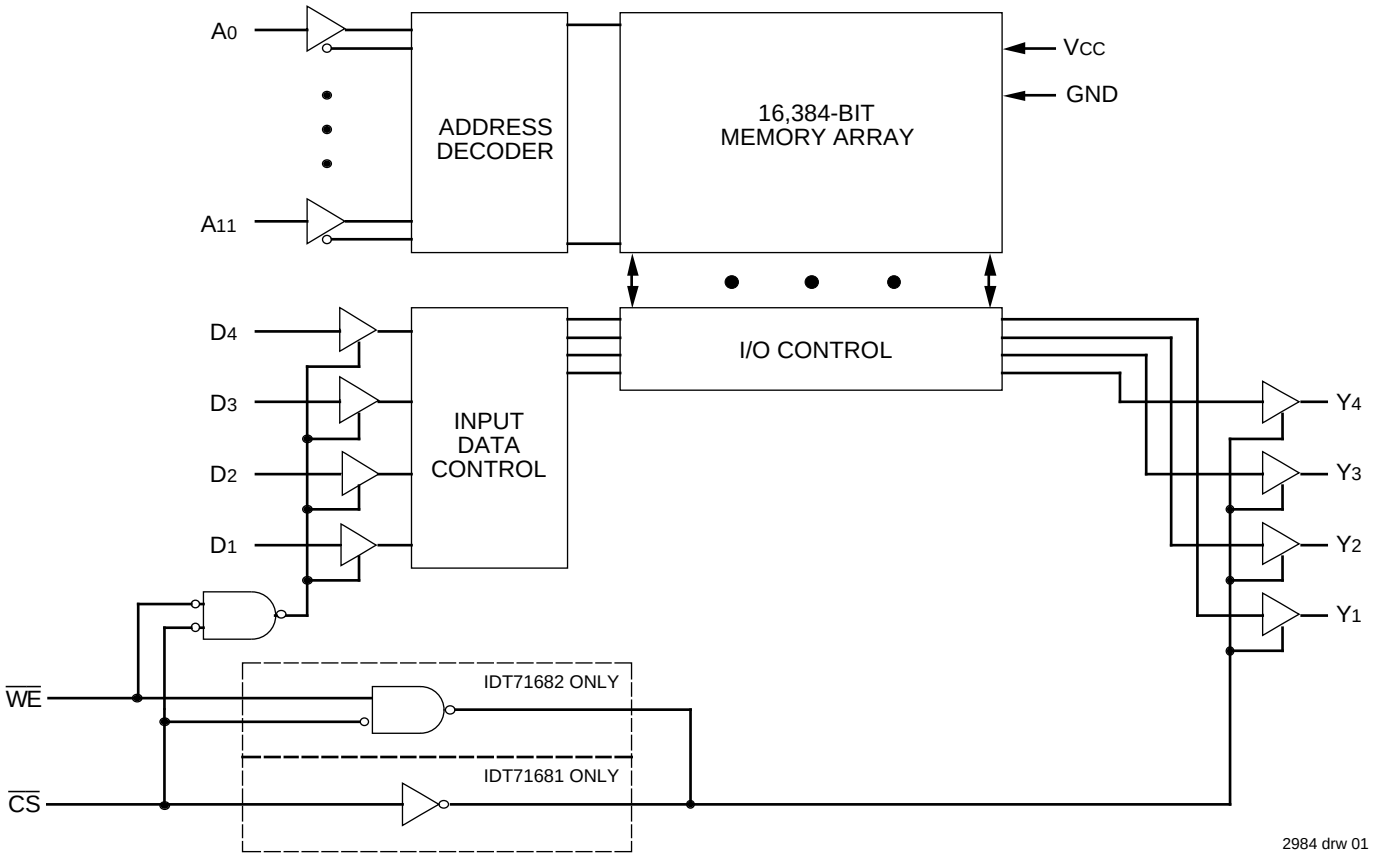
DESCRIPTION:

The IDT71681/IDT71682 are 16,384-bit high-speed static RAMs organized as 4K x 4. They are fabricated using IDT's high-performance, high-reliability technology—CMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective approach for high-speed memory applications.

Access times as fast as 15ns are available. These circuits also offer a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to, and remain in, this standby mode as long as $\overline{CS}$ remains HIGH. In the standby mode, the devices consume less than 10µW, typically. This capability provides significant system-level power and cooling savings. The low-power (LA) versions also offer a battery backup data retention capability where the circuit typically consumes only 1µW operating off a 2V battery.

All inputs and outputs of the IDT71681/IDT71682 are TTL-compatible and operate from a single 5V supply.

FUNCTIONAL BLOCK DIAGRAM

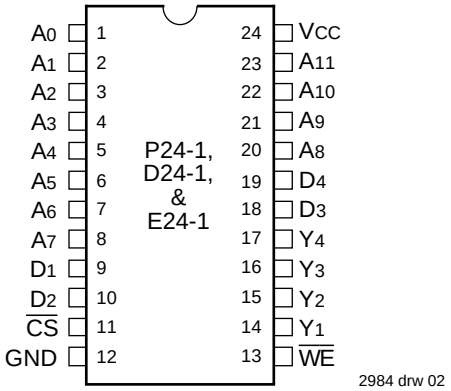


DESCRIPTION (Continued):

The IDT71681/IDT71682 are packaged in either space-saving 24-pin, 300-mil DIPs, CERPACKS, or 28-pin leadless chip carriers.

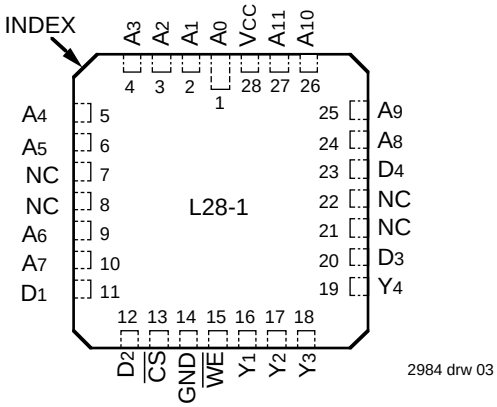
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS



2984 drw 02

DIP/SOIC/SOJ/CERPACK
TOP VIEW



2984 drw 03

LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0 – A11	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
D1 – D4	DATAIN
Y1 – Y4	DATAOUT
VCC	Power
GND	Ground

2984 tbl 01

TRUTH TABLE(3)

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	DATAOUT	Active
Write(1)	L	L	DATAIN	Active
Write(2)	L	L	High-Z	Active

NOTES: 2984 tbl 02
1. For IDT71681 only.
2. For IDT71682 only.
3. H = VIH, L = VIL, X = don't care.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE: 2984 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE: 2984 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2984 tbl 05
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V_{CC}
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2984 tbl 06

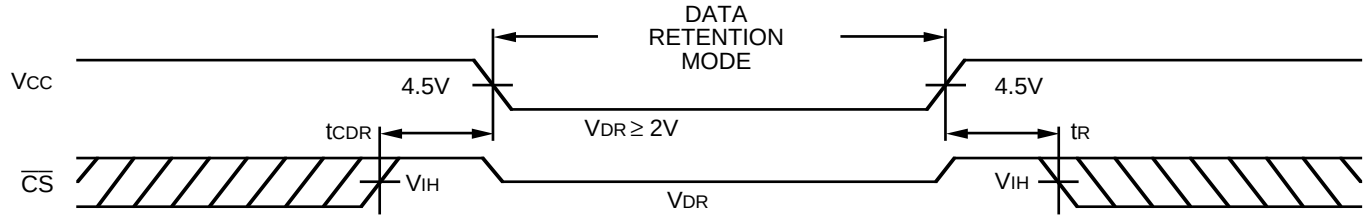
DATA RETENTION CHARACTERISTICS

(LA Version Only; V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	Test Condition		IDT71681/2LA Min.	IDT71681/2LA Typ.(1)	IDT71681/2LA Max.	Unit
V_{DR}	V_{CC} for Data Retention	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		2.0	—	—	V
I_{CCDR}	Data Retention Current		MIL.	— —	0.5(2) 1.0(3)	100(2) 150(3)	µA
			COM'L.	— —	0.5(2) 1.0(3)	20(2) 30(3)	µA
t_{CDR}(5)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(5)	Operation Recovery Time			t_{RC}(4)	—	—	ns

NOTES: 2984 tbl 07
1. T_A = +25°C.
2. At V_{CC} = 2V
3. At V_{CC} = 3V
4. t_{RC} = Read Cycle Time.
5. This parameter is guaranteed by device characterization, but is not production tested.

LOW V_{CC} DATA RETENTION WAVEFORM



2984 drw 04

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT71681/2SA Min.	IDT71681/2SA Typ.	IDT71681/2SA Max.	IDT71681/2LA Min.	IDT71681/2LA Typ.	IDT71681/2LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	— —	10 5	— —	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	— —	10 5	— —	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.			—	0.5	—	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	—	0.4	—	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

2984 tbl 08

DC ELECTRICAL CHARACTERISTICS[1,5]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71681x15 71682x15 Com'l.	71681x15 71682x15 Mil.	71681x20 71682x20 Com'l.	71681x20 71682x20 Mil.	71681x25 71682x25 Com'l.	71681x25 71682x25 Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = 0[3]	SA	110	120	90	100	90	100	mA
		LA	—	—	70	80	70	80	
I_{CC2}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	145	165	120	120	110	120	mA
		LA	—	—	100	110	90	100	
I_{SB}	Standby Power SupplyCurrent (TTL Level) $\overline{CS} \ge V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	SA	55	65	45	55	35	45	mA
		LA	—	—	30	35	25	30	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, V_{CC} = Max., $V_{IN} \ge V_{HC}$ or $V_{IN} \le V_{LC}$, f = 0[3]	SA	20	20	20	20	3	10	mA
		LA	—	—	0.5	0.3	0.5	0.3	

DC ELECTRICAL CHARACTERISTICS (Continued)[1,5]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	Power	71681x35 71682x35 Com'l.	71681x35 71682x35 Mil.	71681x45 71682x45 Com'l.	71681x45 71682x45 Mil.	71681x55[4] 71682x55[4] Com'l.	71681x55[4] 71682x55[4] Mil.	71681x70[2,4] 71682x70[2,4] Com'l.	71681x70[2,4] 71682x70[2,4] Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = 0[3]	SA	90	100	90	100	—	100	—	100	mA
		LA	70	80	70	80	—	80	—	80	
I_{CC2}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	100	110	100	110	—	110	—	110	mA
		LA	80	90	70	80	—	80	—	80	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	SA	30	35	30	35	—	35	—	35	mA
		LA	20	25	20	25	—	20	—	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, V_{CC} = Max., $V_{IN} \ge V_{HC}$ or $V_{IN} \le V_{LC}$, f = 0[3]	SA	3	10	3	10	—	10	—	10	mA
		LA	0.5	0.3	0.5	0.3	—	0.3	—	0.3	

NOTES:

2984 tbl 09

1. All values are maximum guaranteed values.
2. Also available 85 and 100ns military devices.
3. f_{MAX} = 1/tRC, only address inputs are cycling at fMAX. f = 0 means no address inputs are changing.
4. –55°C to +125°C temperature range only.
5. "x" in part numbers indicates power rating (SA or LA).

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2984 tbl 10

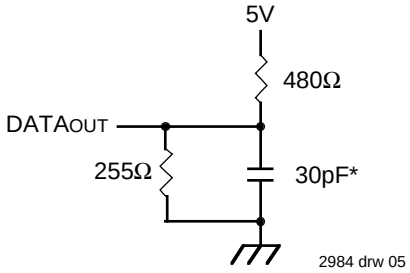


Figure 1. AC Test Load

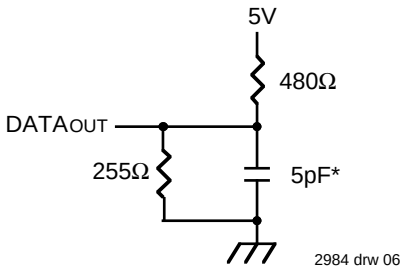


Figure 2. AC Test Load (for t_{CLZ}, t_{CHZ}, t_{WHZ}, and t_{OW})

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS(3) (VCC = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71681x15 71682x15 Min.	71681x15 71682x15 Max.	71681x20 71682x20 Min.	71681x20 71682x20 Max.	71681x25 71682x25 Min.	71681x25 71682x25 Max.	Unit
Read Cycle								
t_{RC}	Read Cycle Time	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	ns
t_{ACS}	Chip Select Access Time	—	15	—	20	—	25	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{CLZ}(2)	Chip Select to Output in Low-Z	5	—	5	—	5	—	ns
t_{CHZ}(2)	Chip Select to Output in High-Z	—	7	—	9	—	10	ns
t_{PU}(2)	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}(2)	Chip Select to Power Down Time	—	15	—	20	—	25	ns

AC ELECTRICAL CHARACTERISTICS(3) (Continued) (VCC = 5.0V ± 10%, All Temperature Ranges)

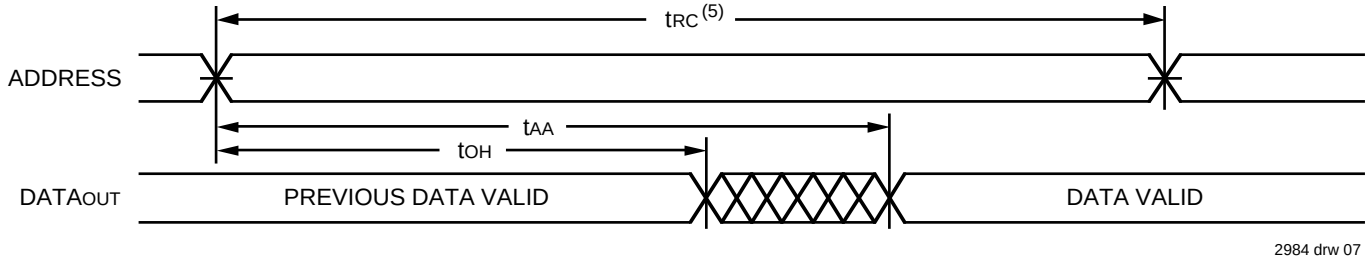
Symbol	Parameter	71681x35 71682x35 Min.	71681x35 71682x35 Max.	71681x45 71682x45 Min.	71681x45 71682x45 Max.	71681x55(1) 71682x55(1) Min.	71681x55(1) 71682x55(1) Max.	71681x70(1) 71682x70(1) Min.	71681x70(1) 71682x70(1) Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	35	—	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	35	—	45	—	55	—	70	ns
t_{ACS}	Chip Select Access Time	—	35	—	45	—	55	—	70	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{CLZ}(2)	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	ns
t_{CHZ}(2)	Chip Select to Output in High-Z	—	15	—	20	—	25	—	30	ns
t_{PU}(2)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}(2)	Chip Select to Power-Down Time	—	35	—	40	—	50	—	60	ns

NOTES:

2984 tbl 11

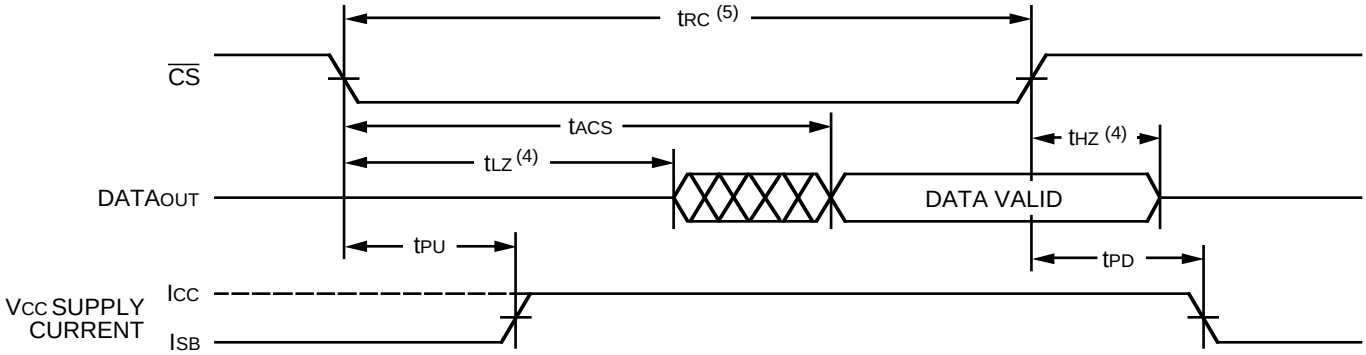
1. –55°C to +125°C temperature range only.
2. This parameter guaranteed with AC Load (Figure 2) by device characterization, but is not production tested.
3. "x" in part numbers indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1(1, 2)



2984 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 3)



2984 drw 08

NOTES:
1. $\overline{WE}$ is HIGH for Read cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. Transition is measured ±200mV from steady state.
5. All read cycle timings are referenced from the last valid address to the first transmitting address.

AC ELECTRICAL CHARACTERISTICS(3) (VCC = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71681x15 71682x15 Min.	71681x15 71682x15 Max.	71681x20 71682x20 Min.	71681x20 71682x20 Max.	71681x25 71682x25 Min.	71681x25 71682x25 Max.	Unit
Write Cycle								
tWC	Write Cycle Time	15	—	20	—	20	—	ns
tCW	Chip Select to End of Write	15	—	20	—	20	—	ns
tAW	Address Valid to End of Write	15	—	20	—	20	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	9	—	10	—	10	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	ns
tIY(2)	Data Valid to Output Valid (71681 only)	—	15	—	20	—	25	ns
tWY(2)	Write Enable to Output Valid (71681 only)	—	15	—	20	—	25	ns
tWHZ(2)	Write Enable to Output in High-Z (71682 only)	—	6	—	7	—	7	ns
tOW(2)	Output Active from End of Write (71682 only)	0	—	0	—	0	—	ns

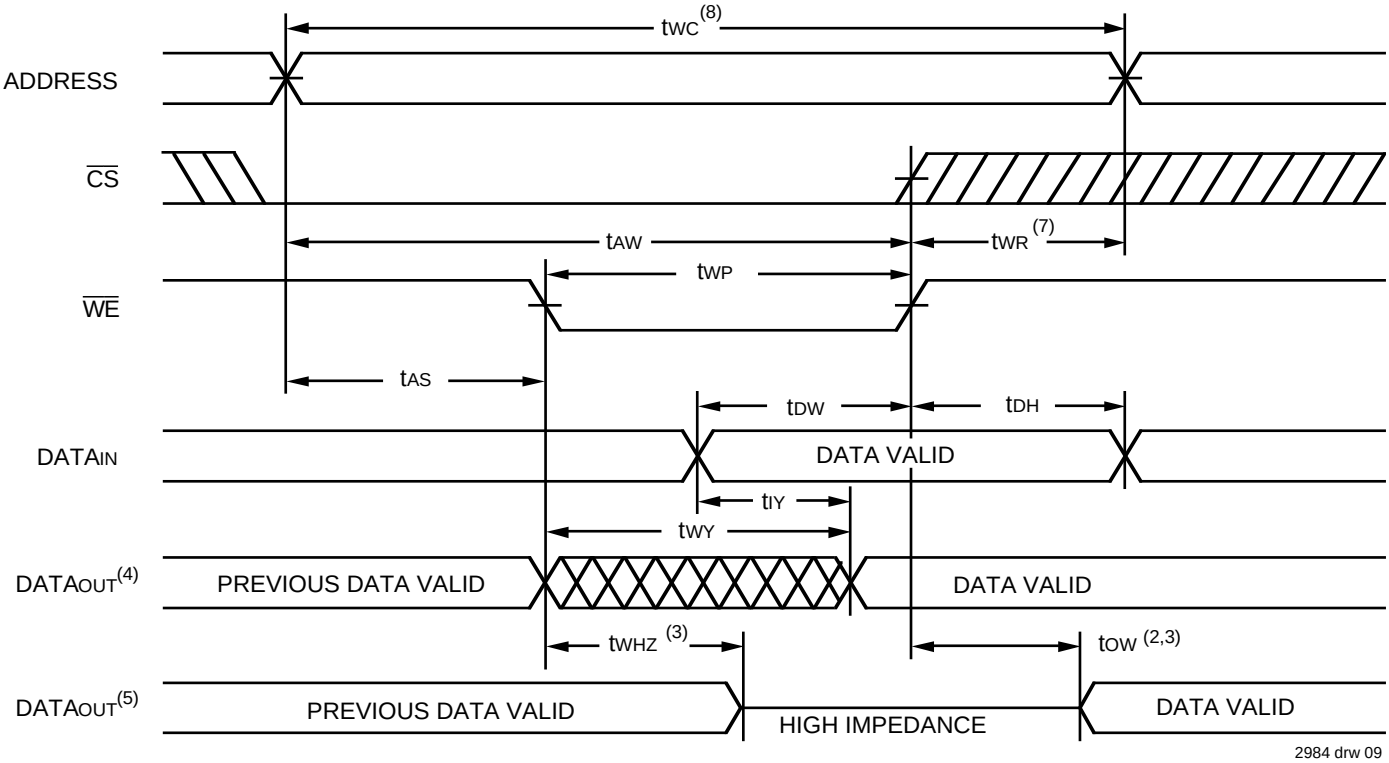
AC ELECTRICAL CHARACTERISTICS (Continued) (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71681x35 71682x35 Min.	71681x35 71682x35 Max.	71681x45 71682x45 Min.	71681x45 71682x45 Max.	71681x55[1] 71682x55[1] Min.	71681x55[1] 71682x55[1] Max.	71681x70[1] 71682x70[1] Min.	71681x70[1] 71682x70[1] Max.	Unit
Write Cycle										
t_{WC}	Write Cycle Time	30	—	40	—	50	—	60	—	ns
t_{CW}	Chip Select to End of Write	25	—	35	—	50	—	60	—	ns
t_{AW}	Address Valid to End of Write	25	—	35	—	50	—	60	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	35	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	15	—	20	—	20	—	25	—	ns
t_{DH}	Data Hold Time	3	—	3	—	3	—	3	—	ns
t_{IY}[2]	Data Valid to Output Valid (71681 only)	—	30	—	35	—	35	—	40	ns
t_{WY}[2]	Write Enable to Output Valid (71681 only)	—	30	—	35	—	35	—	40	ns
t_{WHZ}[2]	Write Enable to Output in High-Z (71682 only)	—	13	—	20	—	25	—	30	ns
t_{OW}[2]	Output Active from End of Write (71682 only)	0	—	0	—	0	—	0	—	ns

NOTES: 2984 tbl 12

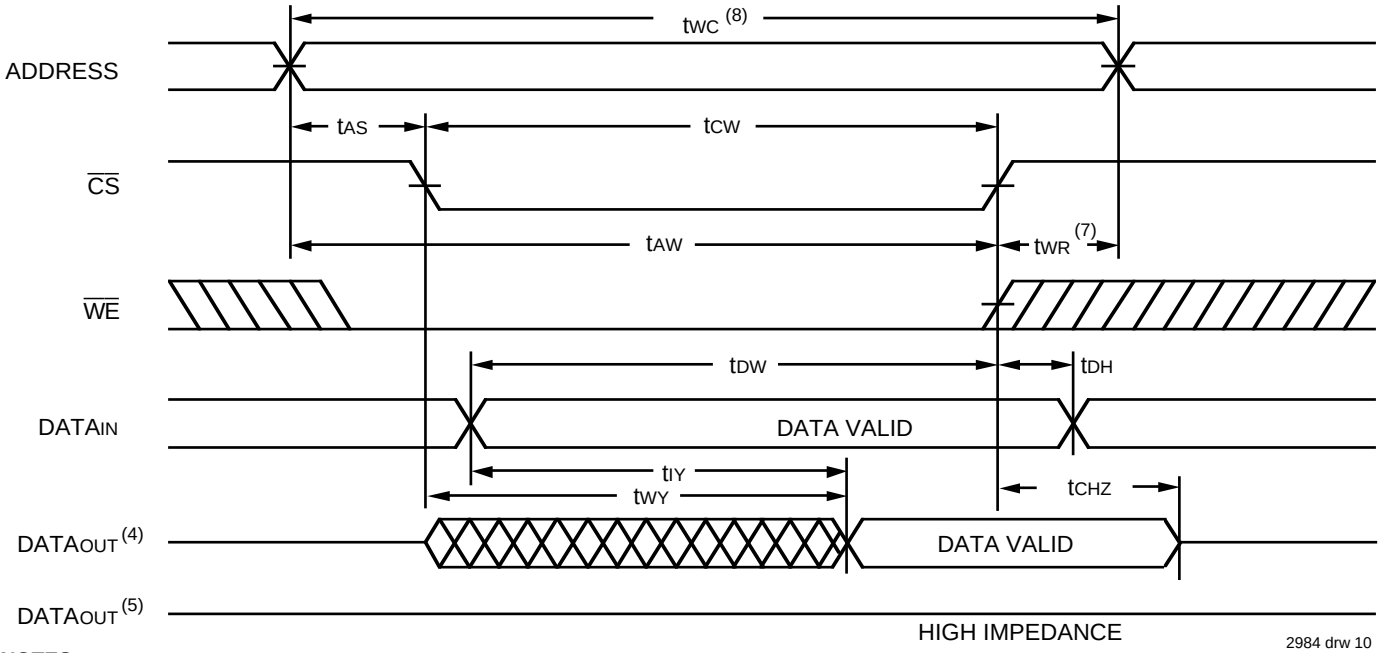
1. –55°C to +125°C temperature range only.
2. This parameter guaranteed with AC Load (Figure 2) by device characterization, but is not production tested.
3. "x" in part numbers indicates power rating (SA or LA).

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1,7]



2984 drw 09

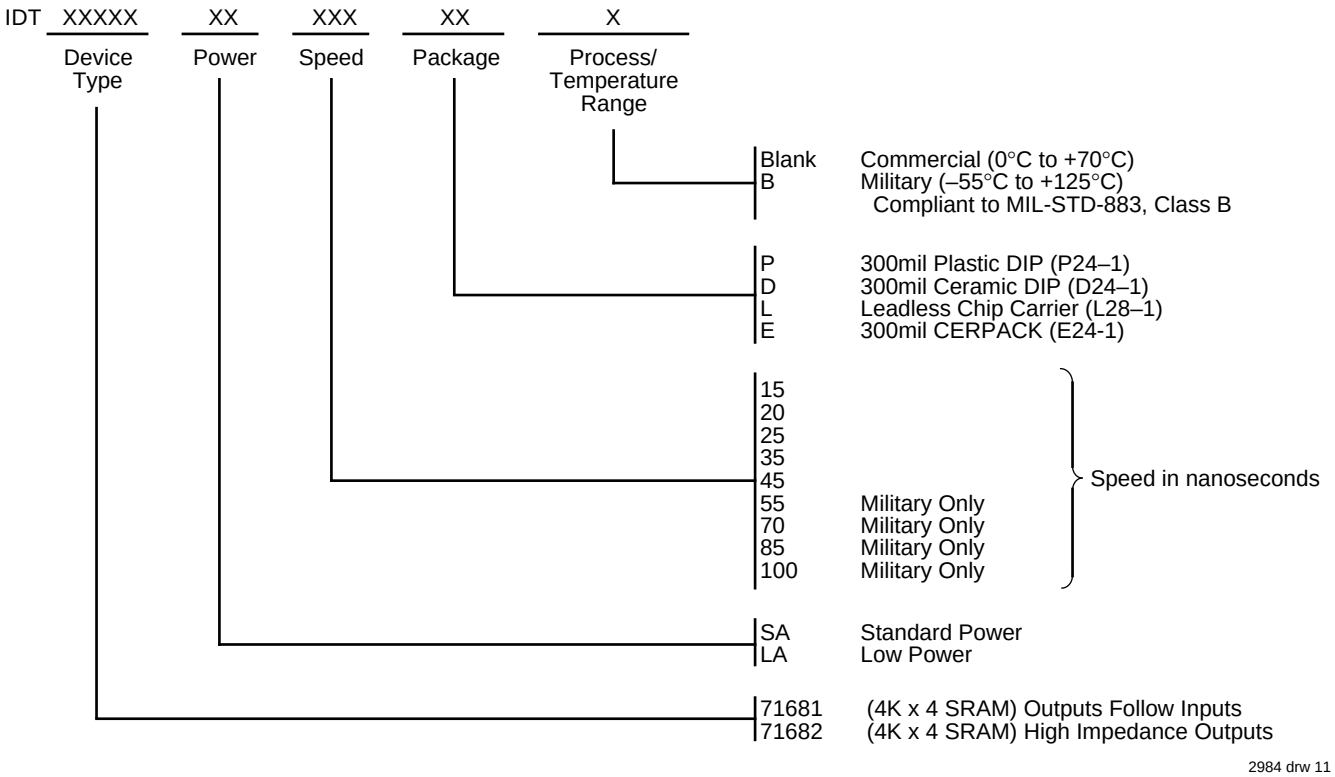
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1,6)



2984 drw 10

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. If the $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the outputs remain in a high-impedance state.
3. Transition is measured ±200mV from steady state.
4. For IDT71681 only.
5. For IDT71682 only.
6. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
7. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
8. All write cycle timings are referenced from the last valid address to the first transitioning address.

ORDERING INFORMATION



2984 drw 11