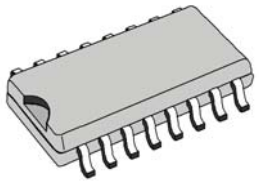
HVLED807PF

Offline LED driver with primary-sensing and high power factor up to 7 W

Datasheet – production data

Features

- High power factor capability (> 0.9)
- 800 V, avalanche rugged internal 11 Ω power MOSFET
- Internal high-voltage startup
- Primary sensing regulation (PSR)
- +/- 5% accuracy on constant LED output current
- Quasi-resonant (QR) operation
- Optocoupler not needed
- Open or short LED string management
- Automatic self supply



SO16N

Table 1. Device summary

Order code	Package	Packaging
HVLED807PF	SO16N	Tube
HVLED807PFTR		Tape & Reel

Applications

- AC-DC LED driver bulb replacement lamps up to 7 W, with high power factor
- AC-DC LED drivers up to 7 W

Description

The HVLED807PF is a high-voltage primary switcher intended for operating directly from the rectified mains with minimum external parts and enabling high power factor (> 0.90) to provide an efficient, compact and cost effective solution for LED driving. It combines a high-performance low-voltage PWM controller chip and an 800 V, avalanche-rugged Power MOSFET, in the same package. There is no need for the optocoupler thanks to the patented primary sensing regulation (PSR) technique. The device assures protection against LED string fault (open or short).

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1 Principle application circuit and block diagram

1.1 Principle application circuit

Figure 1. Application circuit for high power factor LED driver - single range input

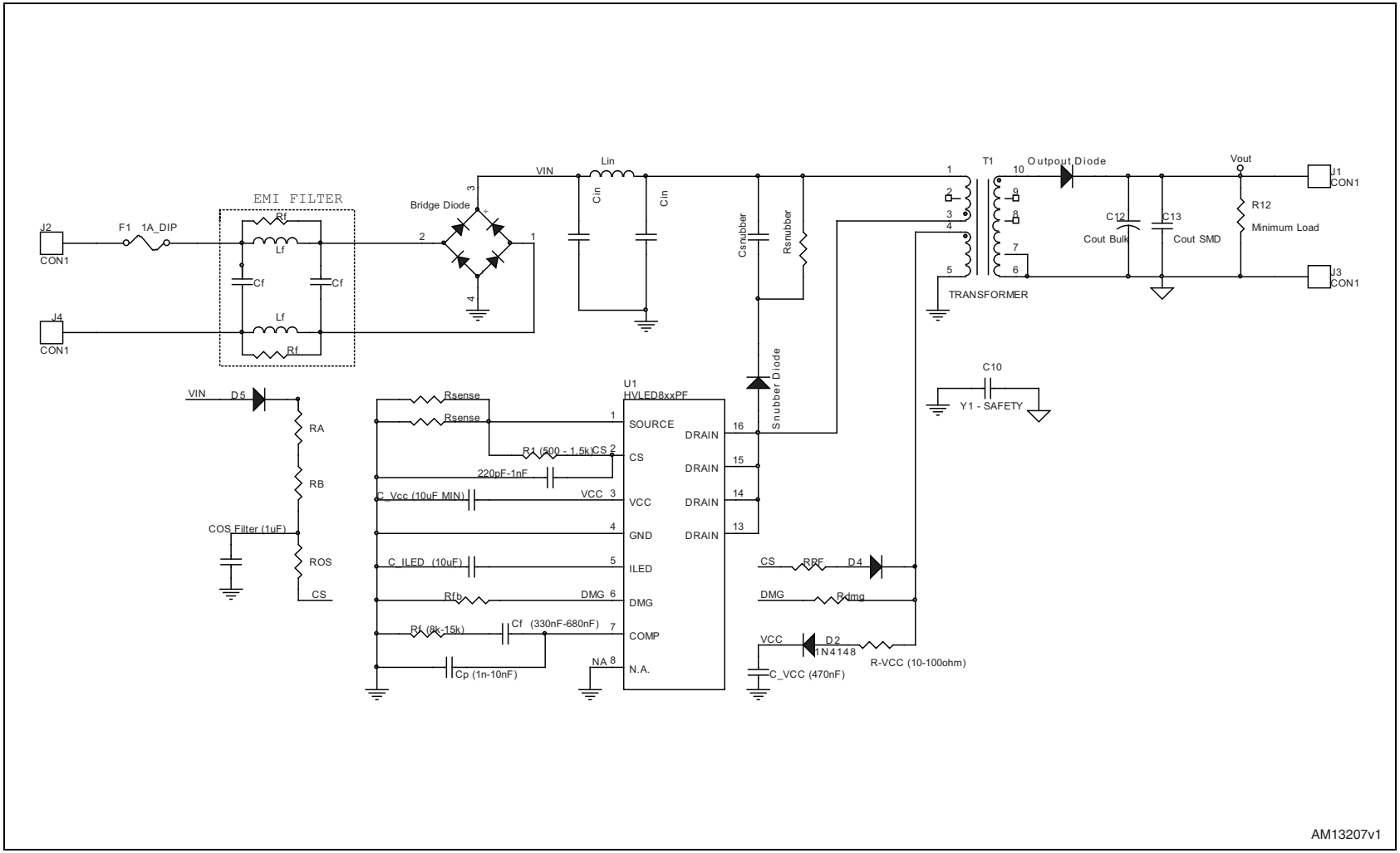
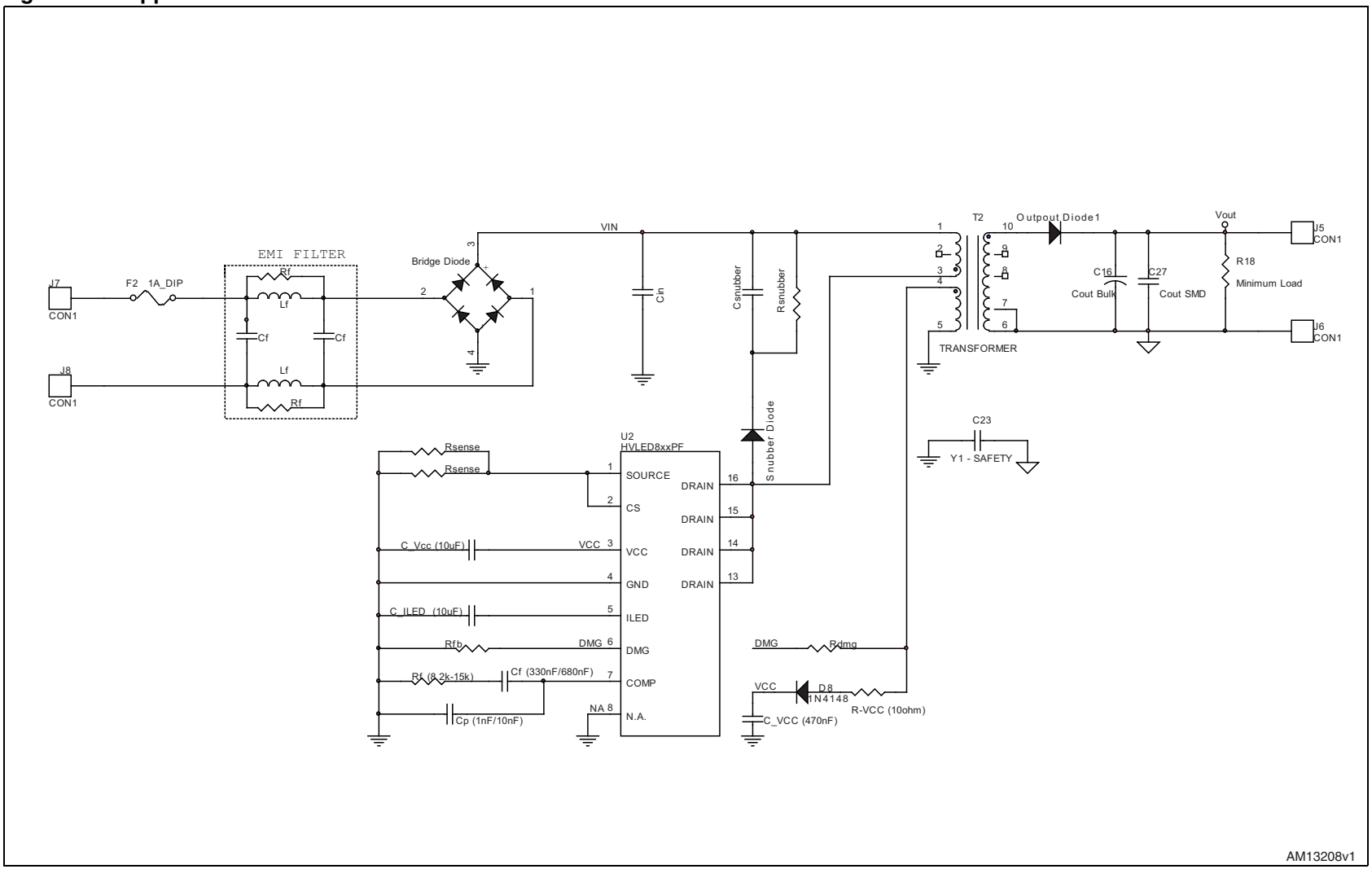
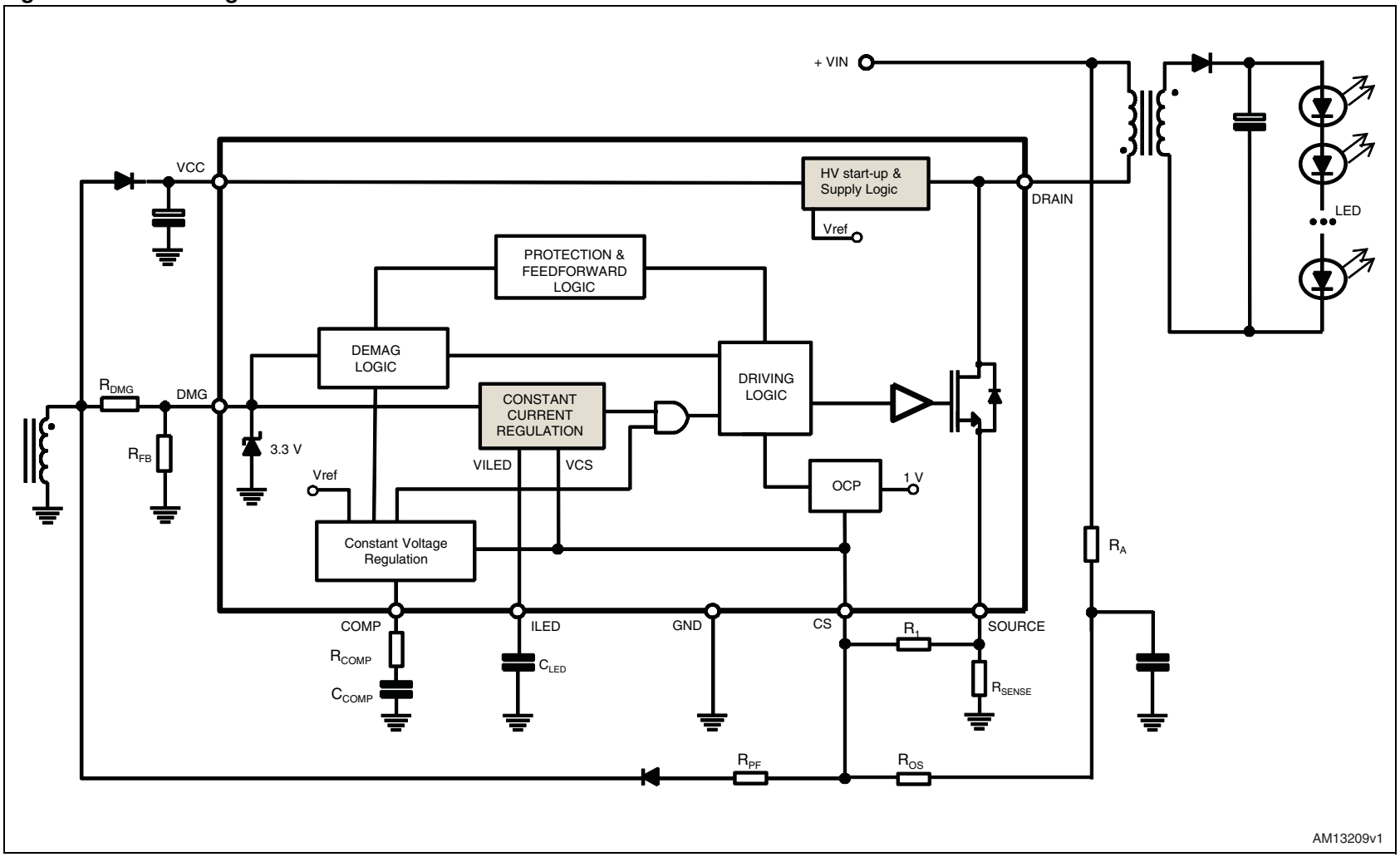


Figure 2. Application circuit for standard LED driver



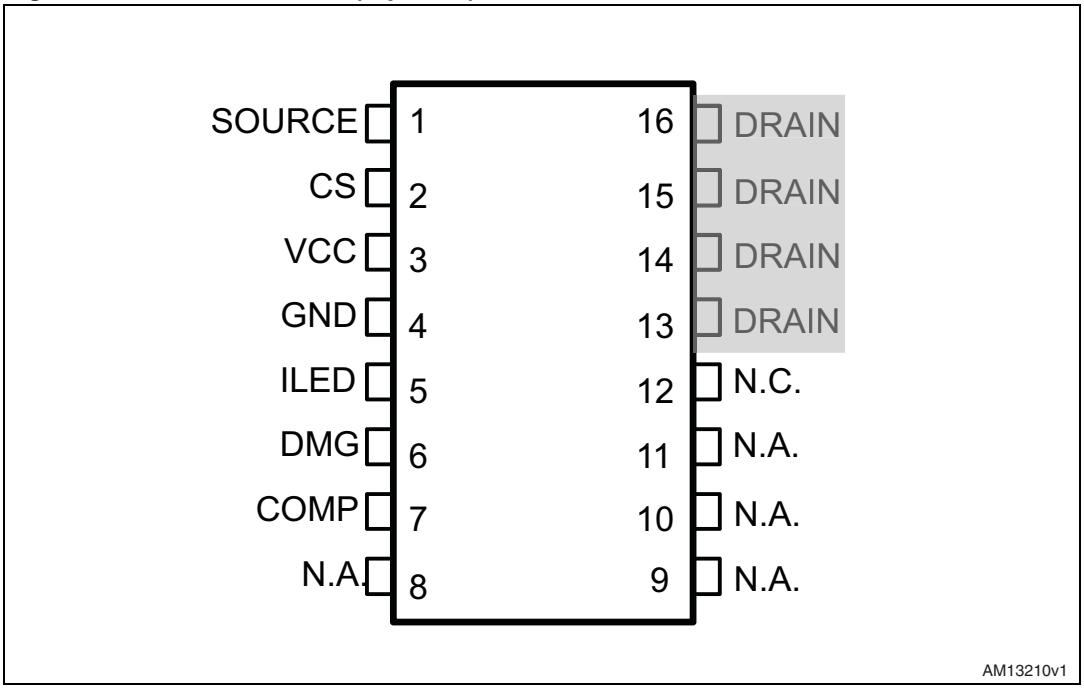
1.2 Block diagram

Figure 3. Block diagram



2 Pin description and connection diagrams

Figure 4. Pin connection (top view)



2.1 Pin description

Table 2. Pin description

N.	Name	Function
1	SOURCE	Source connection of the internal power section.
2	CS	Current sense input. Connect this pin to the SOURCE pin (through an R1 resistor) to sense the current flowing in the MOSFET through an R_{SENSE} resistor connected to GND. The CS pin is also connected through dedicated ROS, RPF resistors to the input and auxiliary voltage, in order to modulate the input current flowing in the MOSFET according to the input voltage and therefore achieving a high power factor. See dedicated section for more details. The resulting voltage is compared with the voltage on the ILED pin to determine MOSFET turn-off. The pin is equipped with 250 ns blanking time after the gate-drive output goes high for improved noise immunity. If a second comparison level located at 1 V is exceeded, the IC is stopped and restarted after V_{CC} has dropped below 5 V.

Table 2. Pin description (continued)

N.	Name	Function
3	VCC	Supply voltage of the device. A capacitor, connected between this pin and ground, is initially charged by the internal high-voltage startup generator; when the device is running, the same generator keeps it charged in case the voltage supplied by the auxiliary winding is not sufficient. This feature is disabled in case a protection is tripped. A small bypass capacitor (100 nF typ.) to GND may be useful to get a clean bias voltage for the signal part of the IC.
4	GND	Ground. Current return for both the signal part of the IC and the gate drive. All of the ground connections of the bias components should be tied to a trace going to this pin and kept separate from any pulsed current return.
5	ILED	Constant current (CC) regulation loop reference voltage. An external capacitor C_{LED} is connected between this pin and GND. An internal circuit develops a voltage on this capacitor that is used as the reference for the MOSFET's peak drain current during CC regulation. The voltage is automatically adjusted to keep the average output current constant.
6	DMG	Transformer demagnetization sensing for quasi-resonant operation and output voltage monitor. A negative-going edge triggers the MOSFET turn-on, to achieve quasi-resonant operation (zero voltage switching). The pin voltage is also sampled-and-held right at the end of transformer demagnetization to get an accurate image of the output voltage to be fed to the inverting input of the internal, transconductance-type, error amplifier, whose non-inverting input is referenced to 2.5 V. The maximum I_{DMG} sunk/sourced current must not exceed ± 2 mA (AMR) in all the Vin range conditions. No capacitor is allowed between the pin and the auxiliary transformer.
7	COMP	Output of the internal transconductance error amplifier. The compensation network is placed between this pin and GND to achieve stability and good dynamic performance of the voltage control loop.
8	N.a.	Not available. These pins must be connected to GND.
9-11	N.a.	Not available. These pins must be left not connected.
12	N.c.	Not internally connected. Provision for clearance on the PCB to meet safety requirements.
13 to 16	DRAIN	Drain connection of the internal power section. The internal high-voltage startup generator sinks current from this pin as well. Pins connected to the internal metal frame to facilitate heat dissipation.

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Max. value	Unit
R_{thJP}	Thermal resistance, junction-to-pin	10	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	110	°C/W

Table 3. Thermal data (continued)

Symbol	Parameter	Max. value	Unit
P_{TOT}	Maximum power dissipation at T_A = 50 °C	0.9	W
T_{STG}	Storage temperature range	-55 to 150	°C
T_J	Junction temperature range	-40 to 150	°C

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{DS}	1, 13-16	Drain-to-source (ground) voltage	-1 to 800	V
I_D	1, 13-16	Drain current (1)	1	A
Eav	1, 13-16	Single pulse avalanche energy (T_j = 25 °C, I_D = 0.7 A)	50	mJ
V_{CC}	3	Supply voltage (Icc < 25 mA)	Self limiting	V
I_{DMG}	6	Zero current detector current	±2	mA
V_{CS}	2	Current sense analog input	-0.3 to 3.6	V
Vcomp	7	Analog input	-0.3 to 3.6	V

1. Limited by maximum temperature allowed.

3.2 Electrical characteristics

Table 5. Electrical characteristics(1) (2)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Power section						
$V_{(BR)DSS}$	Drain-source breakdown	I_D < 100 µA; Tj = 25 °C	800			V
I_{DSS}	OFF-state drain current	V_{DS} = 750 V; Tj = 125 °C (3) see *Figure 5*			80	µA
$R_{DS(on)}$	Drain-source ON-state resistance	Id = 250 mA; Tj = 25 °C		11	14	Ω
		Id = 250 mA; Tj = 125 °C (3)			28	
C_{OSS}	Effective (energy-related) output capacitance	(3) See *Figure 6*				
High-voltage startup generator						
V_{START}	Min. drain start voltage	I_{charge} < 100 µA	40	50	60	V
I_{CHARGE}	V_{CC} startup charge current	V_{DRAIN} > V_{Start}; Vcc < V_{CCon} Tj = 25 °C	4	5.5	7	mA
		V_{DRAIN} > V_{Start}; Vcc < Vcc_{On}	+/- 10%			
$V_{CC\_RESTART}$	V_{CC} restart voltage (V_{CC} falling)	(4)	9.5	10.5	11.5	V
		After protection tripping		5		

Table 5. Electrical characteristics(1) (2) (continued)

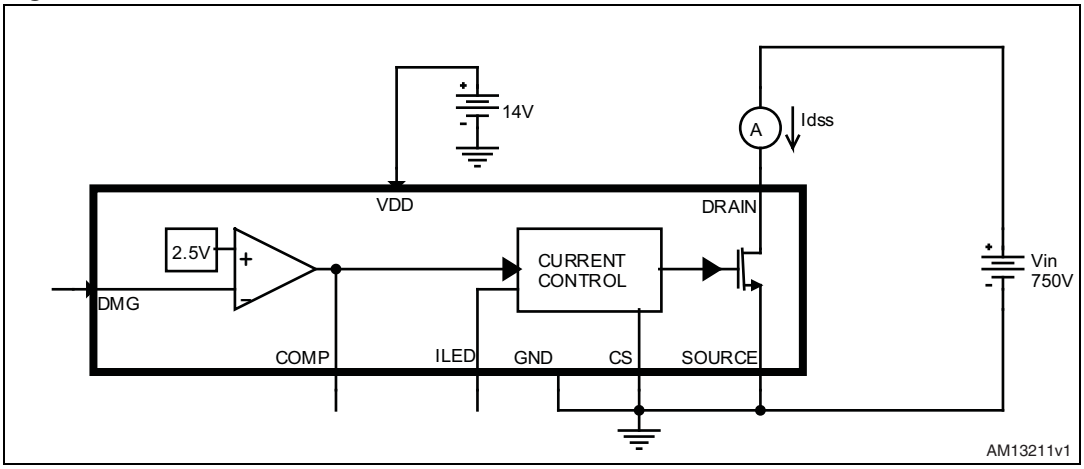
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltage						
V_{CC}	Operating range	After turn-on	11.5		23	
V_{CC_ON}	Turn-on threshold	(4)	12	13	14	V
V_{CC_OFF}	Turn-off threshold	(4)	9	10	11	V
V_Z	Internal Zener voltage	Icc = 20 mA	23	25	27	V
Supply current						
$I_{CC\_START-UP}$	Startup current	See *Figure 7*		200	300	µA
Iq	Quiescent current	See *Figure 8*		1	1.4	mA
I_{CC}	Operating supply current at 50 kHz	See *Figure 9*		1.4	1.7	mA
$Iq_{(fault)}$	Fault quiescent current	See *Figure 10*		250	350	µA
Startup timer						
T_{START}	Start timer period		105	140	175	µs
$T_{RESTART}$	Restart timer period during burst mode		420	500	700	µs
Demagnetization detector						
I_{Dmgb}	Input bias current	V_{DMG} = 0.1 to 3 V		0.1	1	µA
V_{DMGH}	Upper clamp voltage	I_{DMG} = 1 mA	3.0	3.3	3.6	V
V_{DMGL}	Lower clamp voltage	I_{DMG} = - 1 mA	-90	-60	-30	mV
V_{DMGA}	Arming voltage	Positive-going edge	100	110	120	mV
V_{DMGT}	Triggering voltage	Negative-going edge	50	60	70	mV
T_{BLANK}	Trigger blanking time after MOSFET turn-off	$V_{COMP} \geq 1.3$ V		6		µs
		V_{COMP} = 0.9 V		30		
Line feedforward						
R_{FF}	Equivalent feedforward resistor	I_{DMG} = 1 mA		45		Ω
Transconductance error amplifier						
V_{REF}	Voltage reference	T_j = 25 °C	2.45	2.51	2.57	V
		(3) Tj = -25 to 125 °C and V_{CC} = 12 V to 23 V	2.4		2.6	
gm	Transconductance	ΔI_{COMP} = ± 10 µA V_{COMP} = 1.65 V	1.3	2.2	3.2	ms
Gv	Voltage gain	(5) Open loop		73		dB
GB	Gain-bandwidth product	(5)		500		KHz
I_{COMP}	Source current	V_{DMG} = 2.3 V, V_{COMP} = 1.65 V	70	100		µA
	Sink current	V_{DMG} = 2.7 V, V_{COMP} = 1.65 V	400	750		µA

Table 5. Electrical characteristics(1) (2) (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{COMPH}	Upper COMP voltage	V_{DMG} = 2.3 V		2.7		V
V_{COMPL}	Lower COMP voltage	V_{DMG} = 2.7 V		0.7		V
V_{COMPBM}	Burst-mode threshold			1		V
Hys	Burst-mode hysteresis			65		mV
Current reference						
V_{ILEDx}	Maximum value	$V_{COMP} = V_{COMPL}$	1.5	1.6	1.7	V
V_{CLED}	Current reference voltage		0.192	0.2	0.208	V
Current sense						
t_{LEB}	Leading-edge blanking	(5)		330		ns
T_D	Delay-to-output (H-L)			90	200	ns
V_{CSx}	Max. clamp value	(4) dVcs/dt = 200 mV/µs	0.7	0.75	0.8	V
V_{CSdis}	Hiccup-mode OCP level	(4)	0.92	1	1.08	V

1. V_{CC}=14 V (unless otherwise specified).
2. Limits are production tested at Tj=Ta=25 °C, and are guaranteed by statistical characterization in the range Tj -25 to +125 °C.
3. Not production tested, guaranteed statistical characterization only.
4. Parameters tracking each other (in the same section).
5. Guaranteed by design.

Figure 5. OFF-state drain and source current test circuit



Note: The measured IDSS is the sum between the current across the startup resistor and the effective MOSFET's OFF-state drain current.

Figure 6. COSS output capacitance variation

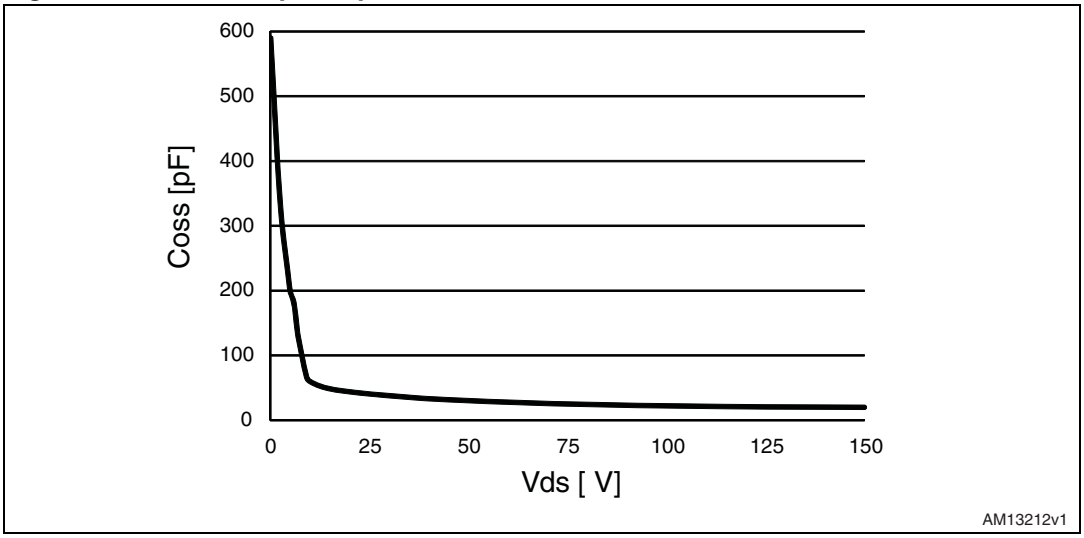


Figure 7. Startup current test circuit

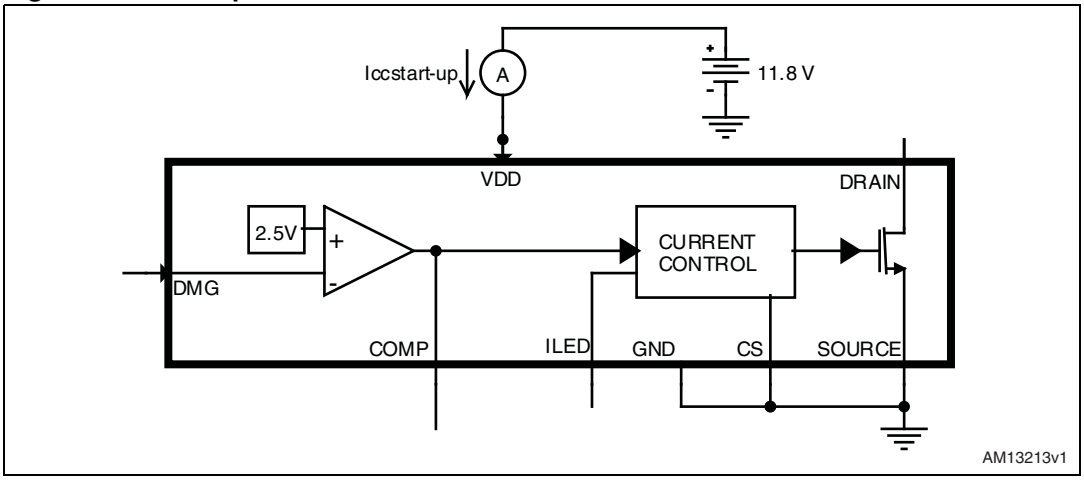


Figure 8. Quiescent current test circuit

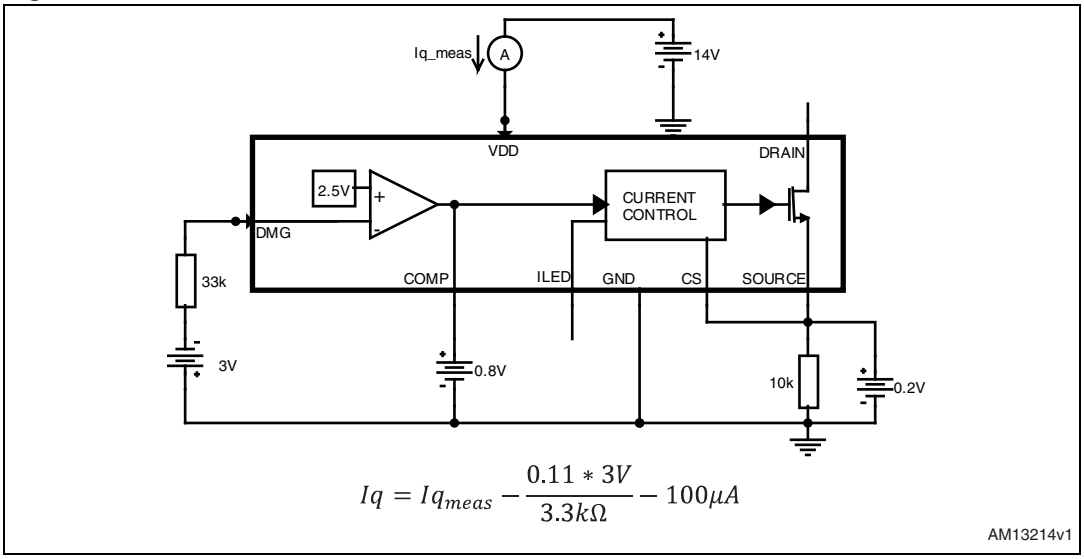
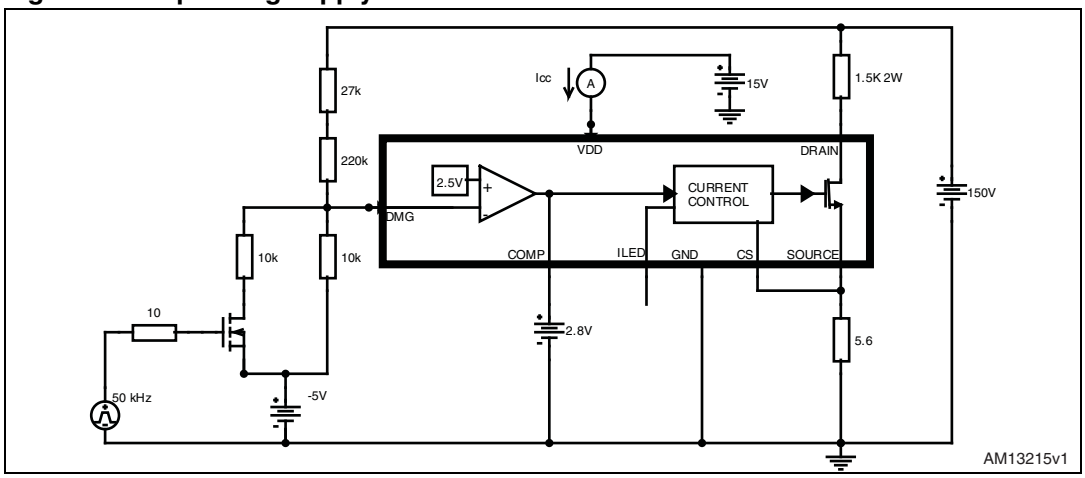
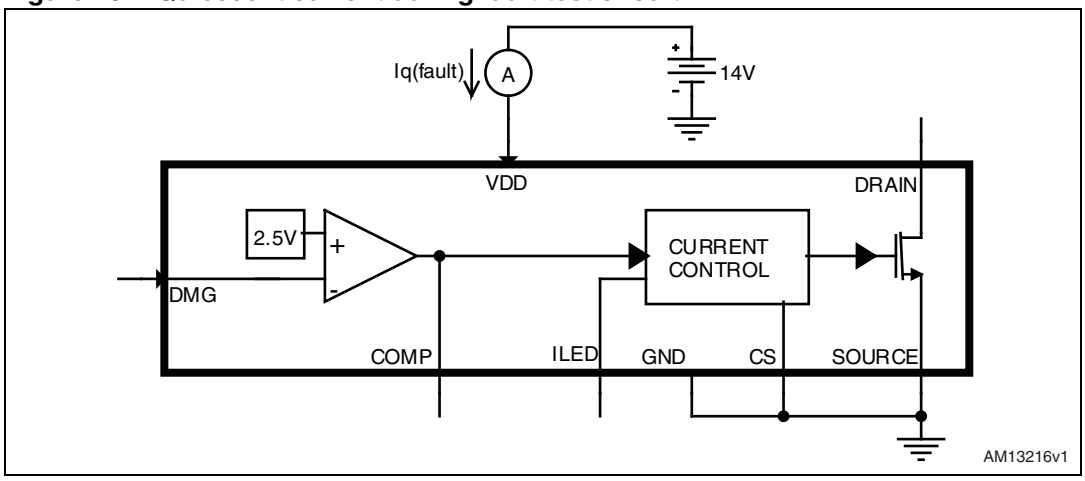


Figure 9. Operating supply current test circuit



Note: The circuit across the DMG pin is used for switch-on synchronization.

Figure 10. Quiescent current during fault test circuit



4 Device description

The HVLED807PF is a high-voltage primary switcher intended for operating directly from the rectified mains with minimum external parts to provide high power factor (> 0.90) and an efficient, compact and cost effective solution for LED driving. It combines a high-performance low-voltage PWM controller chip and an 800 V, avalanche-rugged Power MOSFET, in the same package.

The PWM is a current-mode controller IC specifically designed for ZVS (Zero Voltage Switching) flyback LED drivers, with constant output current (CC) regulation using primary sensing feedback (PSR). This eliminates the need for the optocoupler, the secondary voltage reference, as well as the current sense on the secondary side, while still maintaining a good LED current accuracy. Moreover, it guarantees a safe operation when short-circuit of one or more LEDs occurs.

The device can also provide a constant output voltage regulation (CV): it allows the application to be able to work safely when the LED string opens due to a failure.

In addition, the device offers the shorted secondary rectifier (i.e. LED string shorted due to a failure) or transformer saturation detection.

Quasi-resonant operation is achieved by means of a transformer demagnetization sensing input that triggers MOSFET turn-on. This input serves also as both output voltage monitor, to perform CV regulation, and input voltage monitor, to achieve mains-independent CC regulation (line voltage feedforward).

The maximum switching frequency is top-limited below 166 kHz, so that at medium-light load a special function automatically lowers the operating frequency still maintaining the operation as close to ZVS as possible. At very light load, the device enters a controlled burst-mode operation that, along with the built-in high-voltage startup circuit and the low operating current of the device, helps minimize the residual input consumption.

Although an auxiliary winding is required in the transformer to correctly perform CV/CC regulation, the chip is able to power itself directly from the rectified mains. This is useful especially during CC regulation, where the flyback voltage generated by the winding drops.

4.1 Application information

The device is an off-line led driver with all-primary sensing, based on quasi-resonant flyback topology, with high power factor capability. In particular, using different application schematic the device is able to provide a compact, efficient and cost-effective led driver solution with high power factor (PF>0.9 - see application schematic on *Figure 1*) or with standard power factor (PF>0.5/0.6 - see application schematic on *Figure 2*), based on the specific application requirements.

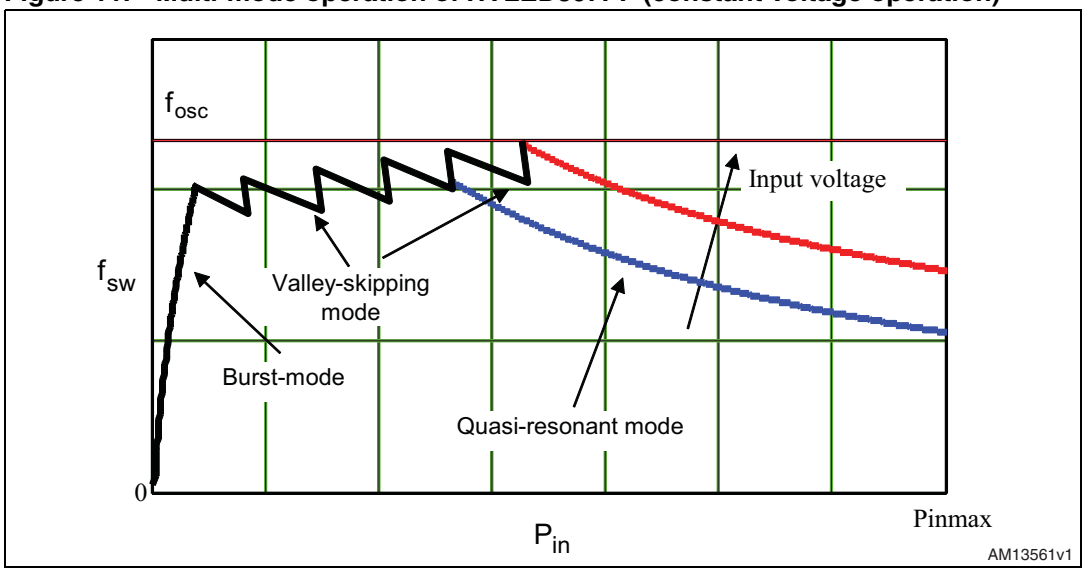
Referring to the application schematic on *Figure 1*, the IC modulates the input current in according to the input voltage providing the high power factor capability (PF>0.9) keeping a good line regulation. This application schematic is intended for a single range input voltage.

For wide range application a different reference schematic can be used; refer to the dedicated application note for further details.

Moreover, the device is able to work in different modes depending on the LED's driver load condition (see *Figure 11*):

1. QR mode at heavy load. Quasi-resonant operation lies in synchronizing MOSFET's turn-on to the transformer's demagnetization by detecting the resulting negative-going edge of the voltage across any winding of the transformer. Then the system works close to the boundary between discontinuous (DCM) and continuous conduction (CCM) of the transformer. As a result, the switching frequency is different for different line/load conditions (see the hyperbolic-like portion of the curves in *Figure 11*). Minimum turn-on losses, low EMI emission and safe behavior in short circuit are the main benefits of this kind of operation.
2. Valley-skipping mode at medium/ light load. Depending on voltage on COMP pin, the device defines the maximum operating frequency of the converter. As the load is reduced MOSFET's turn-on does not occur any more on the first valley but on the second one, the third one and so on. In this way the switching frequency is no longer increased (piecewise linear portion in *Figure 11*).
3. Burst-mode with no or very light load. When the load is extremely light or disconnected, the converter enters a controlled on/off operation with constant peak current. Decreasing the load result in frequency reduction, which can go down even to few hundred hertz, thus minimizing all frequency-related losses and making it easier to comply with energy saving regulations or recommendations. Being the peak current very low, no issue of audible noise arises.

Figure 11. Multi-mode operation of HVLED807PF (constant voltage operation)



4.2 Power section and gate driver

The power section guarantees safe avalanche operation within the specified energy rating as well as high dv/dt capability. The Power MOSFET has a V_{DSS} of 800 V min. and a typical $R_{DS(on)}$ of 11 Ω

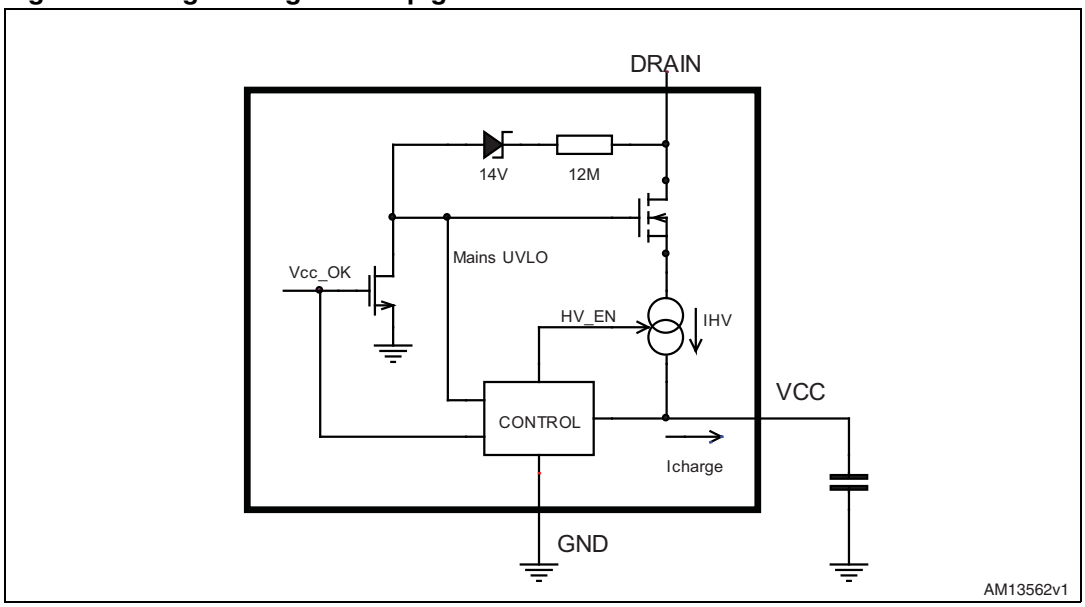
The internal gate driver of the power MOSFET is designed to supply a controlled gate current during both turn-on and turn-off in order to minimize common mode EMI. Under UVLO conditions an internal pull-down circuit holds the gate low in order to ensure that the power MOSFET cannot be turned on accidentally.

4.3 High voltage startup generator

Figure 12 shows the internal schematic of the high-voltage start-up generator (HV generator). It includes an 800 V-rated N-channel MOSFET, whose gate is biased through the series of a 12 MΩ resistor and a 14 V Zener diode, with a controlled, temperature compensated current generator connected to its source.

The HV generator input is in common with the DRAIN pins, while its output is the supply pin of the device (VCC pin). A mains "UVLO" circuit (separated from the UVLO of the device that sense VCC) keeps the HV generator off if the drain voltage is below VSTART (50 V typical value).

Figure 12. High-voltage start-up generator: internal schematic



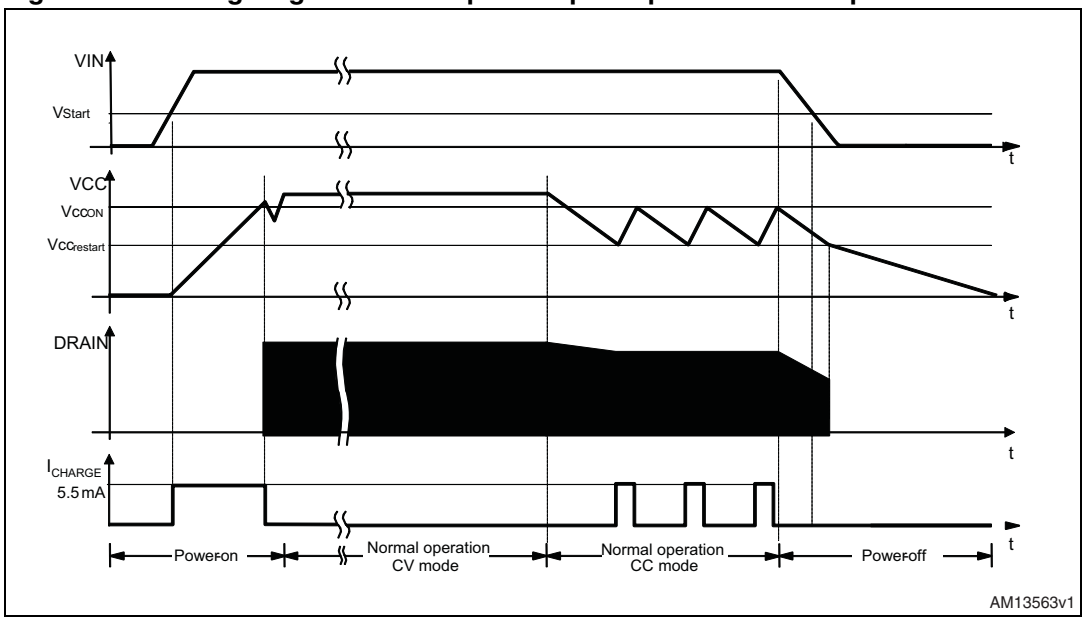
With reference to the timing diagram of *Figure 13*, when power is applied to the circuit and the voltage on the input bulk capacitor is high enough, the HV generator is sufficiently biased to start operating, thus it will draw about 5.5 mA (typical) to the V_{CC} capacitor.

Most of this current will charge the bypass capacitor connected between the VCC pin and ground and make its voltage rise linearly. As soon as the VCC pin voltage reaches the V_{CC_ON} turn on threshold (13 V typ) the chip starts operating, the internal power MOSFET is enabled to switch and the HV generator is cut off by the Vcc_OK signal asserted high. The IC is powered by the energy stored in the VCC capacitor.

The chip is able to power itself directly from the rectified mains: when the voltage on the VCC pin falls below $V_{CC\_RESTART}$ (10.5 V typ.), during each MOSFET's off-time the HV current generator is turned on and charges the supply capacitor until it reaches the V_{CC_ON} threshold.

In this way, the self-supply circuit develops a voltage high enough to sustain the operation of the device. This feature is useful especially during constant current (CC) regulation, when the flyback voltage generated by the auxiliary winding alone may not be able to keep VCC pin above $V_{CC\_RESTART}$.

Figure 13. Timing diagram: normal power-up and power-down sequences

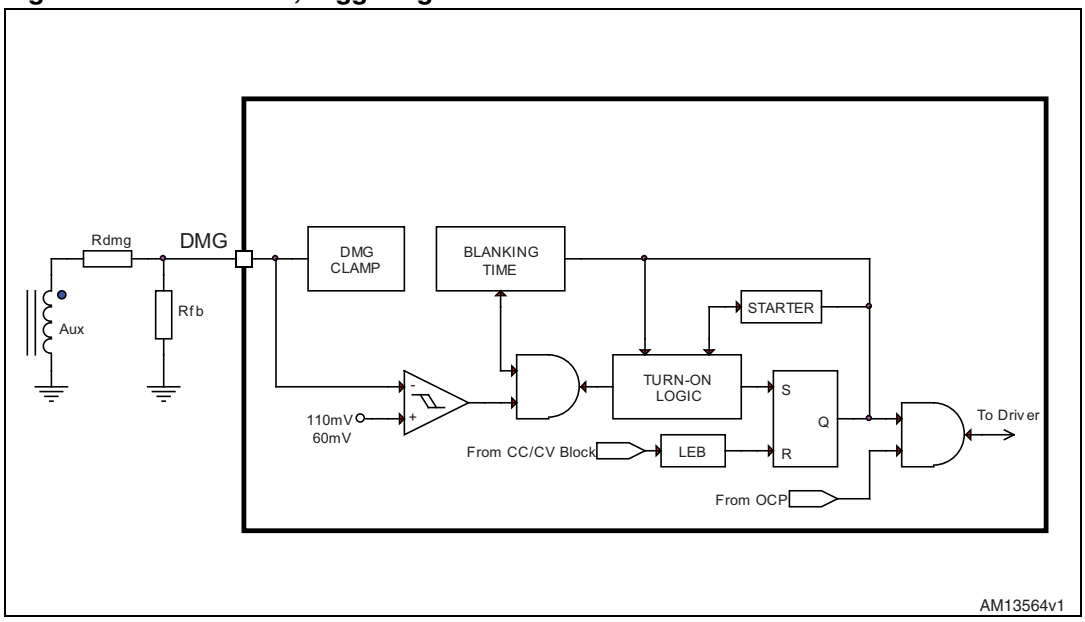


4.4 Secondary side demagnetization detection and triggering block

The demagnetization detection (DMG) and triggering blocks switch on the power MOSFET if a negative-going edge falling below 50 mV is applied to the DMG pin. To do so, the triggering block must be previously armed by a positive-going edge exceeding 100 mV.

This feature is used to detect transformer demagnetization for QR operation, where the signal for the DMG input is obtained from the transformer's auxiliary winding used also to supply the IC.

Figure 14. DMG block, triggering block



The triggering block is blanked after MOSFET's turn-off to prevent any negative-going edge that follows leakage inductance demagnetization from triggering the DMG circuit erroneously. This T_{BLANK} blanking time is dependent on the voltage on COMP pin: it is T_{BLANK}=30 µs for V_{COMP}=0.9 V, and decreases almost linearly down to T_{BLANK}=6 µs for V_{COMP}=1.3 V.

The voltage on the pin is both top and bottom limited by a double clamp, as illustrated in the internal diagram of the DMG block of *Figure 14*. The upper clamp is typically located at 3.3 V, while the lower clamp is located at -60 mV. The interface between the pin and the auxiliary winding will be a resistor divider. Its resistance ratio as well as the individual resistance values will be properly chosen (see *Section 4.6*, *4.7* and *4.11*).

Please note that the maximum IDMG sunk/sourced current has to not exceed ±2 mA (AMR) in all the Vin range conditions. No capacitor is allowed between DMG pin and the auxiliary transformer.

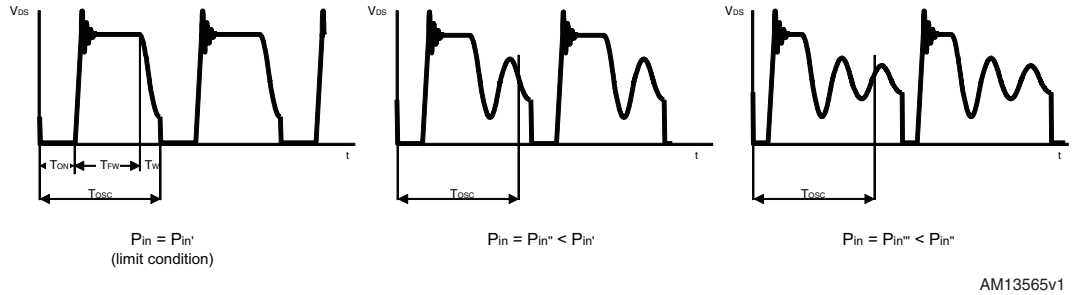
The switching frequency is top-limited below 166 kHz, as the converter's operating frequency tends to increase excessively at light load and high input voltage.

A Starter block is also used to start-up the system, that is, to turn on the MOSFET during converter power-up, when no or a too small signal is available on the DMG pin. The starter frequency is 2 kHz if COMP pin is below burst mode threshold, i.e. 1 V, while it becomes 8 kHz if this voltage exceed this value.

After the first few cycles initiated by the starter, as the voltage developed across the auxiliary winding becomes large enough to arm the DMG circuit, MOSFET's turn-on will start to be locked to transformer demagnetization, hence setting up QR operation. The starter is activated also when the IC is in Constant Current regulation and the output voltage is not high enough to allow the DMG triggering.

If the demagnetization completes - hence a negative-going edge appears on the DMG pin - after a time exceeding time T_{BLANK} from the previous turn-on, the MOSFET will be turned on again, with some delay to ensure minimum voltage at turn-on. If, instead, the negative-going edge appears before T_{BLANK} has elapsed, it will be ignored and only the first negative-going edge after T_{BLANK} will turn-on the MOSFET. In this way one or more drain ringing cycles will be skipped ("valley-skipping mode", *Figure 15*) and the switching frequency will be prevented from exceeding $1/T_{BLANK}$.

Figure 15. Drain ringing cycle skipping as the load is progressively reduced



Note: That when the system operates in valley skipping-mode, uneven switching cycles may be observed under some line/load conditions, due to the fact that the OFF-time of the MOSFET is allowed to change with discrete steps of one ringing cycle, while the OFF-time needed for cycle-by-cycle energy balance may fall in between. Thus one or more longer switching cycles will be compensated by one or more shorter cycles and vice versa. However, this mechanism is absolutely normal and there is no appreciable effect on the performance of the converter or on its output voltage.

4.5 Constant current operation

Figure 16 presents the principle used for controlling the average output current of the flyback converter.

The voltage of the auxiliary winding is used by the demagnetization block to generate the control signal for the internal MOSFET switch Q. A resistor R in series with it absorbs a current equal to $V_{ILED/R}$, where V_{ILED} is the voltage developed across the capacitor C_{LED} capacitor.

The flip-flop's output is high as long as the transformer delivers current on secondary side. This is shown in *Figure 17*.

Figure 16. Current control principle

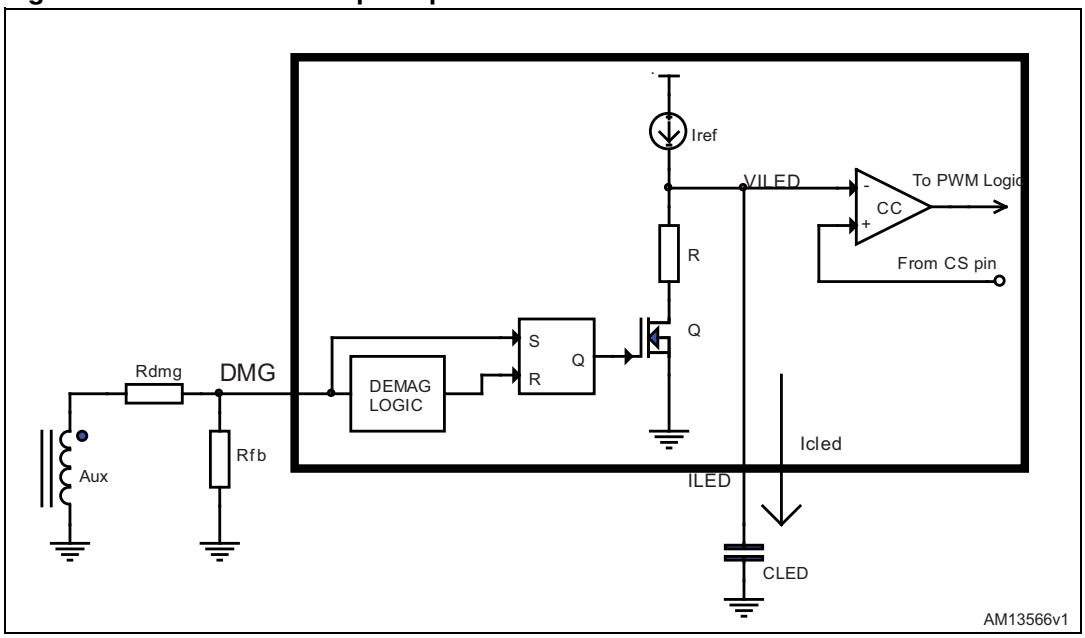
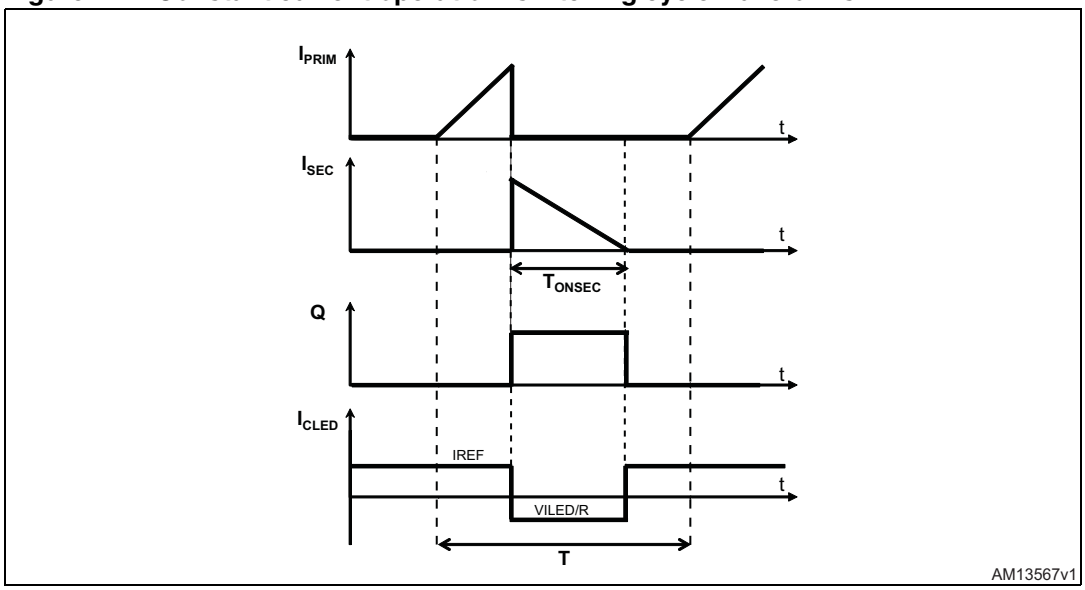


Figure 17. Constant current operation: switching cycle waveforms



The capacitor C_{LED} has to be chosen so that its voltage V_{ILED} can be considered as a constant. Since it is charged and discharged by currents in the range of some ten µA (IREF=20 µA typ.) at the switching frequency rate, a capacitance value in the range 4.7-10 nF is suited for switching frequencies in the ten kHz. When high power factor schematic is implemented, a higher capacitor value should be used (i.e. 1 µF-10 µF).

The average output current I_{OUT} can be expressed as:

Equation 1

$$I_{OUT} = \frac{I_{SEC}}{2} * \left(\frac{T_{ONSEC}}{T}\right)$$

Where I_{SEC} is the secondary peak current, T_{ONSEC} is the conduction time of the secondary side and T is the switching period.

Taking into account the transformer ratio N between primary and secondary side, ISEC can also be expressed as a function of the primary peak current I_{PRIM}:

Equation 2

$$I_{SEC} = N * I_{PRIM}$$

As in steady state the average current I_{CLED}:

Equation 3

$$[I_{REF} * (T - T_{ONSEC})] + \left[\left(I_{REF} - \frac{V_{ILED}}{R}\right) * T_{ONSEC}\right] = 0$$

Which can be solved for V_{ILED}:

Equation 4

$$V_{ILED} = (R * I_{REF}) * \frac{T}{T_{ONSEC}} = V_{CLED} * \frac{T}{T_{ONSEC}}$$

where V_{CLED}=R* I_{REF} and it is internally defined (0.2 V typical - see *Table 5: Electrical characteristics*).

The V_{ILED} pin voltage is internally compared with the CS pin voltage (constant current comparator):

Equation 5

$$V_{CS} = R_{SENSE} * I_{PRIM} = R_{SENSE} * \frac{I_{SEC}}{N}$$

Combining (1), (2) (4) and (5) the average output current results:

Equation 6

$$I_{OUT} = \frac{N}{2} * \frac{V_{CLED}}{R_{SENSE}}$$

This formula shows that the average output current I_{OUT} does not depend anymore on the input voltage V_{IN} or the output voltage V_{OUT}, neither on transformer inductance values. The external parameters defining the output current are the transformer ratio n and the sense resistor R_{SENSE}.

The previous formula (Equation *6*) is valid for both standard and high power factor implementation.

4.6 Constant voltage operation

The IC is specifically designed to work in primary regulation and the output voltage is sensed through a voltage partition of the auxiliary winding, just before the auxiliary rectifier diode.

Figure 18 shows the internal schematic of the constant voltage mode and the external connections.

Due to the parasitic wires resistance, the auxiliary voltage is representative of the output just when the secondary current becomes zero. For this purpose, the signal on DMG pin is sampled-and-held at the end of transformer's demagnetization to get an accurate image of the output voltage and it is compared with the error amplifier internal reference voltage V_{REF} (2.51 V typ - see *Table 5: Electrical characteristics*).

During the MOSFET's OFF-time the leakage inductance resonates with the drain capacitance and a damped oscillation is superimposed on the reflected voltage. The S/H logic is able to discriminate such oscillations from the real transformer's demagnetization.

When the DMG logic detects the transformer's demagnetization, the sampling process stops, the information is frozen and compared with the error amplifier internal reference.

The internal error amplifier is a transconductance type and delivers an output current proportional to the voltage unbalance of the two outputs: the output generates the control voltage that is compared with the voltage across the sense resistor, thus modulating the cycle-by-cycle peak drain current.

The COMP pin is used for the frequency compensation: usually, an RC network, which stabilizes the overall voltage control loop, is connected between this pin and ground.

As a result, the output voltage V_{OUT} at zero-load (i.e. no led on the led driver output) can be selected trough the R_{FB} resistor in according to the following formula:

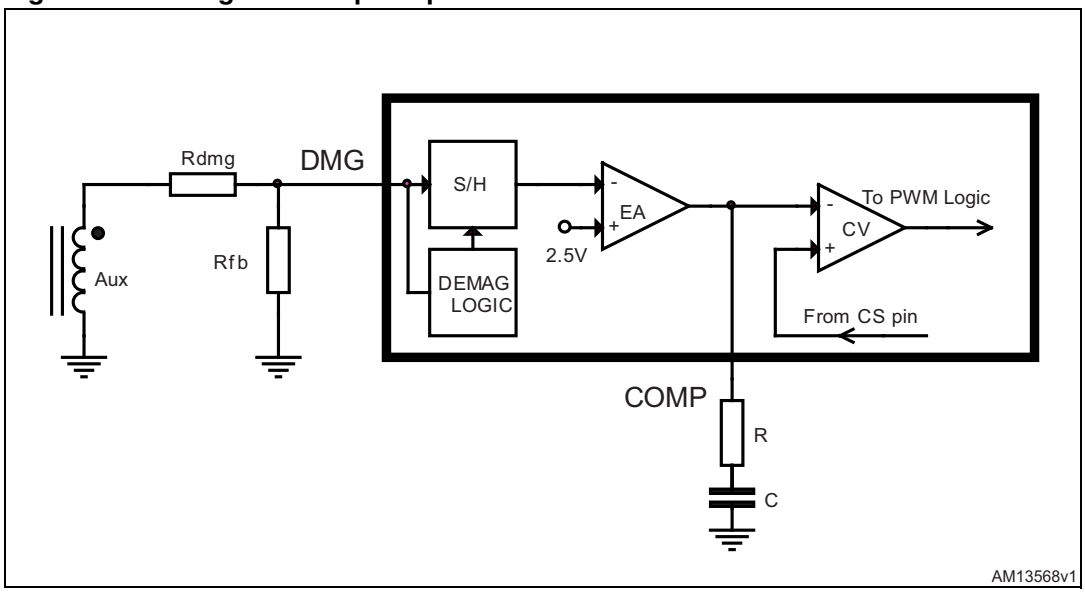
Equation 7

$$R_{FB} = R_{DMG} * \left[\frac{V_{REF}}{\left(\frac{N_{AUX}}{N_{SEC}} * V_{OUT} \right) - V_{REF}} \right]$$

Where N_{AUX} and N_{SEC} are the auxiliary and secondary turn's number respectively.

The R_{DMG} resistor value can be defined depending on the application parameters (see *Section 4.7: Voltage feed-forward block*).

Figure 18. Voltage control principle: internal schematic



4.7 Voltage feed-forward block

The current control structure uses the V_{CLED} voltage to define the output current, according to equation *6* on *Section 4.5*. Actually, the constant current comparator will be affected by an internal propagation delay T_D, which will switch off the MOSFET with a peak current than higher the foreseen value.

This current overshoot will be equal to:

Equation 8

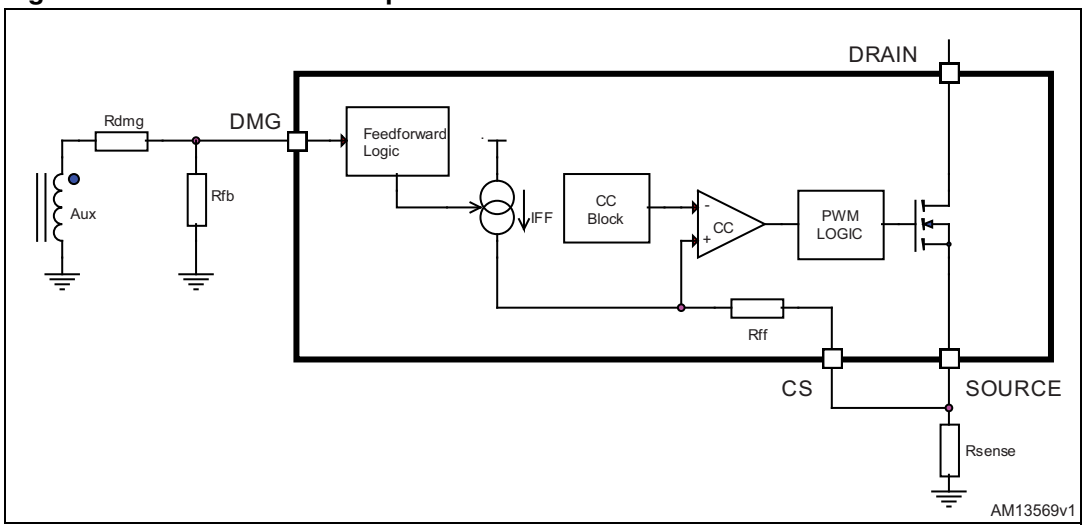
$$\Delta I_{PRIM} = \frac{V_{IN} * T_D}{L_P}$$

The previous terms introduce a small error on the calculated average output current set-point, depending on the input voltage.

The HVLED807PF implements a line feed-forward function, which solves the issue by introducing an input voltage dependent offset on the current sense signal, in order to adjust the cycle-by-cycle current limitation.

The internal schematic is shown in *Figure 19*.

Figure 19. Feed-forward compensation: internal schematic



During MOSFET's ON-time the current sourced from DMG pin is mirrored inside the "Feed-forward Logic" block in order to provide a feed-forward current, I_{FF}.

Such "feed-forward current" is proportional to the input voltage according to the formula:

Equation 9

$$I_{FF} = \frac{V_{IN} * \frac{N_{AUX}}{N_{PRIM}}}{R_{dmg}} = \frac{V_{IN}}{m * R_{dmg}}$$

Where m is the primary-to-auxiliary turns ratio.

According to the schematic, the voltage on the non-inverting comparator will be:

Equation 10

$$V(-) = (R_{SENSE} * I_D) + [I_{FF} * (R_{FF} + R_{SENSE})]$$

The offset introduced by feed-forward compensation will be:

Equation 11

$$V_{OFFSET} = \frac{V_{IN}}{m * R_{dmg}} * (R_{FF} + R_{SENSE})$$

As $R_{FF} >> R_{SENS}E$, the previous one can be simplified as:

Equation 12

$$V_{OFFSET} = \frac{V_{IN}}{m * R_{dmg}} * R_{FF}$$

This offset is proportional to VIN and it is used to compensate the current overshoot, according to the following formula:

Equation 13

$$\frac{V_{IN} * T_D}{L_P} * R_{SENSE} = \frac{V_{IN}}{m * R_{dmg}} * R_{FF}$$

Finally, the Rdmg resistor can be calculated as follows:

Equation 14

$$R_{dmg} = \frac{N_{AUX}}{N_{PRIM}} * \frac{L_P * R_{FF}}{T_D * R_{SENSE}}$$

In this case the peak drain current does not depend on input voltage anymore, and as a consequence the average output current I_{OUT} do not depend from the V_{IN} input voltage.

When high power factor is implemented (see *Section 4.11*), the feed-forward current has to be minimized because the line regulation is assured by the external offset circuitry (see *Figure 1: Application circuit for high power factor LED driver - single range input*).

The maximum value is limited by the minimum Idmg internal current needed to guarantee the correct functionality of the internal circuitry:

Equation 15

$$R_{dmg}{}^{MAX} = \frac{N_{AUX}}{N_{PRIM}} * \frac{Vin\_\min(ac) * \sqrt{2}}{100uA}$$

4.8 Burst-mode operation at no load or very light load

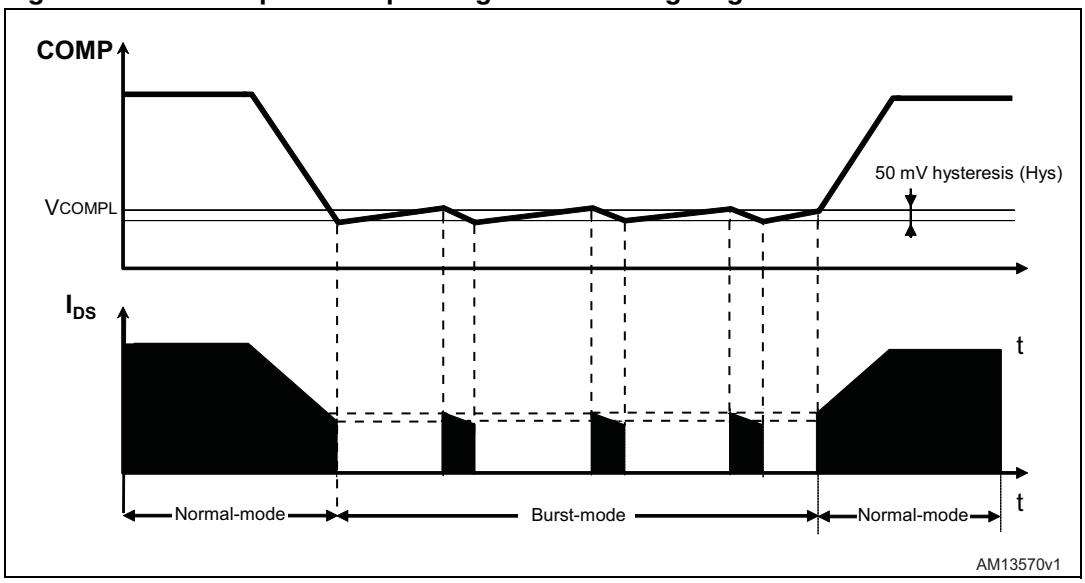
When the voltage at the COMP pin falls 65 mV is below the internally fixed threshold V_{COMPBM}, the IC is disabled with the MOSFET kept in OFF state and its consumption reduced at a lower value to minimize VCC capacitor discharge.

In this condition the converter operates in burst-mode (one pulse train every T_{START}=500 µs), with minimum energy transfer.

As a result of the energy delivery stop, the output voltage decreases: after 500 µs the controller switches-on the MOSFET again and the sampled voltage on the DMG pin is compared with the internal reference V_{REF}. If the voltage on the EA output, as a result of the comparison, exceeds the VCOMPL threshold, the device restarts switching, otherwise it stays OFF for another 500 µs period.

In this way the converter will work in burst-mode with a nearly constant peak current defined by the internal disable level. A load decrease will then cause a frequency reduction, which can go down even to few hundred hertz, thus minimizing all frequency-related losses and making it easier to comply with energy saving regulations. This kind of operation, shown in the timing diagrams of *Figure 20* along with the others previously described, is noise-free since the peak current is low.

Figure 20. Load-dependent operating modes: timing diagrams



4.9 Soft-start and starter block

The soft start feature is automatically implemented by the constant current block, as the primary peak current will be limited from the voltage on the C_{LED} capacitor.

During start-up, as the output voltage is zero, the IC will start in constant current (CC) mode with no high peak current operations. In this way the voltage on the output capacitor will increase slowly and the soft-start feature will be ensured.

Actually the C_{LED} value is not important to define the soft-start time, as its duration depends on others circuit parameters, like transformer ratio, sense resistor, output capacitors and load. The user will define the best appropriate value by experiments.

4.10 Hiccup mode OCP

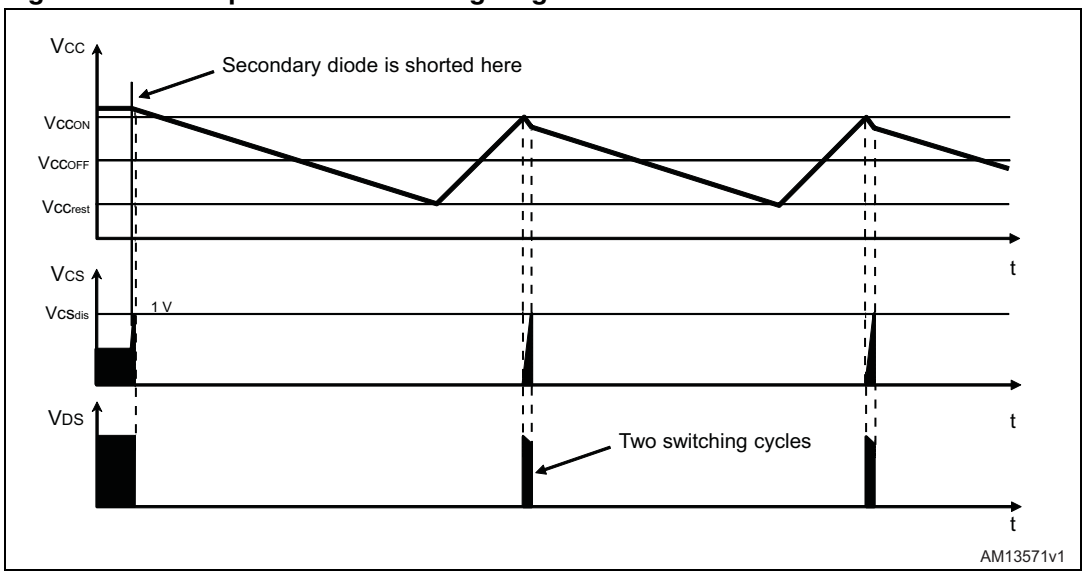
The device is also protected against short-circuit of the secondary rectifier, short-circuit on the secondary winding or a hard-saturated flyback transformer. An internal comparator monitors continuously the voltage on CS pin and activates a protection circuitry if this voltage exceeds an internally fixed threshold VCSdis (1 V typ. - see *Table 5: Electrical characteristics*).

To distinguish an actual malfunction from a disturbance (e.g. induced during ESD tests), the first time the comparator is tripped the protection circuit enters a "warning state". If in the subsequent switching cycle the comparator is not tripped, a temporary disturbance is assumed and the protection logic will be reset in its idle state; if the comparator will be tripped again a real malfunction is assumed and the device will be stopped.

This condition is latched as long as the device is supplied. While it is disabled, however, no energy is coming from the self-supply circuit; hence the voltage on the V_{CC} capacitor will decay and cross the UVLO threshold after some time, which clears the latch. The internal start-up generator is still off, then the VCC voltage still needs to go below its restart voltage before the VCC capacitor is charged again and the device restarted.

Ultimately, this will result in a low-frequency intermittent operation (hiccup-mode operation), with very low stress on the power circuit. This special condition is illustrated in the timing diagram of *Figure 21*.

Figure 21. Hiccup-mode OCP: timing diagram



4.11 High Power Factor implementation

Referring to the principle application schematic on *Figure 1*, two contributions are added on the CS pin in order to implement the high power factor capability (trough R_{PF} resistor) and keeping a good line-regulation (trough R_{OS} resistor). The application schematic on *Figure 1* is intended for a single range input voltage. For wide range application a different reference schematic can be used; refer to the dedicated application note for further details.

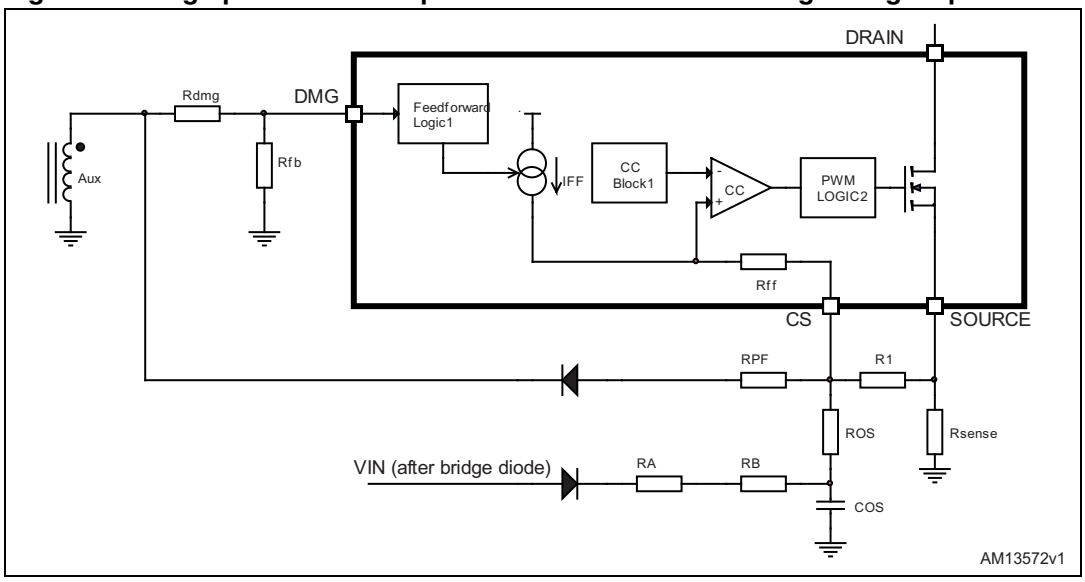
Through the R_{PF} resistor a contribution proportional to the input voltage is added on the CS pin: as a consequence the input current is proportional to the input voltage during the line period, implementing a high power factor correction. The contribution proportional to the input voltage is generated using the auxiliary winding, as a consequence a diode in series to the R_{PF} resistor is needed.

Through the ROS resistor a positive contribution proportional to the average value of the input voltage is added on the CS pin in order to keep a good line-regulation.

The voltage contribution proportional to the average value of the input voltage is generated trough the low pass filter R_A/R_B resistor and C_{OS} capacitor. A diode in series to the R_A/R_B resistor is suggested to avoid the discharge of C_{OS} capacitor in any condition.

The R1 resistor between CS and SOURCE pin is needed to add on the CS pin also the contribution proportional the output current trough the R_{SENSE} resistor.

Figure 22. High power factor implementation connection - single range input



The components selection flow starts from Rdmg resistor: this resistor has to be selected in order to minimize the internal feed-forward effect.

The maximum selectable value is limited is by the minimum internal current circuitry I_{DMG} needed to guarantee the correct functionality of the internal circuitry:

Equation 16

$$R_{dmg}{}^{MAX} = \frac{N_{AUX}}{N_{PRIM}} * \frac{V_{IN\_MIN} * \sqrt{2}}{100uA}$$

where N_{AUX} and N_{PRIM} are the auxiliary and primary turn's number respectively and V_{IN_MIN} is the minimum rms input voltage of the application (i.e. 88 V for 110 V_{ac} or 175 V for 230 V_{ac} range).

The RFB resistor defines the V_{OUT} output voltage value in the open circuit condition (no-load condition, i.e. no led on the output of led driver) and it can be selected using the following relationship:

Equation 17

$$R_{FB} = R_{DMG} * \left[\frac{V_{REF}}{\left(\frac{N_{AUX}}{N_{SEC}} * V_{OUT} \right) - V_{REF}} \right]$$

where N_{AUX} and N_{SEC} are the auxiliary and secondary turn's number respectively and V_{REF} is the internal reference voltage (V_{REF} =2.51 V typ - see *Table 5: Electrical characteristics*).

The R_1 resistor is typically selected in the range of 500 Ω-1.5 kΩ in order to minimize the internal feed-forward effect and to minimize the power dissipation on the R_A/R_B resistor offset circuitry.

The R_A, R_B, R_{OS} resistors are selected to add a positive offset on CS pin in order to keep a good line regulation over the input voltage range and cab be selected using the following relationship:

Equation 18

$$R_{OS} = R_1 * \left\{ \left[\frac{V_{OS\_TYP}}{V_{CLED}} * \left[\frac{N_{SEC}}{V_{OUT} * N_{PRIM}} * \sqrt{2 * P_{OUT} * L_P * F_{SW}} \right] \right] - 1 \right\}$$

Where V_{OS_TYP} is the desired voltage across C_{OS} capacitor applying the V_{IN_TYP} typical input voltage (i.e. VIN_TYP=220 V for 176/264 Vac input range); F_{sw} is the switching frequency and can be estimated using the following formula, where f_T and f_R are the transition and resonant frequency respectively:

Equation 19

$$F_{SW} = \left[\frac{2 * f_T}{1 + \frac{f_T}{f_R} + \sqrt{1 + 2 * \frac{f_T}{f_R}}} \right]$$

Equation 20

$$f_T = \frac{1}{2 * \frac{P_{OUT}}{\eta} * L_P * \left[\frac{1}{V_{IN\_TYP} * \sqrt{2}} + \frac{N_{SEC}}{V_{OUT} * N_{PRIM}} \right]^2}$$

Equation 21

$$f_R = \frac{1}{2 * \pi * \sqrt{L_P * C_D}}$$

where CD is the total equivalent capacitor afferent at the drain node.

Based on the desired voltage across C_{OS} capacitor and calculated R_{OS} resistor, then the sum of R_A and R_B can then calculated as a results of partitioning divider:

Equation 22

$$R_A + R_B = R_{OS} * \frac{\left[\left(V_{IN\_TYP} * \sqrt{2} * \frac{2}{\pi} \right) - V_{OS\_TYP} \right]}{V_{OS-TYP}}$$

Using the previous R_{OS} resistor value the R_{PF} resistor can be estimated using the following formula:

Equation 23

$$R_{PF} = \frac{\left[V_{IN\_TYP} * \sqrt{2} * \frac{N_{AUX}}{N_{PRIM}} \right]}{\left[\left(\left(V_{IN\_TYP} * \sqrt{2} * \frac{N_{AUX}}{N_{PRIM}} \right) * R_{OS} \right) + \left(V_{OS\_TYP} * R_{DMG} \right) \right]} * \left(R_{OS} * R_{DMG} \right)$$

Finally the current sense resistor R_{SENSE} can be estimated in order to select the desiderated average output current value:

Equation 24

$$R_{SENSE} = \frac{N_{PRIM}}{N_{SEC}} * \frac{1}{2} * \frac{V_{CLED}}{I_{OUT}}$$

where V_{CLED} is internally defined (0.2 V typical - see *Table 5: Electrical characteristics*).

System design tips

Starting from the estimated value using the previous formulas, further fine-tuning on the real led driver board could be necessary and it can be easily done considering that:

- Decreasing/increasing the R_{PF} resistor value, the power factor effect increase/decrease
- Decreasing/increasing the R_{OS} resistor value, the line-regulation effect increase/decrease
- Decreasing/increasing the R_{OS} resistor value, the R_A+R_B resistors value should be increase/decrease to keep the desiderated voltage across the C_{OS} capacitor (Equation *22*).
- Decreasing/increasing the R_{SENSE} resistor value the average output current increase/decrease (Equation *24*).

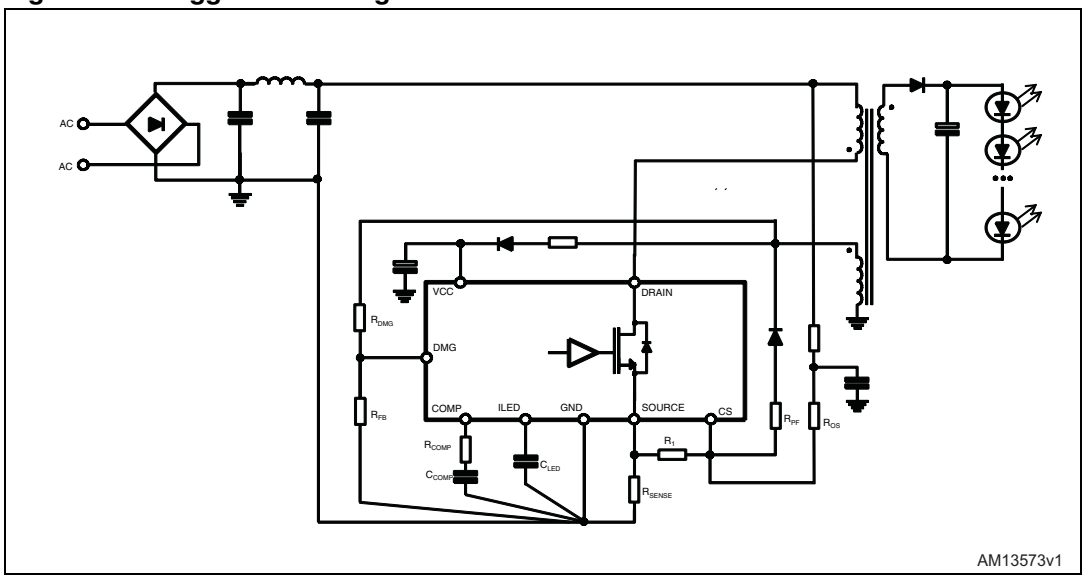
4.12 Layout recommendations

A proper printed circuit board layout is essential for correct operation of any switch-mode converter and this is true for the HVLED815PF as well. Careful component placing, correct traces routing, appropriate traces widths and compliance with isolation distances are the major issues.

In particular:

- Current sense resistor (R_{SENSE}) should be connected as close as possible to the SOURCE pin, maintaining the trace for the GND as short as possible.
- Resistor connected on CS pin (R_{OS}, R_{PF}, R_1) should be connected as close as possible to the pin.
- Compensation network (R_{COMP}, C_{COMP}) should be connected as close as possible to the COMP pin, maintaining the trace for the GND as short as possible.
- Signal ground should be routed separately from power ground, as well from the sense resistor trace.
- DMG partition resistors (R_{DMG}, R_{FB}) should be connected as close as possible to the DMG pin, minimizing the equivalent parasitic capacitor on DMG pin.

Figure 23. Suggested routing for the led driver



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 24. SO16N mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
k	0		8°
ccc			0.10

Figure 25. SO16N drawing

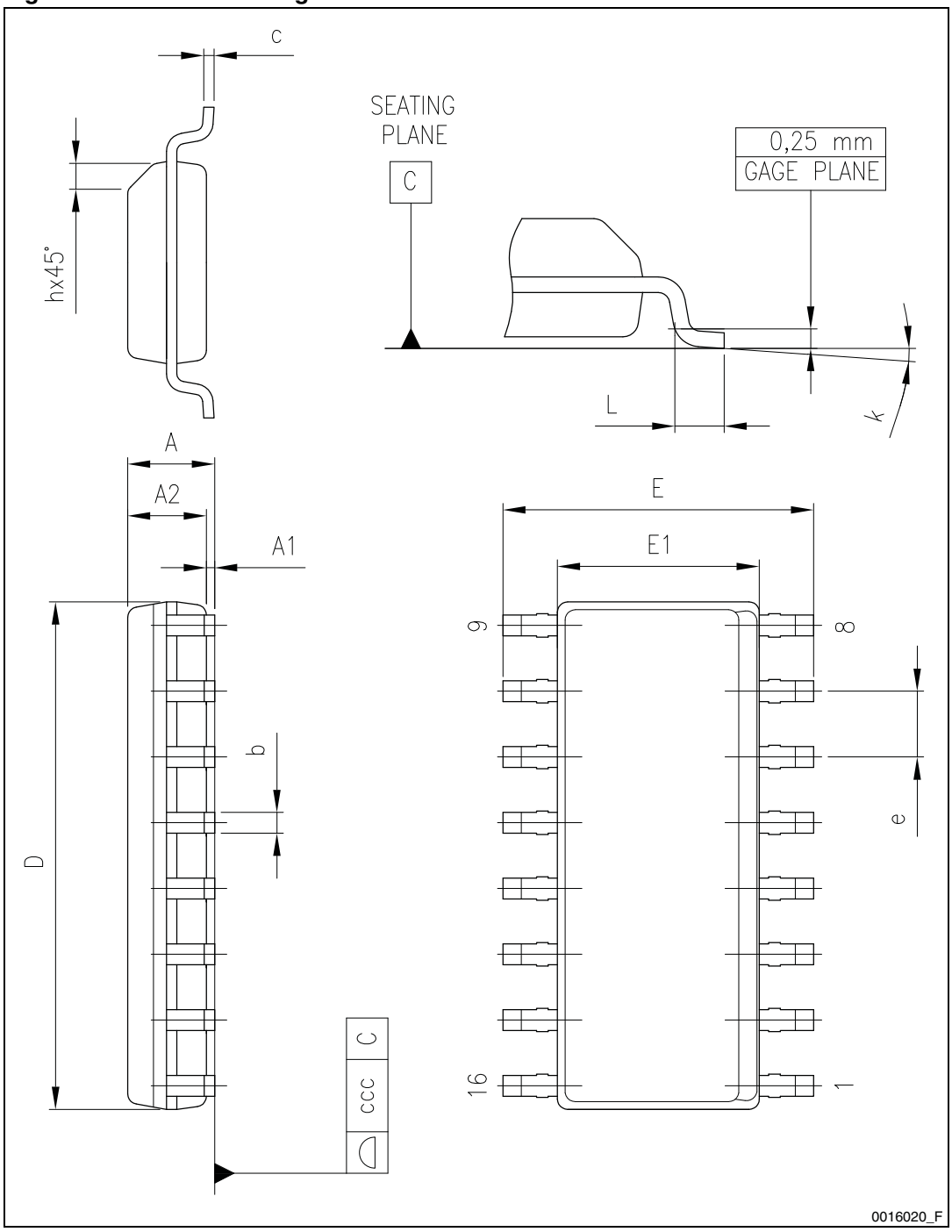
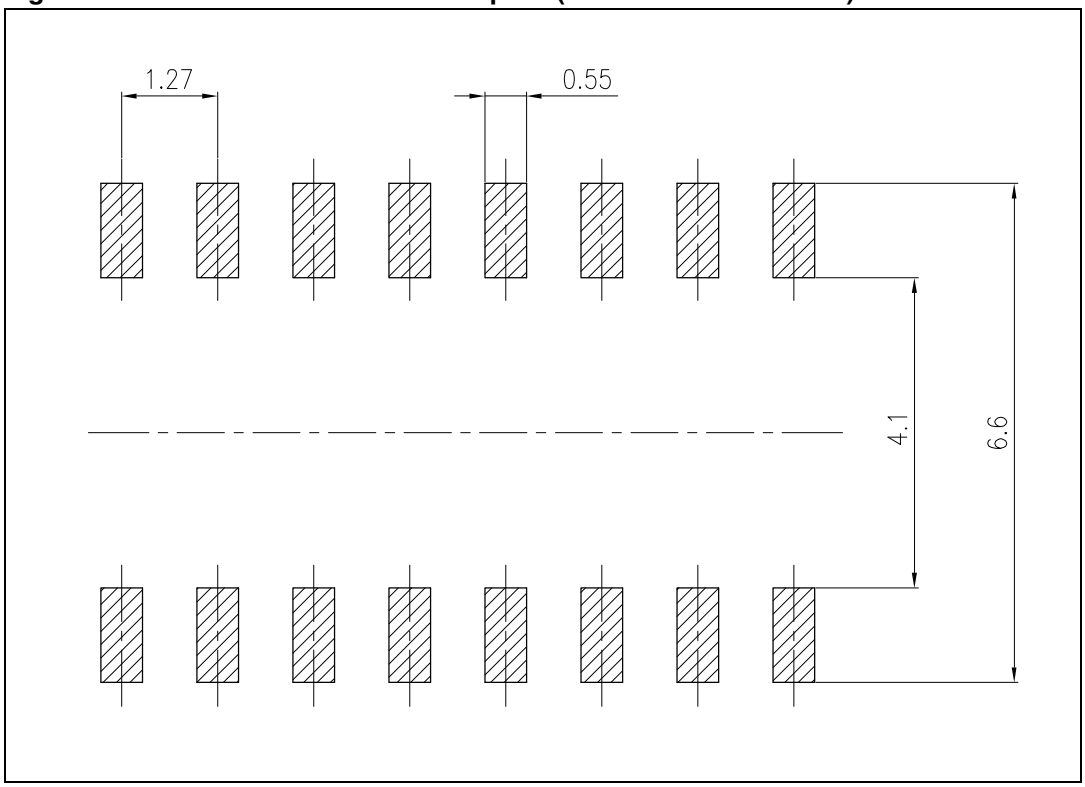


Figure 26. SO16N recommended footprint (dimensions are in mm)



6 Revision history

Table 6. Document revision history

Date	Revision	Changes
26-Jul-2012	1	Initial release.
29-Aug-2012	2	Added *Table 2: Pin description on page 7*.
23-Oct-2012	3	Modified T_J value on *Table 3: Thermal data*. Updated T_J value in note 2 (below *Table 5: Electrical characteristics*). Minor text changes.
27-Nov-2012	4	Updated $R_{DS(on)}$ value on *Table 5: Electrical characteristics*.
01-Feb-2013	5	Added sections from *4.1* to *4.12*. Modified *Figure 1: Application circuit for high power factor LED driver - single range input* and *Figure 2: Application circuit for standard LED driver*.

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