NTP4302, NTB4302

Power MOSFET
74 Amps, 30 Volts

N−Channel TO−220 & D^{2}PAK

ON Semiconductor®

http://onsemi.com

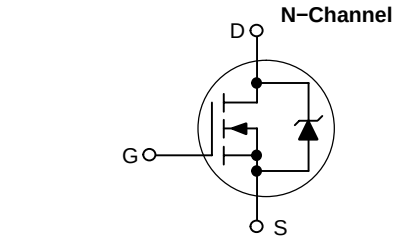
V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
30 V	9.3 mΩ @ 10 V	74 A

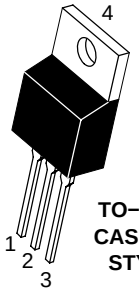
Features

- Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- I_{DSS} Specified at Elevated Temperature
- Pb−Free Packages are Available

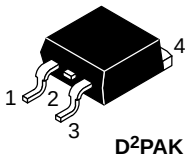
Typical Applications

- DC−DC Converters
- Low Voltage Motor Control
- Power Management in Portable and Battery Powered Products: Ie: Computers, Printers, Cellular and Cordless Telephones, and PCMCIA Cards





TO−220AB
CASE 221A
STYLE 5



D^{2}PAK
CASE 418AA
STYLE 2

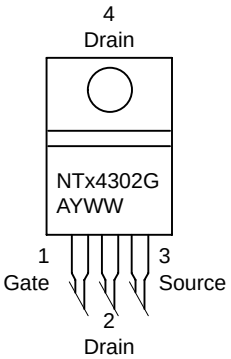
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

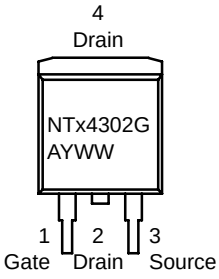
Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	30	Vdc
Drain−to−Gate Voltage (R_{GS} = 10 MΩ)	V_{DGR}	30	Vdc
Gate−to−Source Voltage − Continuous	V_{GS}	±20	Vdc
Drain Current − Continuous @ T_C = 25°C − Continuous @ T_C = 100°C − Single Pulse ($t_p \le 10$ μs)	 I_D I_D I_{DM}	 74 47 175	 Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.66	W W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 30 Vdc, V_{GS} = 10 Vdc, L = 5.0 mH $I_{L(pk)}$ = 17 A, V_{DS} = 30 Vdc, R_G = 25 Ω)	E_{AS}	722	mJ
Thermal Resistance − Junction−to−Case − Junction−to−Ambient (Note 1)	 $R_{\theta JC}$ $R_{\theta JA}$	 1.55 70	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8 in from case for 10 seconds	T_L	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 Board using minimum recommended Pad Size, (Cu Area 0.412 in^2).
2. Current limited by internal lead wires.

MARKING DIAGRAMS & PIN ASSIGNMENTS





NTx4302	= Device Code
x	= B or P
A	= Assembly Location
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (Note 3) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 30 −	 − 25	 − −	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 − −	 − −	 1.0 10	μAdc
Gate−Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	−	−	±100	nAdc
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage (Note 3) (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 −	 1.9 −3.8	 3.0 −	Vdc mV/°C
Static Drain−to−Source On−Resistance (Note 3) (V_{GS} = 10 Vdc, I_D = 37 Adc) (V_{GS} = 10 Vdc, I_D = 20 Adc) (V_{GS} = 4.5 Vdc, I_D = 10 Adc)		$R_{DS(on)}$	 −	 6.8 6.8 9.5	 9.3 9.3 12.5	mΩ
Forward Transconductance (Note 3) (V_{DS} = 10 Vdc, I_D = 20 Adc)		g_{FS}	−	40	−	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 24 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	−	2050	2400	pF
Output Capacitance		C_{oss}	−	640	800	
Transfer Capacitance		C_{rss}	−	225	310	
SWITCHING CHARACTERISTICS (Note 4)						
Turn−On Delay Time	(V_{DD} = 24 Vdc, I_D = 20 Adc, V_{GS} = 10 Vdc, R_G = 2.5 Ω) (Note 3)	$t_{d(on)}$	−	10	18	ns
Rise Time		t_r	−	22	35	
Turn−Off Delay Time		$t_{d(off)}$	−	45	75	
Fall Time		t_f	−	35	70	
Turn−On Delay Time	(V_{DD} = 24 Vdc, I_D = 10 Adc, V_{GS} = 4.5 Vdc, R_G = 2.5 Ω) (Note 3)	$t_{d(on)}$	−	18	−	ns
Rise Time		t_r	−	70	−	
Turn−Off Delay Time		$t_{d(off)}$	−	32	−	
Fall Time		t_f	−	30	−	
Gate Charge	(V_{DS} = 24 Vdc, I_D = 37 Adc, V_{GS} = 4.5 Vdc) (Note 3)	Q_T	−	28	−	nC
		Q_{gs}	−	7.5	−	
		Q_{gd}	−	19	−	
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage	(I_S = 20 Adc, V_{GS} = 0 Vdc) (Note 3) (I_S = 20 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	− −	0.90 0.75	1.3 −	Vdc
Reverse Recovery Time	(I_S = 20 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (Note 3)	t_{rr}	−	37	−	ns
		t_a	−	21	−	
		t_b	−	16	−	
Reverse Recovery Stored Charge		Q_{RR}	−	0.035	−	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

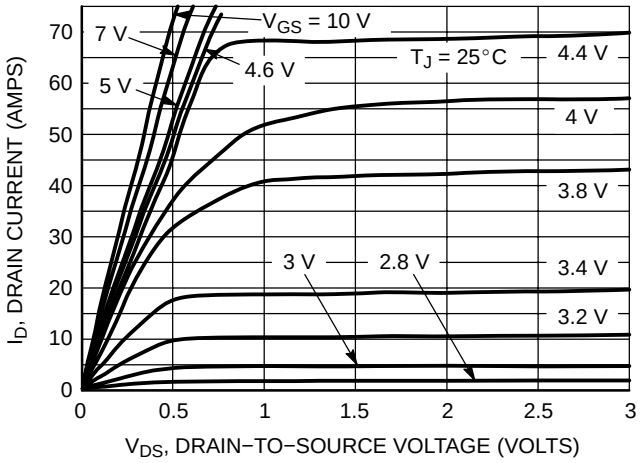


Figure 1. On−Region Characteristics

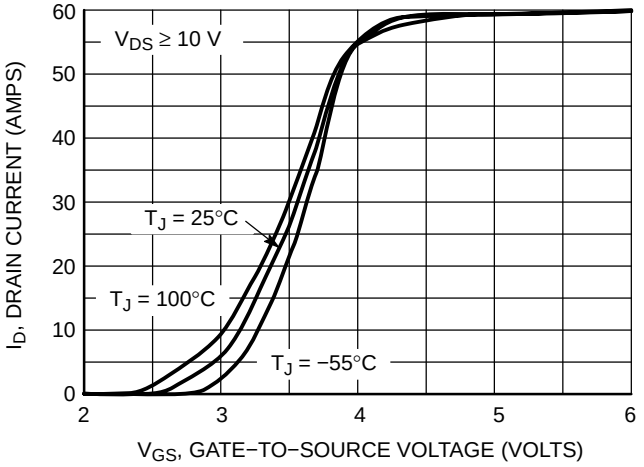


Figure 2. Transfer Characteristics

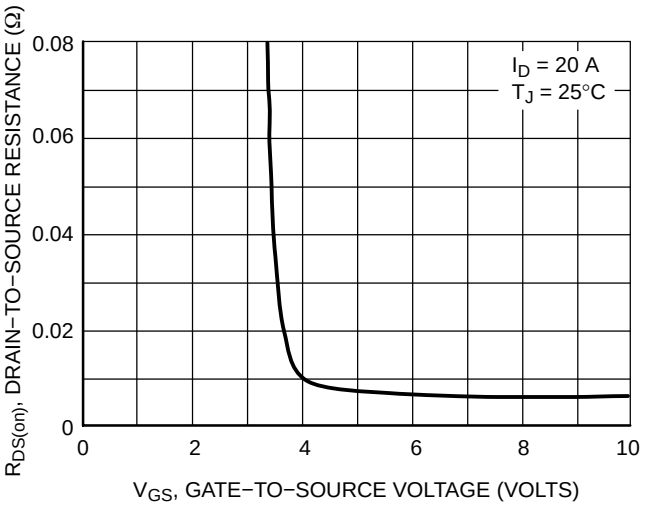


Figure 3. On−Resistance versus Gate−to−Source Voltage

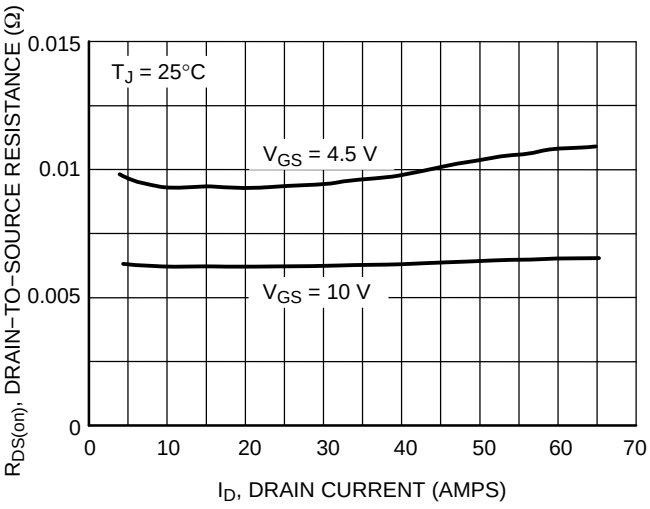


Figure 4. On−Resistance versus Drain Current and Gate Voltage

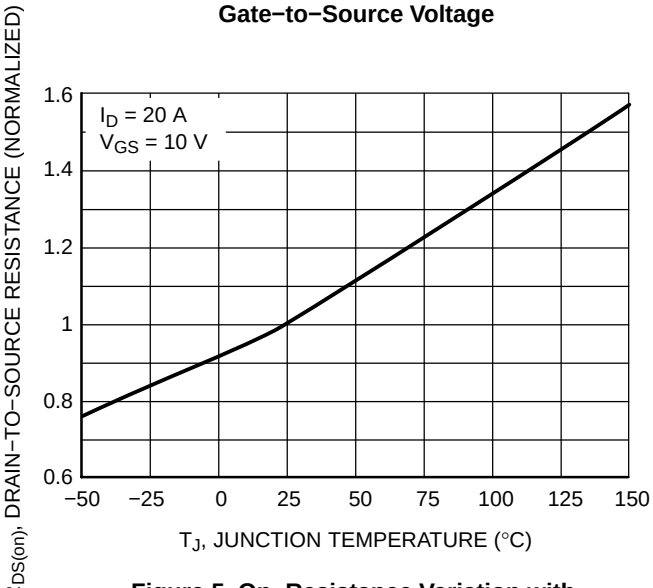


Figure 5. On−Resistance Variation with Temperature

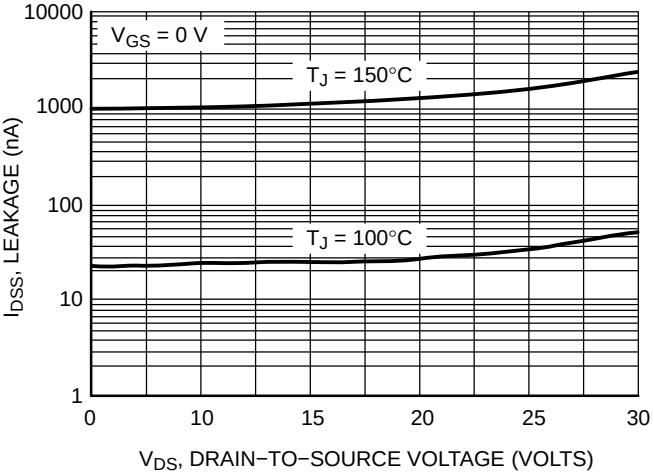


Figure 6. Drain−to−Source Leakage Current versus Voltage

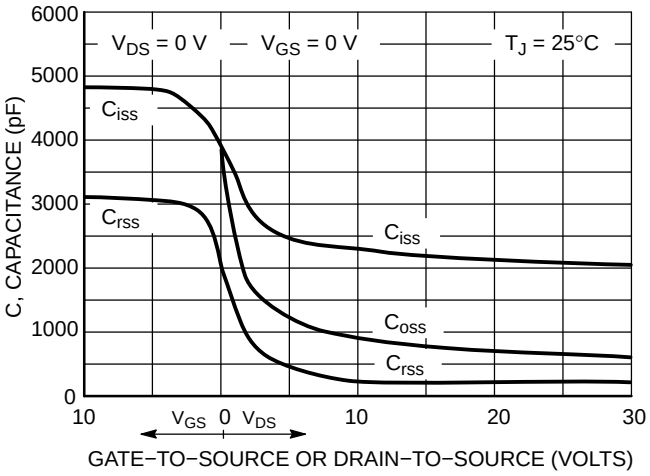


Figure 7. Capacitance Variation

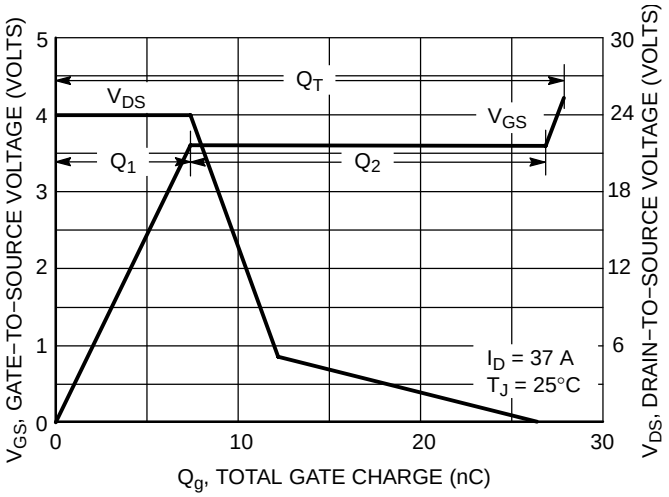


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

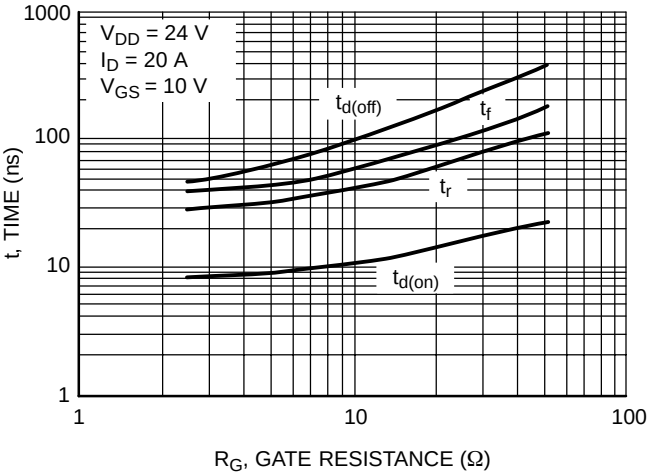


Figure 9. Resistive Switching Time Variations versus Gate Resistance

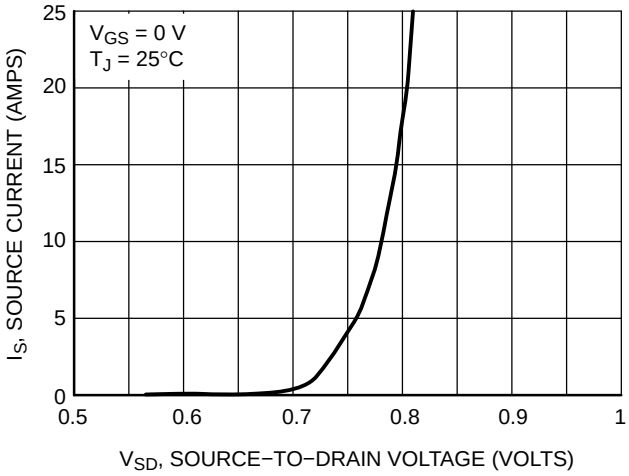


Figure 10. Diode Forward Voltage versus Current

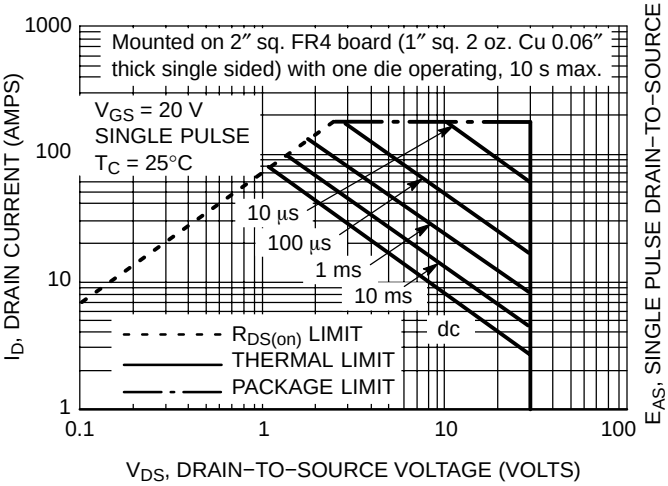


Figure 11. Maximum Rated Forward Biased Safe Operating Area

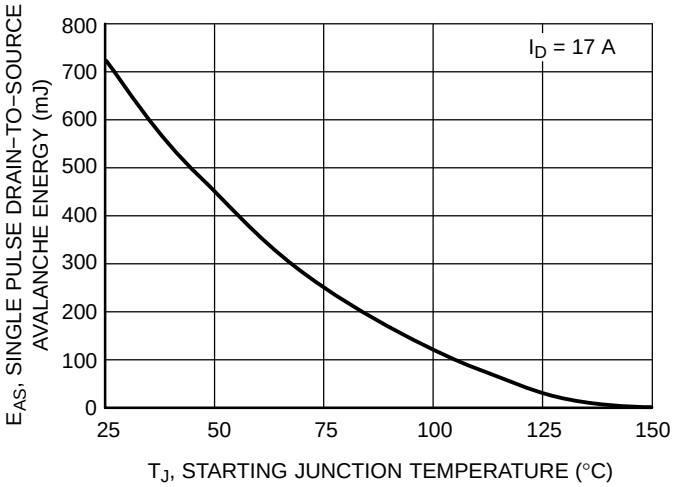


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

SAFE OPERATING AREA

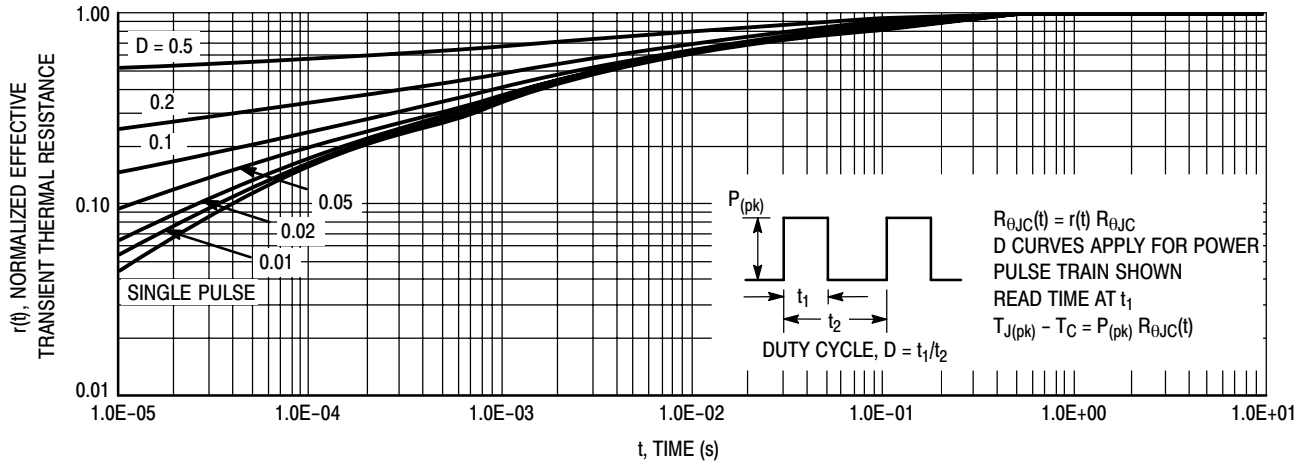


Figure 13. Thermal Response

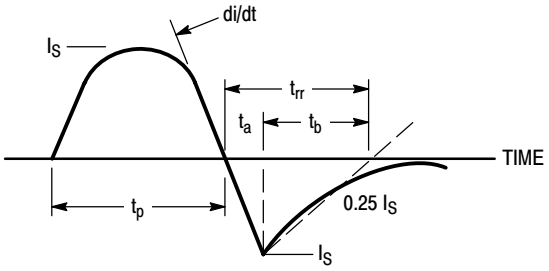


Figure 14. Diode Reverse Recovery Waveform

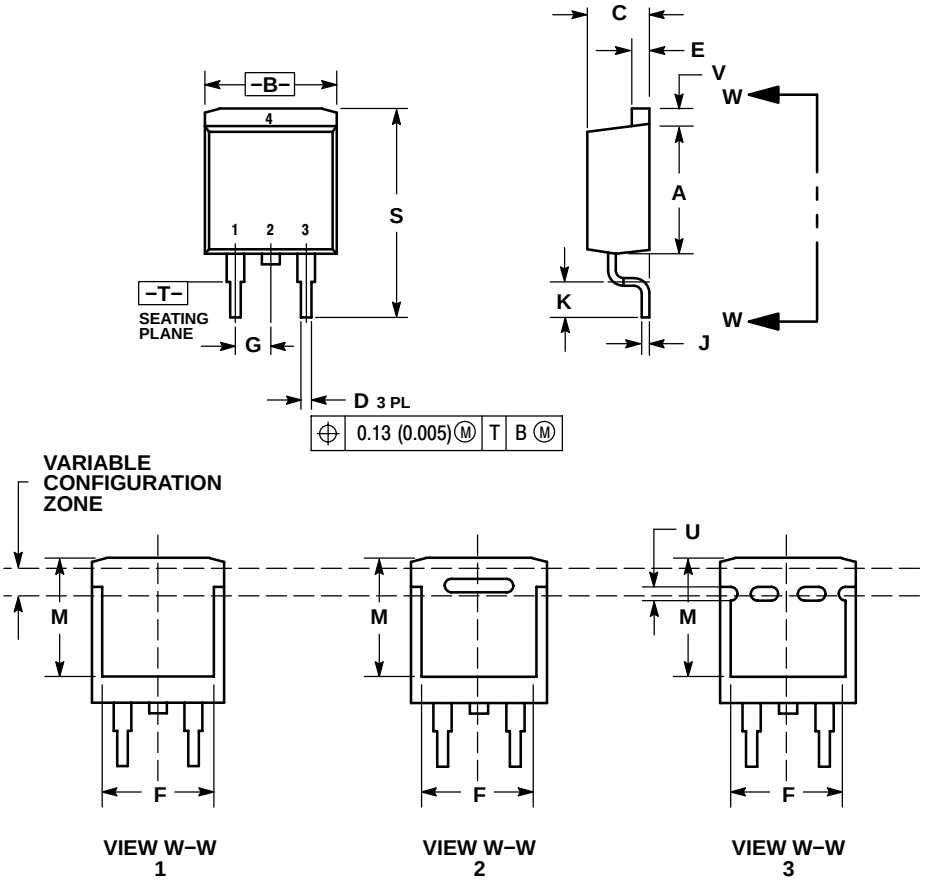
ORDERING INFORMATION

Device	Package	Shipping†
NTP4302	TO−220AB	50 Units / Rail
NTP4302G	TO−220AB (Pb−Free)	50 Units / Rail
NTB4302	D^{2}PAK	50 Units / Rail
NTB4302G	D^{2}PAK (Pb−Free)	50 Units / Rail
NTB4302T4	D^{2}PAK	800 / Tape & Reel
NTB4302T4G	D^{2}PAK (Pb−Free)	800 / Tape & Reel

†For information on tape and reel specifications,including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

D²PAK
CASE 418AA−01
ISSUE O

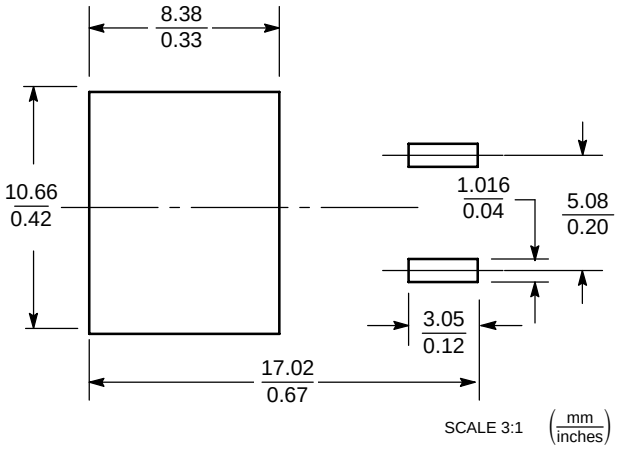


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.036	0.51	0.92
E	0.045	0.055	1.14	1.40
F	0.310	−−−	7.87	−−−
G	0.100 BSC		2.54 BSC	
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
M	0.280	−−−	7.11	−−−
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

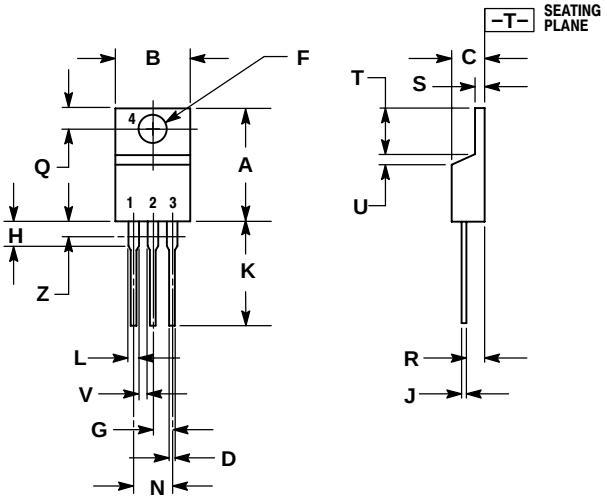
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TO−220
CASE 221A−09
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PUBLICATION ORDERING INFORMATION

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