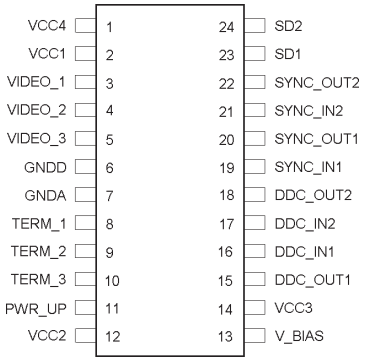
VGA PORT COMPANION CIRCUIT

Features

- 7 channels of ESD protection for all VGA port connector pins meeting IEC-61000-4-2 Level-4 ESD requirements (8KV contact discharge)
- Very low loading capacitance from ESD protection diodes on VIDEO lines, 4pF typical
- TTL to CMOS level-translating buffers with power down mode for HSYNC and VSYNC lines
- 75 Ω termination resistors for VIDEO lines (matched to 1% typ.)
- Bi-directional level shifting N-channel FETs provided for DDC_CLK & DDC_DATA channels
- Compact 24-pin QSOP package

Pin Diagram



24-PIN QSOP PACKAGE

Product Description

The PACVGA200 incorporates 7 channels of ESD protection for all signal lines commonly found in a VGA port. ESD protection is implemented with current steering diodes designed to safely handle the high surge currents encountered with IEC-1000-4-2 Level-4 ESD Protection (8KV contact discharge). When a channel is subjected to an electrostatic discharge, the ESD current pulse is diverted via the protection diodes into the positive supply rail or ground where it may be safely dissipated.

Separate positive supply rails are provided for the VIDEO, DDC and SYNC channels to facilitate interfacing with low voltage Video Controller ICs and provide design flexibility in multi-supply-voltage environments.

Two non-inverting drivers provide buffering for the HSYNC and VSYNC signals from the Video Controller IC (SYNC1, SYNC2). These buffers accept TTL input levels and convert them to CMOS output levels that swing between Ground and V_{CC4}. These drivers have nominal 60Ω output impedance to match the characteristic impedance of the HSYNC & VSYNC lines of the video cables typically used in PC applications.

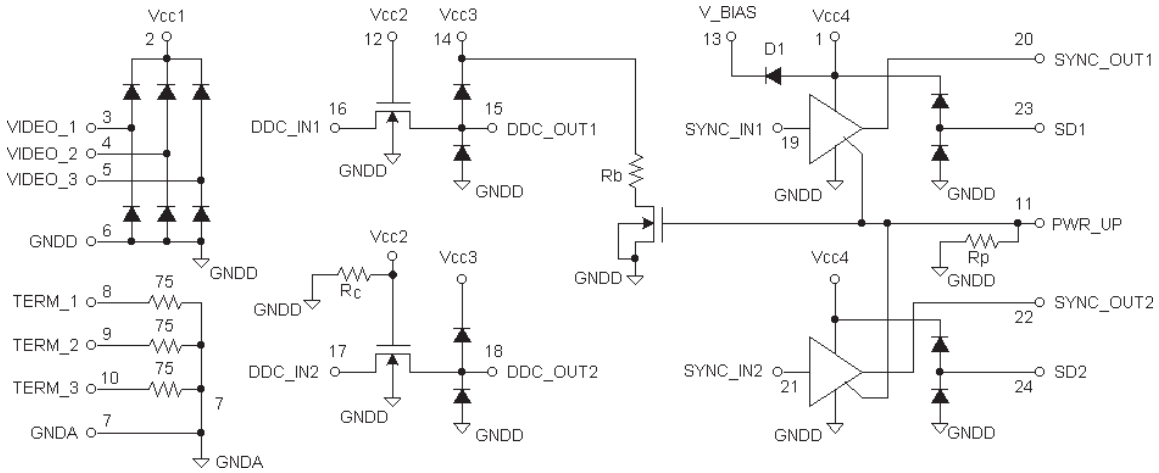
Two N-channel FETs provide the level shifting function required when the DDC controller is operated at a lower supply voltage than the monitor.

Three 75Ω termination resistors suitable for terminating the video signals from the video DAC are also provided. These resistors have separate input pins to allow insertion of additional EMI filtering, if required, between the termination point and the ESD protection diodes. These resistors are matched to better than 2% for excellent signal level matching for the R/G/B signals.

When the PWR_UP input is driven LOW the SYNC inputs can be floated without causing the SYNC buffers to draw any current from the V_{CC3} supply. When the PWR_UP input is LOW the SYNC outputs are driven LOW.

An internal diode (D1 in schematic below) is also provided so that V_{CC3} can be derived from V_{CC4}, if desired, by connecting V_{CC3} to V_BIAS. In applications where V_{CC4} may be powered down, diode D1 blocks any DC current paths from the DDC_OUT pins back to the powered down V_{CC4} rail via the top ESD protection diodes.

Schematic Diagram



C0641299

ABSOLUTE MAXIMUM RATINGS		
Parameter	Rating	Unit
V_{CC1}, V_{CC2} , V_{CC3} & V_{CC4} supply voltage	GND-0.5, +6.0	V
Diode D1 forward current	100	uA
DC voltage at inputs:		V
VIDEO_1, VIDEO_2, VIDEO_3	GND-0.5, V_{CC1}+0.5	V
TERM_1, TERM_2, TERM_3	-6.0, +6.0	V
DDC_IN1, DDC_IN2	GND-0.5, V_{CC2}+0.5	
DDC_OUT1, DDC_OUT2	GND-0.5, V_{CC3}+0.5	V
SYNC_IN1, SYNC_IN2	GND-0.5, V_{CC4}+0.5	V
Temperature:		
Storage	-40 to +150	ºC
Operating Ambient	0 to +70	ºC
Package power dissipation	1.0	W

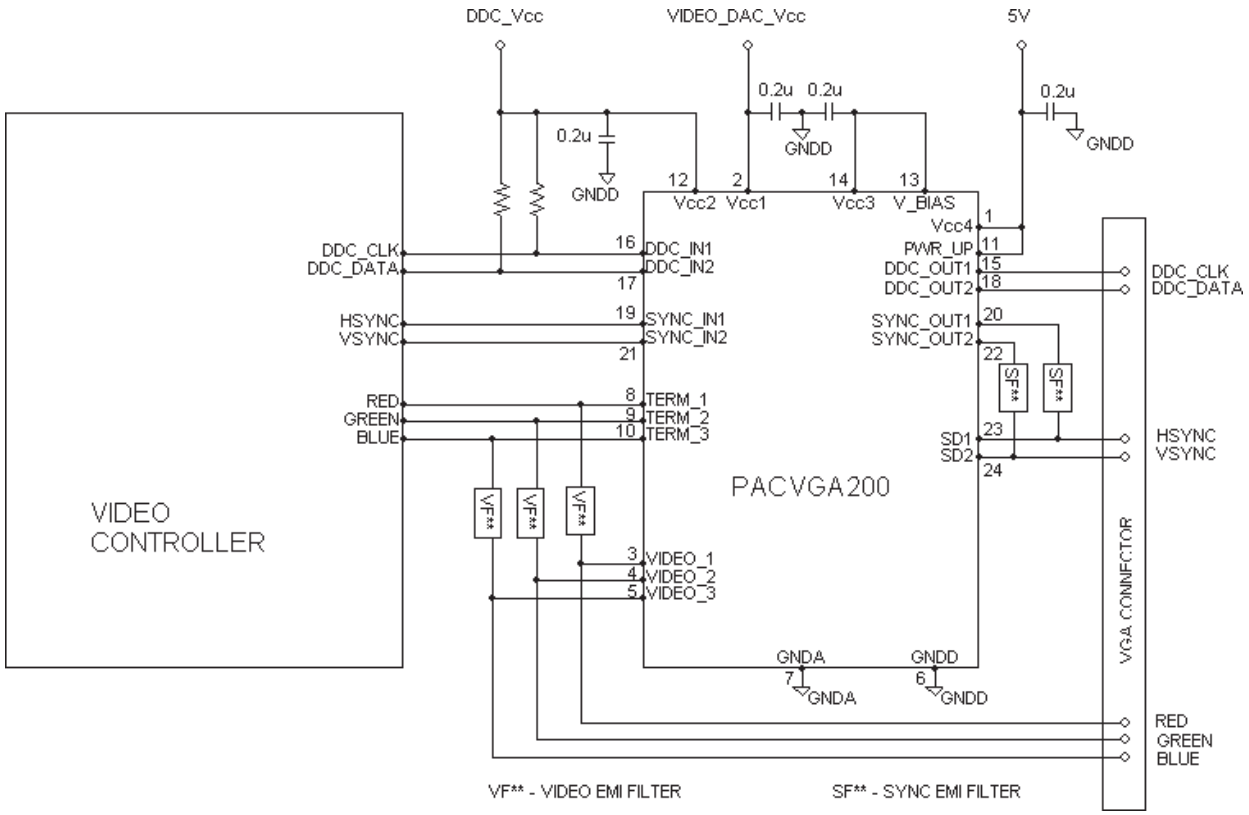
ELECTRICAL OPERATING CHARACTERISTICS (over operating conditions unless specified otherwise)						
Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
I_{CC1}	V_{CC1} supply current	V_{CC1} = 5V; VIDEO inputs at V_{CC1} or GND			10	uA
$I_{CC2, 3}$	V_{CC2}, V_{CC3} supply current	V_{CC2} = V_{CC3} = 5V			10	uA
I_{CC4}	V_{CC4} supply current	V_{CC4} = 5V; SYNC inputs at GND or V_{CC4}; PWR_UP pin at V_{CC4}; SYNC outputs unloaded		10		uA
		V_{CC4} = 5V; SYNC inputs at 3.0V; PWR_UP pin at V_{CC4}; SYNC outputs unloaded		200		uA
		V_{CC4} = 5V; PWR_UP input at GND; SYNC outputs unloaded			10	uA
V_{BIAS}	V_{BIAS} open circuit voltage	No external current drawn from V_{BIAS} pin		V_{CC4}-0.8		V
R_T	VIDEO termination resistance		71.25	75	78.75	Ω
	R_T resistance matching			1	2	%
V_{IH}	Logic High input voltage[1]	V_{CC4} = 5.0V	2.0			V
V_{IL}	Logic Low input voltage[1]	V_{CC4} = 5.0V			0.8	V
V_{OH}	Logic High output voltage[1]	I_{OH} = -4mA, V_{CC4} = 5.0V	4.4			V
V_{OL}	Logic Low output voltage[1]	I_{OL} = 4mA, V_{CC4} = 5.0V			0.4	V
R_b, R_p	Resistor value	PWR_UP, V_{CC3} = 5.0V	0.5	1	2	MΩ
R_c	V_{CC2} pull-down resistor	V_{CC2} = 3.0V	0.5	1.5	3	MΩ
I_N	Input current					
	VIDEO inputs	V_{CC1} = 5V; V_{IN} = V_{CC1} or GND			±1	µA
	HSYNC, VSYNC inputs	V_{CC4} = 5V; V_{IN} = V_{CC4} or GND			±1	µA
I_{OFF}	OFF state leakage current, level shifting NFET	(V_{CC2} - V_{DDC_IN}) ≤ 0.4V; V_{DDC_OUT}= V_{CC2}			10	µA
		(V_{CC2} - V_{DDC_OUT}) ≤ 0.4V; V_{DDC_IN}= V_{CC2}			10	µA
V_{ON}	Voltage drop across level shifting NFET when turned ON	V_{CC2} = 2.5V; V_S = GND, I_{DS} = 3mA			0.15	V
C_{IN}	Input capacitance [3]					
	VIDEO_1, VIDEO_2, VIDEO_3	V_{CC1} = 5.0V; V_{IN} = 2.5V; measured at 1MHz		4.0		pF
		V_{CC1} = 2.5V; V_{IN} = 1.25V; measured at 1MHz		4.5		
t_{PLH}	SYNC drivers L-H propagation delay	C_L = 50 pF; V_{CC} = 5V; Input t_r and t_f ≤ 5ns		8	12	ns
t_{PHL}	SYNC drivers H-L propagation delay	C_L = 50 pF; V_{CC} = 5V; Input t_r and t_f ≤ 5ns		8	12	ns
t_r, t_f	SYNC drivers output rise & fall times	C_L = 50 pF; V_{CC} = 5V; Input t_r and t_f ≤ 5ns		7		ns
V_{ESD}	ESD withstand voltage[2, 3]	V_{CC1} = V_{CC3} = V_{CC4} = 5V	±8			kV

Note 1: These parameter applies only to the HSYNC and VSYNC channels.

Note 2: Per the IEC-61000-4-2 International ESD Standard, Level 4 contact discharge method. V_{CC1}, V_{CC3} and V_{CC4} must be bypassed to GND via a low impedance ground plane with a 0.2uF, low inductance, chip ceramic capacitor at each supply pin. ESD pulse is applied between the applicable pins and GND. ESD pulse can be positive or negative with respect to GND. Applicable pins are: VIDEO_1, VIDEO_2, VIDEO_3, SYNC_OUT1, SD1, SYNC_OUT2, SD2, DDC_OUT1 and DDC_OUT2. All other pins are ESD protected to the industry standard 2kV per the Human Body model (MIL-STD-883, Method 3015).

Note 3: This parameter is guaranteed by design and characterization.

Typical Connection Diagram



A resistor may be necessary between the V_{CC3} pin and ground if protection against a stream of ESD pulses is required while the PACVGA200 is in the power-down state. The value of this resistor should be chosen such that the extra charge deposited into the V_{CC3} bypass capacitor by each ESD pulse will be discharged before the next ESD pulse occurs. The maximum ESD repetition rate specified by the IEC-61000-4-2 standard is one pulse per second. When the PACVGA200 is in the power-up state, an internal discharge resistor is connected to ground via an FET switch for this purpose.

For the same reason, V_{CC1} and V_{CC4} may also require bypass capacitor discharging resistors to ground if there are no other components in the system to provide a discharge path to ground.

GNDA, the reference voltage for the 75R resistors is not connected internally to GNDD and should ideally be connected to the ground of the video DAC IC.

STANDARD PART ORDERING INFORMATION		
Package		Ordering Part Number
Pins	Style	Part Marking
24	QSOP	PACVGA200Q

When placing an order please specify desired shipping: Tubes or Tape & Reel.