

February 1984 Revised February 2002

# MM74HCT05 Hex Inverter (Open Drain)

### **General Description**

The MM74HCT05 is a logic function fabricated by using advanced silicon-gate CMOS technology, which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. The device is also input and output characteristic and pinout compatible with standard DM74LS logic families. The MM74HCT05 open drain Hex Inverter requires the addition of an external resistor to perform a wire-NOR function.

All inputs are protected from static discharge damage by internal diodes to  $\rm V_{CC}$  and ground.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

### **Features**

- Open drain for wire-NOR function
- LS-TTL pinout and threshold compatible
- Fanout of 10 LS-TTL loads
- Typical propagation delays:

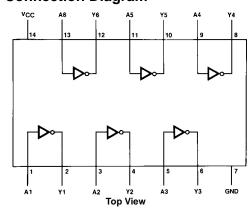
 $t_{PZL}$  (with 1 k $\Omega$  resistor) 10 ns  $t_{PLZ}$  (with 1 k $\Omega$  resistor) 8 ns

### **Ordering Code:**

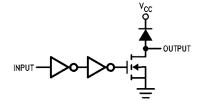
Order Number	Package Number	Package Description
MM74HCT05M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HCT05SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HCT05MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT05N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

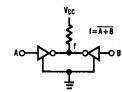
### **Connection Diagram**



### **Logic Diagram**



### **Typical Application**



## **Absolute Maximum Ratings**(Note 1)

(Note 2)

(Note 3) 600 mW S.O. Package only 500 mW

Lead Temperature (T<sub>L</sub>)

(Soldering 10 seconds) 260°C

# Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V <sub>CC</sub> )	4.5	5.5	V
DC Input Voltage (V <sub>IN</sub> )	0	$V_{CC}$	V
Output Voltage (V <sub>OUT</sub> )	0	5.5	V
Operating Temperature Range (T <sub>A</sub> )	-40	+85	°C
Input Rise or Fall Times			
$(t_r, t_f)$		500	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: –

12 mW/°C from 65°C to 85°C.

### **DC Electrical Characteristics**

(VCC = 5V  $\pm$  10%,unless otherwise specified)

Symbol	Parameter	Conditions	T <sub>A</sub> = 25°C		T <sub>A</sub> = -40 to 85°C	Units
			Тур	Typ Guaranteed Limits		
V <sub>IH</sub>	Minimum HIGH Level Input Voltage			2.0	2.0	V
V <sub>IL</sub>	Maximum LOW Level Input Voltage			0.8	0.8	V
V <sub>OL</sub>	Maximum LOW	$V_{IN} = V_{IH}$				
	Level Voltage	$ I_{OUT}  = 20 \mu A$	0	0.1	0.1	V
		$ I_{OUT}  = 4.0 \text{ mA}, V_{CC} = 4.5 \text{V}$	0.2	0.26	0.33	V
		$ I_{OUT}  = 4.8 \text{ mA}, V_{CC} = 5.5 \text{V}$	0.2	0.26	0.33	
I <sub>IN</sub>	Maximum Input Current	$V_{IN} = V_{CC}$ or GND,		± 0.1	± 1.0	μА
		V <sub>IH</sub> or V <sub>IL</sub>		± 0.1	± 1.0	μΑ
I <sub>LKG</sub>	Maximum HIGH Level	$V_{IN} = V_{IH}$ or $V_{IL}$ ,		0.5	5.0	μА
	Output Leakage Current	$V_{OUT} = V_{CC}$		0.5		
I <sub>CC</sub>	Maximum Quiescent	V <sub>IN</sub> = V <sub>CC</sub> or GND	2.0		20	A
	Supply Current	$I_{OUT} = 0\mu A$		2.0	20	μΑ
		V <sub>IN</sub> = 2.4V or 0.5V (Note 4)		0.3	0.4	mA
I <sub>OHZ</sub>	Off State Current	V <sub>CC</sub> = 4.5 - 5.5, V <sub>O</sub> = 5.5			10	μΑ

Note 4: This is measured per input with all other inputs held at V<sub>CC</sub> or ground.

### **AC Electrical Characteristics**

 $V_{CC} = 5V$ ,  $T_A = 25^{\circ}C$ ,  $C_L = 15$  pF,  $t_r = t_f = 6$  ns unless otherwise noted.

Symbol	Parameter	Conditions	Тур	Guaranteed Limit	Units
t <sub>PZL</sub>	Maximum Propagation Delay	$R_L = 1 \text{ k}\Omega$	8	15	ns
t <sub>PLZ</sub>	Maximum Propagation Delay	$R_L = 1 k\Omega$	9	16	ns

### **AC Electrical Characteristics**

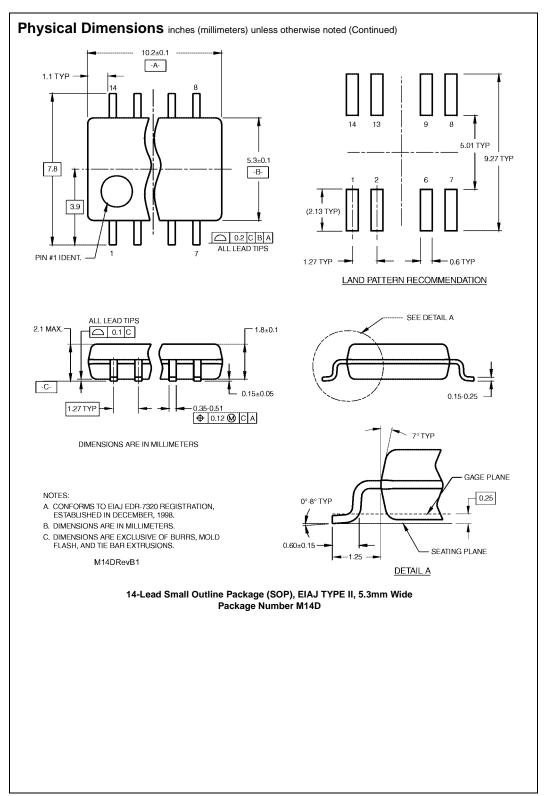
 $\mbox{V}_{CC}=5\mbox{V},\,\pm$  10%,  $\mbox{C}_{L}=50\mbox{pF},\,t_{f}=t_{f}=6$  ns unless otherwise specified.

Symbol	Parameter	Conditions	T <sub>A</sub> =25°C		T <sub>A</sub> = -40 to 85°C	Units
			Тур	Guara	nteed Limits	J.III.
t <sub>PZL</sub>	Maximum Propagation Delay	$R_L = 1k\Omega$	10	22	28	ns
t <sub>PLZ</sub>	Maximum Propagation Delay	$R_L = 1 \text{ k}\Omega$	12	20	25	ns
t <sub>THL</sub>	Maximum Output Fall Time		10	15	19	ns
C <sub>PD</sub>	Power Dissipation Capacitance (Note 5)	(per gate) R <sub>L</sub> = ∞		20		pF
C <sub>IN</sub>	Maximum Input Capacitance			5	10	pF

Note 5:  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} \ V_{CC}^2 \ f + I_{CC} \ V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} \ V_{CC} \ f + I_{CC}$ .

# Physical Dimensions inches (millimeters) unless otherwise noted $\frac{0.335 - 0.344}{(8.509 - 8.738)}$ LEAD NO. 1 IDENT 0.010 MAX (0.254) $\frac{0.150 - 0.157}{(3.810 - 3.988)}$ $\frac{0.053 - 0.069}{(1.346 - 1.753)}$ $\frac{0.010 - 0.020}{(0.254 - 0.508)}$ 8° MAX TYP ALL LEADS $\frac{0.004 - 0.010}{(0.102 - 0.254)}$ SEATING PLANE 0.014 0.008 - 0.010 (0.203 - 0.254) TYP ALL LEADS 0.050 (1.270) TYP $\frac{0.014 - 0.020}{(0.356 - 0.508)} \text{ TYP}$ 0.016 - 0.050 (0.406 - 1.270) TYP ALL LEADS 0.004 (0.102) ALL LEAD TIPS 0.008 (0.203) TYP M14A (REV h)

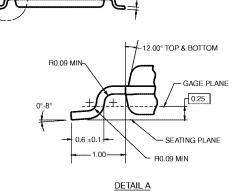
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A



# Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 5.0±0.1 0.43 TYP -A-6.4 4.4±0.1 -B-3.2 0.2 C B A 0.65 ALL LEAD TIPS LAND PATTERN RECOMMENDATION PIN #1 IDENT. - SEE DETAIL A ALL LEAD TIPS 1.2 MAX □ 0.90 +0.15 0.09-0.20 -C-L <sub>0.10±0.05</sub> 0.65 0.19 - 0.30 ⊕ 0.13 M A B C C R0.09 MIN NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC14RevC3



7.72

4.16

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

#### Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770(18.80 - 19.56)0.090 (2.286) 14 13 12 11 10 9 8 14 13 12 0.250 ± 0.010 PIN NO. 1 IDENT PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA 0.030 MAX (0.762) DEPTH OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320 $\overline{(7.620 - 8.128)}$ 0.065 $\frac{0.145 - 0.200}{(3.683 - 5.080)}$ 0.060 4° TYP Optional (1.524) (1.651) $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 0.020 (0.508) 0.125 - 0.150 $0.075 \pm 0.015$ $\overline{(3.175 - 3.810)}$ 0.280 (1.905 ± 0.381) 0.014-0.023 TYP (7.112) MIN 0.100 ± 0.010 (2.540 ± 0.254) (0.356 - 0.584) $\frac{0.050\pm0.010}{(1.270-0.254)}$ TYP 0.325 <sup>+0.040</sup> -0.015 $8.255 + 1.016 \\ -0.381$

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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