PHY (TC-PMD) for 25.6 Mbps ATM Networks

IDT77105

Features List

- **Performs the PHY-Transmission Convergence (TC) and Physical Media Dependent (PMD) Sublayer functions for 25.6 Mpbs ATM Networks**
- **Performs clock/data recovery, serializing/deserializing & framing**
- **ITU-T I.432 and I.432.5 compliant**
- **ATM Forum af-phy-0040 compliant**
- **UTOPIA Level 1 Interface**
- **2-Cell Transmit & Receive FIFOs**
- **Supports Multi PHY Connections**
- **LED Interface for status signalling**
- **Supports UTP Category 3 (CAT 3) physical media**
- **Interfaces to standard magnetics**
- **Low-Power CMOS**
- **64-pin STQFP Package (10 x 10mm)**

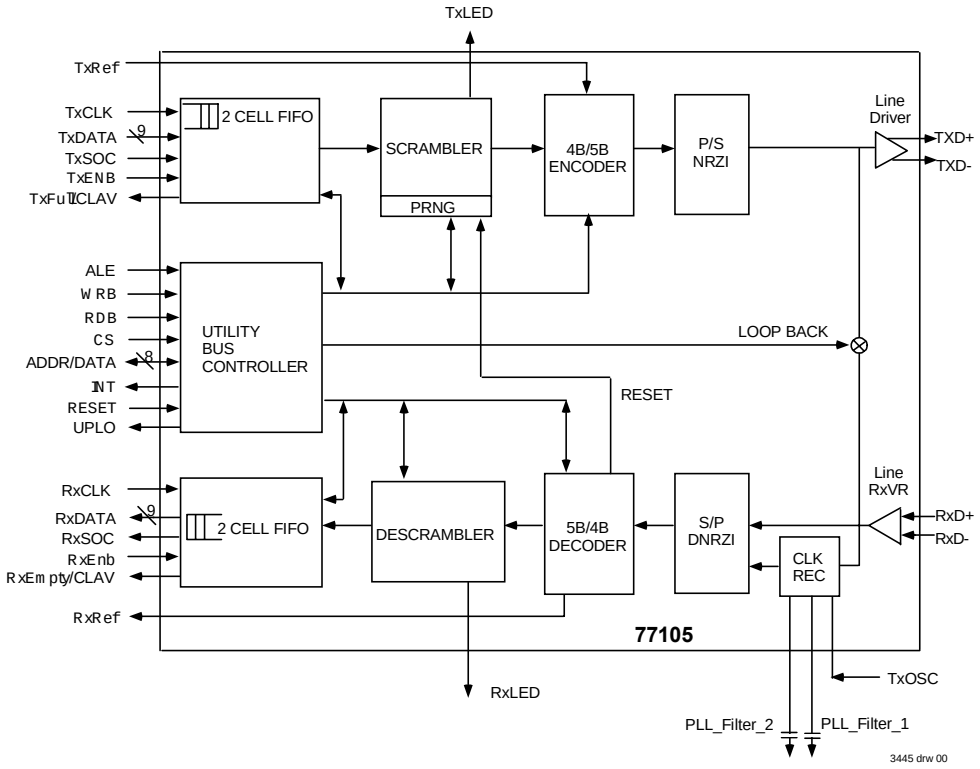
Description

The IDT77105 is a member of IDT's family of products developed to support Asynchronous Transfer Mode (ATM) data communications and networking. The IDT77105 provides the Transmission Convergence (TC) and (PMD) layers of a 25.6 Mbps ATM PHY suitable for ATM networks using Unshielded Twisted Pair (UTP) Category 3 (or better) wiring. The UTOPIA interface provides standardized control and communications to other components, such as Segmentation and Reassembly (SAR) controllers and ATM switches.

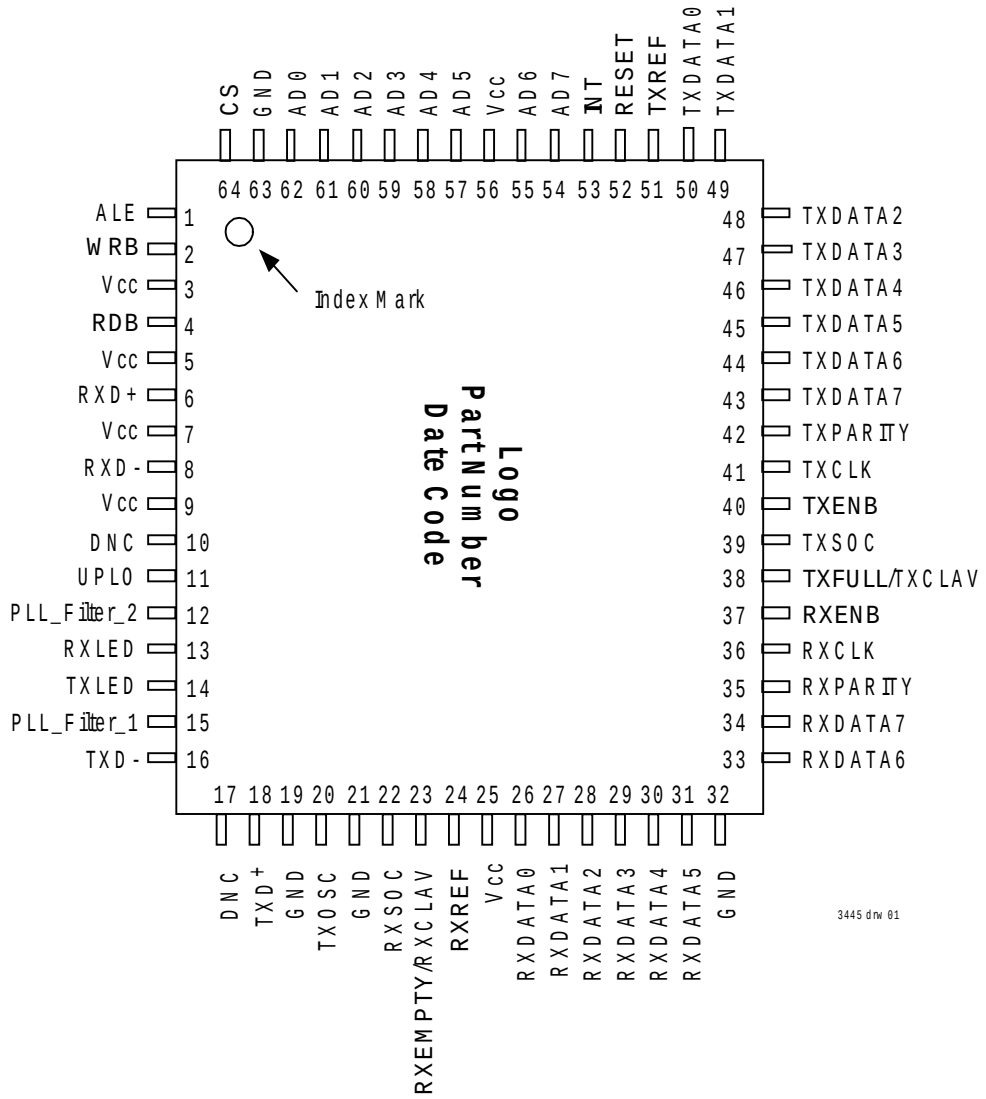
The IDT77105 supports a simple interface to magnetics modules.

The IDT77105 is fabricated using IDT's state-of-the-art CMOS technology, providing the highest levels of integration, performance and reliability, with the low-power consumption characteristics of CMOS.

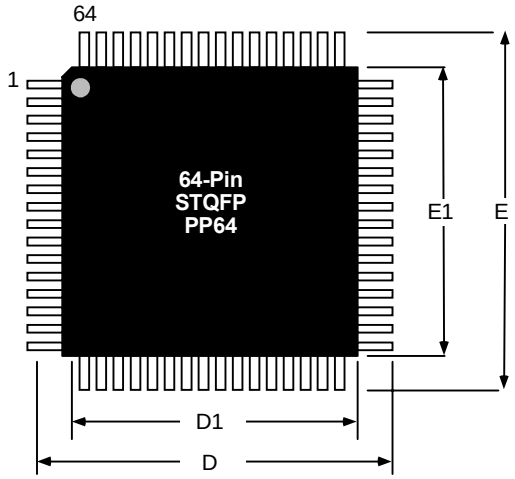
Block Diagram

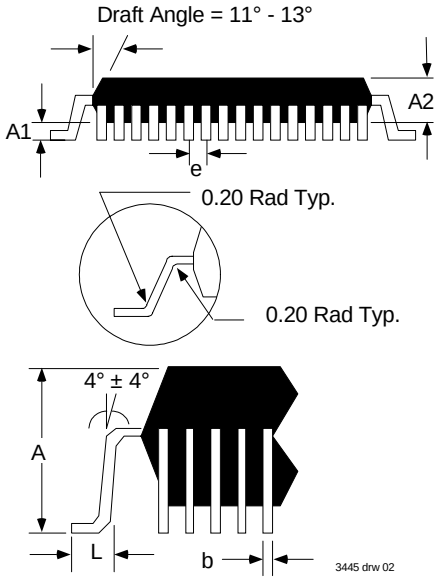


Pin Configurations



Package Dimensions





Dimensions

Dimension Letter	Tolerance (mm)	Dimension (mm)
A	Max.	1.60
A1	±.05	0.10
A2	±.05	1.40
D	±.10	12.00
D1	±.10	10.00
E	±.10	12.00
E1	±.10	10.00
L	±15	0.60
e	Basic	0.50
b	05	0.22

Absolute Maximum Ratings(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +120	°C
I_{OUT}	DC Output Current	50	mA

Note: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Digital Supply Voltage	4.5	5.5	V
GND	Digital Ground Voltage	0	0	V
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3V	V
V_{IL}	Input Low Voltage	GND-0.3V	0.8	V

Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature	GND	Unit
Commercial	0°C to +70°C	0V	5.0V ± 0.5V
Industrial	-40°C to +85°C	0V	5.0V ± 0.5V

DC Electrical Characteristics

Symbol	Parameter	Min.	Max.	Unit
I_{LI} [1]	Input Leakage Current (any input)	-1	1	µA
I_{LO} [2]	Output Leakage Current	-10	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = -2mA	2.4	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8mA	—	0.4	V
I_{DDI} [3]	Active Power Supply Current	—	100	mA

1. Measurements with 0.4V ≤ VIN ≤ VCC.

2. 0.4V ≤ VOUT ≤ VCC.

3. Tested at f = 32MHz with outputs unloaded. Add 13mA additional current when TxD outputs are driving a typical load.

Output Parameters for Transmit Line Signal @ Vcc = 5V ± 10%

Symbol	Parameter	Min.	Typ.	Max.	Unit
Voh	Output High Voltage for Transmit Line Signal, Ioh = 8mA	Vcc - 0.5V	—	—	V
Vol	Output Low Voltage for Transmit Line Signal, Ioh = 8mA	—	—	0.5	V
Ioh	Output High Current for Transmit Line Signal	—	80	—	mA
Iol	Output Low Current for Transmit Line Signal	—	75	—	mA
ZOUT	Output Impedance	—	20	—	Ohm

Input Parameters for IDT77105 Receive Line Signal

Symbol	Parameter	Min.	Typ.	Max.	Unit
ILI	Input Leakage Current[1]	-1	—	1	µA
CIN	Input Capacitance[2]	—	—	10	pF

1. Input Voltage = 2.5V (typ) ± 600mV

2. Measured with f=1MHz

Capacitance (T_A = +25°C, f = 1MHz)

Symbol	Parameter	Conditions	Max.	Unit
CIN[1]	Output Capacitance	VIN = 0V	10	pF
COUT[1]	Input Capacitance	VOUT = 0V	10	pF

1. Characterized values, not currently tested.

Pin Description

Pin	Name	I/O	Interfaces to	Description
1	ALE	I	Utility bus	Address Latch Enable signal. The falling edge of ALE is used to latch the address on AD[7:0].
2	WRB	I	Utility bus	Write Byte Enable (active low).
3	VCC	—	Power Plane	
4	RDB	I	Utility bus	Read Byte Enable (active low).
5	VCC	—		Reserved input
6	RxD+	I	Magnetics	Positive Differential receive serial data input.
7	VCC	—		Reserved input
8	RxD-	I	Magnetics	Negative Differential receive serial data input.
9	VCC	—		Reserved input
10	DNC	—	N/A	NOTE: This pin should float.
11	UPLO	O	User defined	User Programmed Latched Output of Reg 0, bit 7 (opposite polarity).
12	PLL_Filter_2	—	Discrete Capacitor	(See Figure 20).
13	RxLED	O	LED	LED driver output (see Figure 8). Pulses low when a cell is being received.
14	TxLED	O	LED	LED driver output (see Figure 8). Pulses low when a cell is being transmitted
15	PLL_Filter_1	—	Discrete Capacitor	(See Figure 20).
16	TXD–	O	Magnetics	Differential Negative transmit serial data output.
17	DNC	O	N/A	NOTE: This pin should float.
18	TxD+	O	Magnetics	Differential Positive transmit serial data output.
19	GND	—	Ground plane	
20	TxOsc	I	OSC	Input from an external clock oscillator. 32MHz for 25.6 Mbps; ±100ppm
21	GND	—	Ground plane	

Table 1 Pin Description (Part 1 of 2)

Pin	Name	I/O	Interfaces to	Description
22	RxSOC	O	UTOPIA bus	Receive Start of Cell signal.
23	RxEmpty/RxClav	O	UTOPIA bus	Receive Empty (active low; byte mode) or Receive Cell Available (active high; cell mode).
24	RxRef	O	UTOPIA bus	Receive Reference signal (active low). This pin is driven in response to a received X_8 command byte. Assertion duration is programmable to 1,2,4 or 8 clocks, as set via register 0x03, bits 3,4.
25	Vcc	—	Power plane	
26	RxData0	O	UTOPIA bus	Receive data bit 0.
27	RxData1	O	UTOPIA bus	Receive data bit 1.
28	RxData2	O	UTOPIA bus	Receive data bit 2.
29	RxData3	O	UTOPIA bus	Receive data bit 3.
30	RxData4	O	UTOPIA bus	Receive data bit 4.
31	RxData5	O	UTOPIA bus	Receive data bit 5.
32	GND	—	Ground plane	
33	RxData6	O	UTOPIA bus	Receive data bit 6.
34	RxData7	O	UTOPIA bus	Receive data bit 7.
35	RxParity	O	UTOPIA bus	Parity bit for RxData[7:0].
36	RxClk	I	UTOPIA bus	Receive data path synchronization clock.
37	RxEnb	I	UTOPIA bus	Receive Enable signal (active low).
38	TxFull/TxCLAV	O	UTOPIA bus	Transmit Full (active low; byte mode) or Transmit Cell Available (active high; cell mode).
39	TxSOC	I	UTOPIA bus	Transmit Start of Cell signal.
40	TxEnb	I	UTOPIA bus	Transmit Enable signal (active low).
41	TxClk	I	UTOPIA bus	Transmit data path synchronization clock.
42	TxParity	I	UTOPIA bus	Parity bit for TxData[7:0]. If unused, this pin must be tied high or low.
43	TxData7	I	UTOPIA bus	Transmit data bit 7.
44	TxData6	I	UTOPIA bus	Transmit data bit 6.
45	TxData5	I	UTOPIA bus	Transmit data bit 5.
46	TxData4	I	UTOPIA bus	Transmit data bit 4.
47	TxData3	I	UTOPIA bus	Transmit data bit 3.
48	TxData2	I	UTOPIA bus	Transmit data bit 2.
49	TxData1	I	UTOPIA bus	Transmit data bit 1.
50	TxData0	I	UTOPIA bus	Transmit data bit 0.
51	TxRef	I	UTOPIA bus	Transmit Reference signal input (active low). Assertion (falling edge) of this pin stimulates insertion of command byte X_8 into the transmit data stream.
52	Reset	I	control	Reset signal (active low).
53	INT	O	control	Interrupt signal (active low). Always driven.
54	AD7	I/O	Utility bus	Address/Data bit 7. Not used for addressing.
55	AD6	I/O	Utility bus	Address/Data bit 6. Not used for addressing.
56	VCC	—	Power plane	
57	AD5	I/O	Utility bus	Address/Data bit 5. Not used for addressing.
58	AD4	I/O	Utility bus	Address/Data bit 4. Not used for addressing.
59	AD3	I/O	Utility bus	Address/Data bit 3. Not used for addressing.
60	AD2	I/O	Utility bus	Address/Data bit 2.
61	AD1	I/O	Utility bus	Address/Data bit 1.
62	AD0	I/O	Utility bus	Address/Data bit 0.
63	GND	—	Ground plane	
64	CS	I	Utility bus	Utility Bus Chip select (active low).

Table 1 Pin Description (Part 2 of 2)

Functional Description

25MbpsATM Communications Standard

The IDT77105 implements the physical layer standard for 25.6Mbps ATM network communications. The physical layer is divided into a Physical Media Dependent sub layer (PMD) and Transmission Convergence (TC) sub layer. The PMD sub layer includes the functions for the transmitter, receiver, and timing recovery that allow connection to transmission media conforming to TIA/EIA 568 (UTP Category 3). The TC sub layer defines the line coding, scrambling, data framing and synchronization, and is described below.

Transmission Convergence (TC) Sub Layer

Introduction

Under control of a switch interface or Segmentation and Reassembly (SAR) unit, the 25.6Mbps ATM PHY accepts a 53-byte ATM cell, scrambles the data, appends a command byte to the beginning of the cell, and encodes the entire 53 bytes before transmission. These data transformations ensure that the signal is evenly distributed across the frequency spectrum. In addition, the serialized bit stream is NRZI coded. An 8kHz timing sync pulse may be used for isochronous communications.

Data Structure and Framing

Each 53-byte ATM cell is preceded with a command byte. This byte is distinguished by an escape symbol followed by one of 17 encoded symbols. Together, this byte forms one of seventeen possible command bytes. Three command bytes are defined:

1. X_X (read: 'escape' symbol followed by another 'escape'): Start-of-cell with scrambler/descrambler reset.
2. X_4 ('escape' followed by '4'): Start-of-cell without scrambler/descrambler reset.
3. X_8 ('escape' followed by '8'): 8kHz timing marker. This command byte is generated when the 8kHz sync pulse is detected, and has priority over all line activity (data or command bytes). It is transmitted immediately when the sync pulse is detected. When this occurs during a cell transmission, the data transfer is temporarily interrupted on an octet boundary, and the X_8 command byte is inserted. This condition is the only allowed interrupt in an otherwise contiguous transfer.

Below is an illustration of the cell structure and command byte usage:

{X_X} {53-byte ATM cell} {X_4} {53-byte ATM {X_8} cell} ...

In the above example, the first ATM cell is preceded by the X_X start-of-cell command byte which resets both the transmitter-scrambler and receiver-descrambler pseudo-random nibble generators (PRNG) to their initial states. The following cell illustrates the insertion of a start-of-cell command without scrambler/descrambler reset. During this cell's transmission, an 8kHz timing sync pulse triggers insertion of the X_8 8kHz timing marker command byte.

Transmission Description

Refer to the 25Mbps PHY Transmit Block Diagram on the previous page. Cell transmission begins with the Octet Interface Control:

- The SAR (or other upstream system) confirms that the PHY may accept transmit data by polling the TxFull flag. If this signal is 'high' (PHY xmit buffer not full), the SAR then asserts TxEnb.
- The SAR then asserts TxSOC for one cycle of TxCLK, while putting the first byte on the TxData bus. TxSOC is then deasserted.
- Following bytes are transmitted by putting them onto the TxData bus while TxEnb is asserted.
- 4-bit data (MSB first) is asynchronously (to TxClk) sent to the 'Scrambler'.

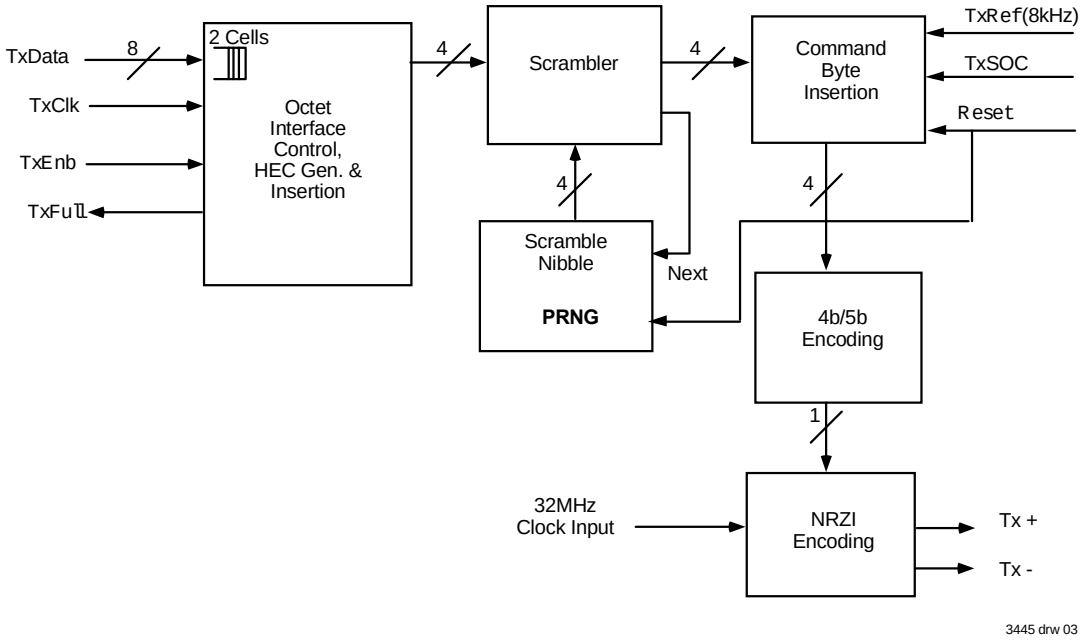


Figure 1 Mbps TC Transmit Block Diagram 8. 25 Mbps PHY Xmit Block Diagram

The 'Scrambler' takes each nibble of data and exclusive-ORs them against the 4 high order bits (X(t), X(t-1), X(t-2), X(t-3)) of a 10 bit pseudo-random nibble generator (PRNG). Its function is to provide the appropriate frequency distribution for the signal across the line.

The PRNG is clocked every time a nibble is processed, regardless of whether the processed nibble is part of a data or command byte. Note however that only data nibbles are scrambled. The entire command byte (X _C) is NOT scrambled before it's encoded (see diagram for illustration). The PRNG is based upon the following polynomial:

$X^{10} + X^7 + 1$

With this polynomial, the four output data bits (D3, D2, D1, D0) will be generated from the following equations:

D3 = d3 xor X(t-3)

D2 = d2 xor X(t-2)

D1 = d1 xor X(t-1)

D0 = d0 xor X(t)

The following nibble is scrambled with X(t+4), X(t+3), X(t+2), and X(t+1).

A scrambler lock between the transmitter and receiver occurs each time an X_X command is sent. An X_X command is initiated only at the beginning of a cell transfer after the PRNG has cycled through all of its states (210 - 1 = 1023 states). The first valid ATM data cell transmitted after power on will also be accompanied with an X_X command byte. Each time an X_X command byte is sent, the first nibble after the last escape (X) nibble is XOR'd with 1111b (PRNG = 3FFx).

Because a timing marker command (X_8) may occur at any time, the possibility of a reset PRNG start-of-cell command and a timing marker command occurring consecutively does exist (e.g. X_X_X_8). In this case, the detection of the last two consecutive escape (X) nibbles will cause the PRNG to reset to its initial 3FFx state. Therefore, the PRNG is clocked only after the first nibble of the second consecutive escape pair.

Once the data nibbles have been scrambled using the PRNG, the nibbles are further encoded using a 4b/5b process. The 4b/5b scheme ensures that an appropriate number of signal transitions occur on the line. A total of 17 5-bit symbols are used to represent the 16 4-bit data nibbles and the one escape (X) nibble. The table below lists the 4-bit data with their corresponding 5-bit symbols:

Data	Symbol
0000	10101
0100	00111
1000	10010
1100	10111

Data	Symbol
0001	01001
0101	01101
1001	11001
1101	11101

Data	Symbol
0010	01010
0110	01110
1010	11010
1110	11110

Data	Symbol
0011	01011
0111	01111
1011	11011
1111	11111

ESC(X) = 00010

3445 drw 03a

This encode/decode implementation has several very desirable properties. Among them is the fact that the output symbol bits can be represented by a set of relatively simple logic equations. The other main advantage is that it contains transmission properties that are desirable, which include:

- Transition averages over 3 per 5 signal elements;
- Encode/Decode is not affected by the incorporation of the scrambler;
- Run length is limited to <= 5;
- Disparity never exceeds +/- 1.

On the receiver, the decoder determines from the received symbols whether a timing marker command (X_8) or a start-of-cell command was sent (X_X or X_4). If a start-of-cell command is detected, the next 53 bytes received are decoded and forwarded to the descrambler. (See Receive Block Diagram, Figure 2).

The output of the 4b/5b encoder provides serial data to the NRZI encoder. The NRZI code transitions the wire voltage each time a '1' bit is sent. This, together with the previous encoding schemes guarantees that long run lengths of either '0' or '1's are prevented. Each symbol is shifted out with its most significant bit sent first.

When it has no cells to transmit, the 77105 keeps the line active by continuing to transmit valid symbols. It does not, however, transmit another start-of-cell command until it has another cell for transmission.

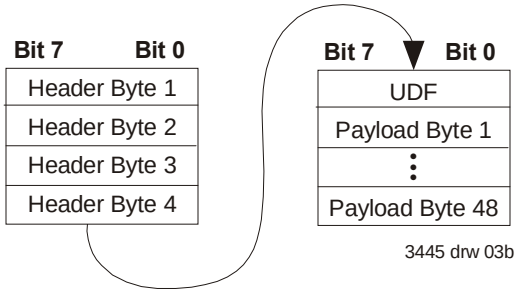
Transmit HEC Byte Calculation/Insertion

Byte #5 of each ATM cell, the HEC (Header Error Control) is calculated automatically across the first 4 bytes of the cell header, depending upon the setting of bit 5 of register 0x03. This byte is then either inserted as a replacement of the fifth byte transferred to the PHY by the external system, or the cell is transmitted as received. A second operating mode provides for insertion of "Bad" HEC codes which may aid in communication diagnostics.

Receiver Description

On the receiving end, the inverse occurs. The data is NRZI decoded before each symbol is reassembled. The symbols are then sent to the 5b/4b decoder, followed by the Command Byte Interpreter, De-Scrambler, and finally the UTOPIA interface to the outside world. Note that although the IDT77105 can detect symbol and HEC errors, it does not attempt to correct them.

ATM Cell Format



3445 drw 03b

UDF = User Defined Field (or HEC)

Upon reset or line re-connect, the IDT77105 receiver is typically not symbol-synchronized. Synchronization is established when it receives a command byte, usually the start-of-cell command preceding the first received cell.

The IDT77105 monitors line conditions and can provide an interrupt if the line is deemed 'bad'. The interrupt status register contains a Good Signal Bit (address 0x01, bit 6 set to 0 = Bad signal initially) which shows the status of the line per the following algorithm:

To declare “Good Signal” (from "Bad" to "Good"):

There is an up-down counter that counts from 7 to 0 and is initially set to 7. When the clock ticks for 1,024 cycles (32MHz clock, 1,024 cycles = 204.8 symbols) and no "bad symbol" has been received, the counter decreases by one (i.e., from 7 to 6). However, if at least one "bad symbol" is detected during these 1,024 clocks, the counter is increased by one with a maximum of 7 (i.e., from 6 back to 7). The Good Signal Bit is set to 1 when this counter reaches 0. The Good Signal Bit could be set to 1 as quickly as 1,433 symbols (204.8 x 7) if no bad symbols have been received.

To declare 'Bad Signal' (from "Good" to "Bad"):

The same up-down counter counts from 0 to 7 (being at 0 to provide a "Good" status). When the clock ticks for 1,024 cycles (32MHz clock, 1,024 cycles = 204.8 symbols) and there is at least one "bad symbol", the clock increases one (i.e., from 0 to 1). If it detects all "good symbols" and no "bad symbols" in the next time period, the counter decreases one (i.e., from 1 back to 0). The "Bad Signal" is declared when the counter reaches 7. The Good Signal Bit could be set to 0 as quickly as 1,433 symbols (204.8 x 7) if at least one "bad symbol" is detected in each 204.8 symbols of seven consecutive groups of 204.8 symbols.

UTOPIA Interface

The 'UTOPIA' (Universal Test & Operations PHY Interface for ATM) interface is used as the data path interface between the IDT77105 PHY and other system elements such as the Segmentation and Reassembly (SAR) device, or switching systems.

Overview

Cell data is transferred via separate Transmit and Receive synchronizing clocks which are controlled by the SAR or other system components. Transfer of data is synchronized at the cell level through the use of a Start of Cell signal. This signal is asserted when the data transfer path contains the first byte of a cell.

Since the PHY layer uses external clocks for data transfer synchronization, flow control signals are provided to allow both the external device and the PHY to throttle the data transfer rate.

Receive data is transferred when the RxEnb signal is asserted by an external device. The PHY also provides an RxEmpty signal to indicate that no valid data is ready for transfer out of the PHY. This signal is active if another read would cause a PHY buffer underflow. Along with RxEmpty, RxClav (Receive Cell Available) indicates that a complete cell has been received and is ready for transfer. Likewise, Transmit data is also transferred using similar controls and handshake signals.

The Status and Control interface for the IDT77105 PHY is provided to allow control of several functions such as Header Error Control (HEC) processing, diagnostics, and error notification/management.

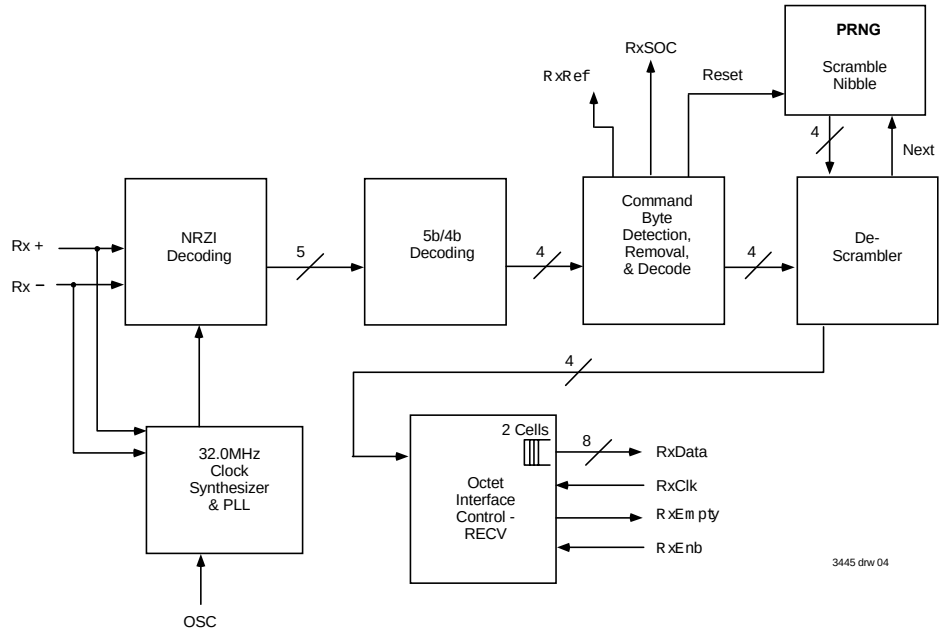


Figure 2

Transmit Interface

Signals

TxData[7:0], TxParity—Transmit Data. TxData[7] is the MSB.

TxSOC—Start Of Cell. Active high signal to be asserted when TxData contains the first byte of the cell.

TxENB—Enable. Active low signal to be asserted when TxData contains valid data.

TxFull/TxClav—Full/Cell Available. For octet (byte)-level handshake control, TxFull is an active low signal asserted by PHY at least 4 cycles before it is no longer able to accept transmit data. For cell-level flow control, the assertion of TxClav indicates that the PHY is capable of receiving an entire 53-byte cell.

TxClk—Transmit Clock. Data transfer clock to synchronize data transfers on TxData to PHY.

TxRef—Transmit Reference. 8kHz input for synchronization.

Operation and Timing

Cell transmission is controlled by the external system and is synchronized to TxClk. All signals are sampled on the rising edge of TxClk. Data is transferred to the PHY using one of two handshake methods: Octet (byte)-Level Handshake, Cell-Level Handshake. Handshake method is selected via setting of the Register 0x00 Bit 1. Octet (byte)-level handshake operates as follows:

- The PHY indicates it can accept data by deasserting TxFull. (The PHY may assert TxFull at any time which will indicate that no more than 4 write cycles (bytes) will be accepted.)
- If TxEnb is asserted by the external system, data is clocked into the PHY on the rising edge of TxClk. Note that TxEnb must be deasserted within 4 cycles of TxFull assertion, and must not be reasserted until after TxFull deassertion is detected.

The "cell-level" handshake is the same as the byte-level except that TxClav is only asserted when the PHY can accept transfer of an entire 53-byte cell. TxEnb must remain asserted until at least the last byte of the cell. If TxClav remains asserted at the end of the cell, TxEnb may also remain asserted, which allows uninterrupted cell transfer from the external system to the PHY.

Receive Interface

Signals

RxData[7:0], RxParity—Receive Data. RxData[7] is the MSB.

RxSOC—Start Of Cell. Active high signal asserted by PHY when RxData contains first byte of a cell.

RxEnb—Enable. Active low signal asserted externally to indicate that RxData and RxSOC will be sampled at the start of the next cycle.

RxEmpty/RxClav—Empty/Cell Available. For octet (byte)-level flow control, RxEmpty is an active low signal asserted by the PHY to indicate that in the current cycle there is no valid data available for delivery over RxData[7:0]. For cell-level flow control, RxClav indicates that an entire cell is available for immediate transfer over RxData. In both cases, this signal indicates cycles where there is valid data on RxData/RxSOC. For Cell-Level Handshake mode, if register 0x02, Bit 6 is set, RxClav can be deasserted by the PHY for 4 cycles before it is no longer able to transfer data out.

RxClk—Receive Clock. Transfer clock provided externally to synchronize transfers on RxData.

RxRef—Receive Reference. 8kHz output derived from incoming data stream.

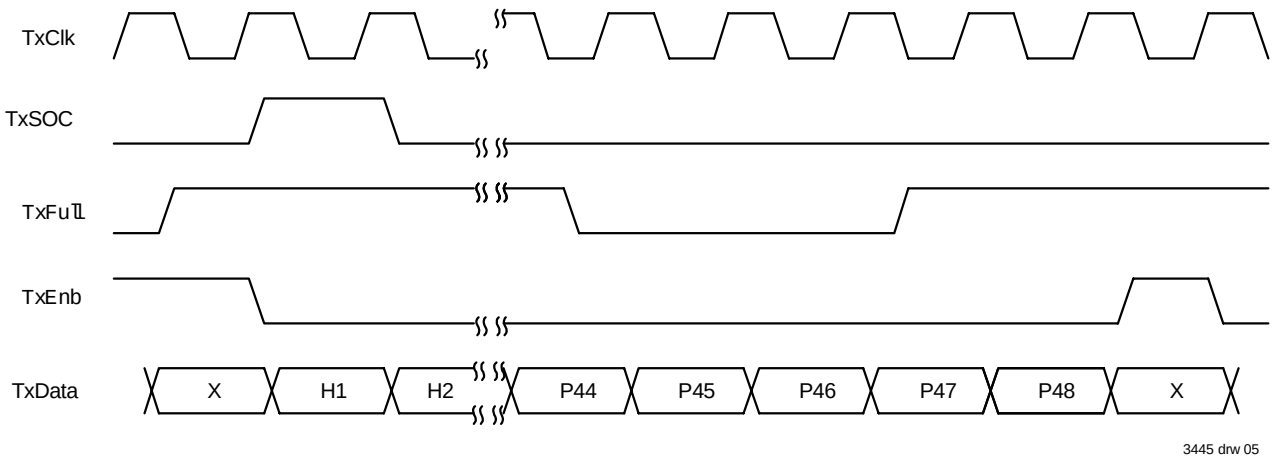


Figure 3 Transmit Waveform for Octet (byte)-Level Handshake

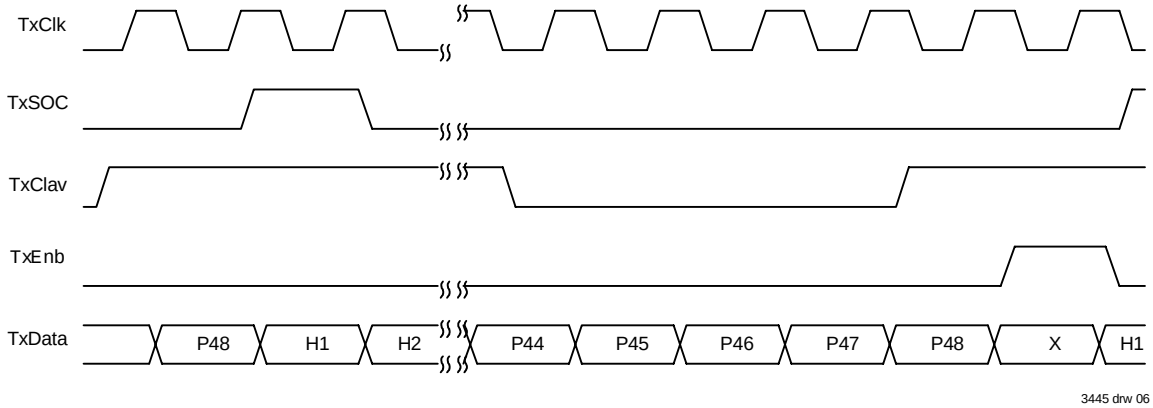


Figure 4 Transmit Waveform for Cell-Level Handshake

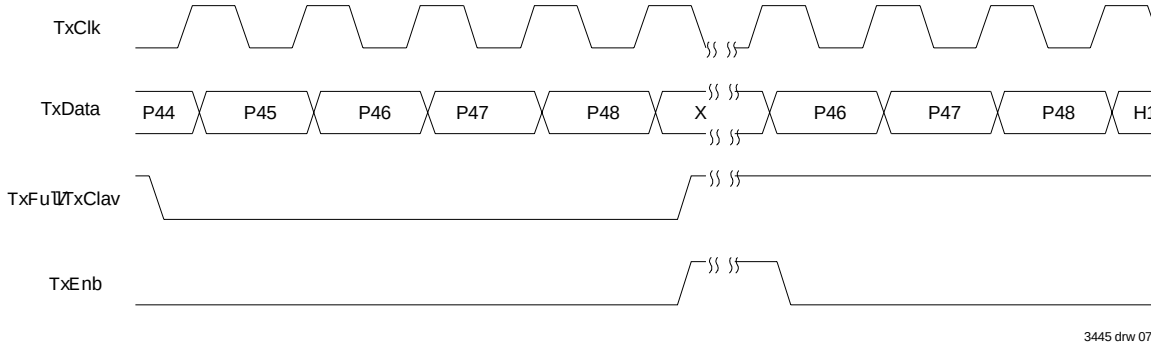


Figure 5 TxFull/TxClav Waveform

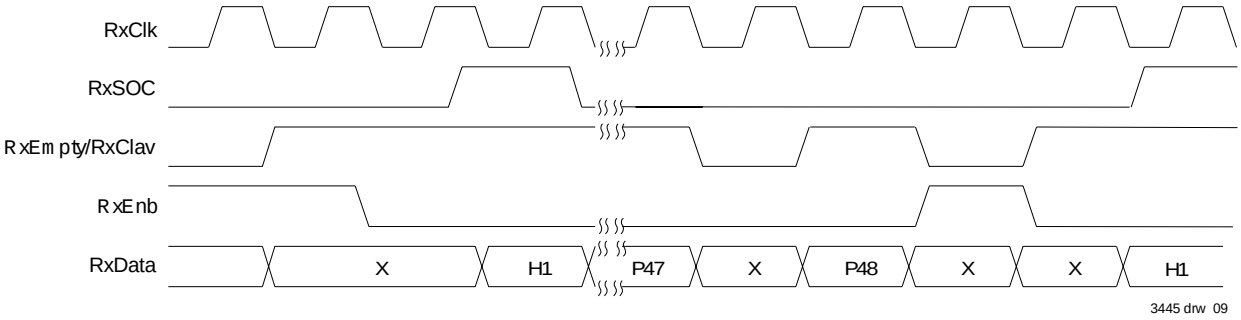


Figure 6 Receive Waveform for Cell or Octet-Level Handshake

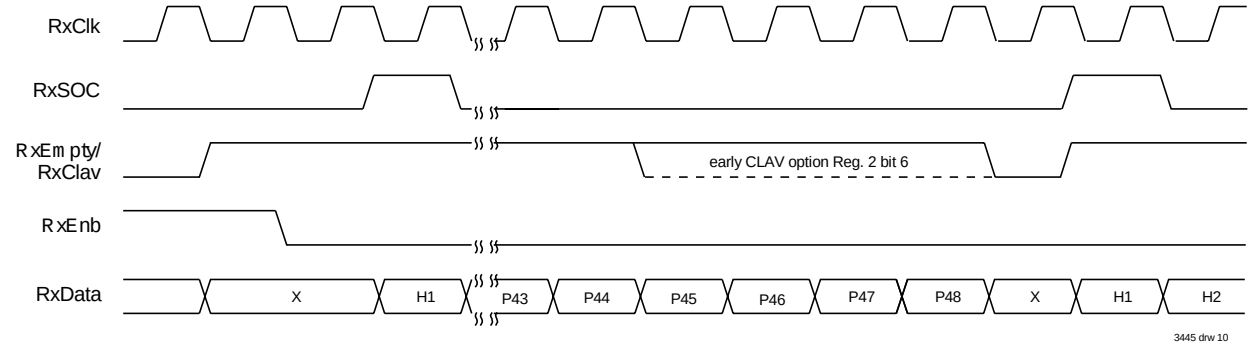


Figure 7 RxEmpty/RxClav Waveform

Operation and Timing

Received-cell transfer from the PHY is controlled externally and is synchronized to RxClk. Since data transfer is dependent upon an external system, a 2-cell FIFO is provided to buffer the receive data path. As with the transmit path, the receive data and controls are sampled on the rising edge of RxClk. The data is transferred from PHY to the external system by Octet (byte-Level Handshake or Cell-Level Handshake. Octet (byte)-Level handshake operates as follows:

- The PHY indicates it can transfer data into external system by deasserting RxEmpty.
- The RxEnb is asserted by the external system, data is clocked on the rising edge of RxClk from PHY into external system.

Cell-Level handshake operates as follows:

- The PHY indicates it can transfer an entire 53-byte cell into external system by asserting RxClav.
- The RxEnb is asserted by the external system, data is clocked on the rising edge of RxClk from PHY into external system. Note that for both Octet (byte)-Level Handshake and Cell-Level Handshake modes, once the PHY indicates data transfer by deasserting RxEmpty/asserting RxClav, the PHY has the capability to transfer the entire 53-byte cell out unless the RxEnb is deasserted by the external system.

Control and Status Interface

The Control and Status Interface provides the data and control pins needed to set and reset registers within the IDT77105. Registers are used to set desired operating characteristics and functions, and to communicate status to external systems.

The Control and Status Interface is implemented using a multiplexed address and data bus (AD[7:0]) where the register address is latched via the use of an Address Latch Enable.

Utility Bus

The Utility Bus is a byte-wide interface that provides access to the registers within the IDT77105. These registers are used to select desired operating characteristics and functions, and to communicate status to external systems.

The Utility Bus is implemented using a multiplexed address and data bus (AD[7:0]) where the register address is latched via the Address Latch Enable (ALE) signal.

The Utility Bus interface is comprised of the following pins:

AD[7:0]

ALE

CS

RDB

WRB

Read Operation

Refer to the Utility Bus waveforms on Figures 19 - 20. A register read is performed as follows:

1. Initial condition:
   - *RDB, WRB, CS not asserted (logic 1)*
   - *ALE not asserted (logic 0)*
2. Set up register address:
   - *place desired register address on AD[7:0]*
   - *set ALE to logic 1;*
   - *latch this address by setting ALE to logic 0.*
3. Read register data:
   - *Remove register address data from AD[7:0]*
   - *assert CS by setting to logic 0;*
   - *assert RDB by setting to logic 0*
   - *wait minimum pulse width time (see AC specifications)*

Write Operation

A register write is performed as described below:

1. Initial condition:
   - *RDB, WRB, CS not asserted (logic 1)*
   - *ALE not asserted (logic 0)*
2. Set up register address:
   - *place desired register address on AD[7:0]*
   - *set ALE to logic 1;*
   - *latch this address by setting ALE to logic 0.*
3. Write data:
   - *place data on AD[7:0]*
   - *assert CS by setting to logic 0;*
   - *assert WRB (logic 0) for minimum time (according to timing specification); reset WRB to logic 1 to complete register write cycle.*

Interrupt Operations

The IDT77105 provides a variety of selectable interrupt and signalling conditions which are useful both during 'normal' operation, and as diagnostic aids. Refer to the Status and Control Register List starting on Page 18.

Overall interrupt control is provided via register 0x00, bit 0. When this bit is cleared (set to 0), interrupt signalling is prevented. Additional interrupt signal control is provided by register 0x00, bit 5. When this bit is set (=1), receive cell errors will be flagged via interrupt signalling and all other interrupt conditions are masked. These errors include:

- *Bad receive HEC*
- *Short (fewer than 53 bytes) cells*
- *Received cell symbol error*

Normal interrupt operations are performed by setting register 0x00 bit-0 = 1, and bit-5 = 0. INT (pin 53) will go to a low state when an interrupt condition is detected. The external system should then interrogate the 77105 to determine which one (or more) conditions caused this flag, and reset the interrupt for further occurrences. This is accomplished by reading register 0x01. Decoding the bits in this byte will tell which error condition caused the interrupt. Reading register 0x01 also:

- *clears all interrupt status bits*
- *resets INT*

This leaves the interrupt system ready to signal an alarm for further problems.

Cable Disconnect Procedures and Link Establishment

During the initial state of connecting the line for IDT77105, there are some interrupts (“HEC Error Cell Received” interrupt, “Short Cell Received” interrupt, and “Received Cell Symbol Error” interrupt) that may appear. These interrupts should be masked.

When the line is disconnected, these interrupts may also appear, but this depends on the passive network between the magnetics and the 77105. Previous network recommendations did not adequately address this matter, the result being that the receiver would generate needless repetitive interrupts. The latest network recommendations, shown in Figure 21, pull the RXD+ and RXD- inputs to different D.C. voltages in the absence of a signal. This prevents false receive signals when there is no actual signal, and thus prevent repetitive interrupts.

Register Status for Established Link

IDT77105 register setting and status are as follows when the link condition exists.

Master Control Register 0x00	contents => 49h
Interrupt Status Register 0x01	contents => 40h
Diagnostic Control Register 0x02	contents => 00h

LED Control and Signalling

The LED outputs, pins 13 and 14 provide bi-directional LED drive capability of 10mA. As an example, the RxLED pin’s output is described in the truth table:

State	Pin Voltage
Cell being received	Low
Cells not being received	High

As illustrated in the following drawing (Figure 8), this could be connected to provide for a two-LED condition indicator. These could also be different colors to provide simple status indication at a glance. (The value of R is determined to limit LED current to 10mA or less as specified by the LED manufacturer. Minimum value for R should be 270Ω).

TxLED Truth Table (Pin 14)

State	Pin Voltage
Cell being transmitted	Low
Cells not being transmitted	High

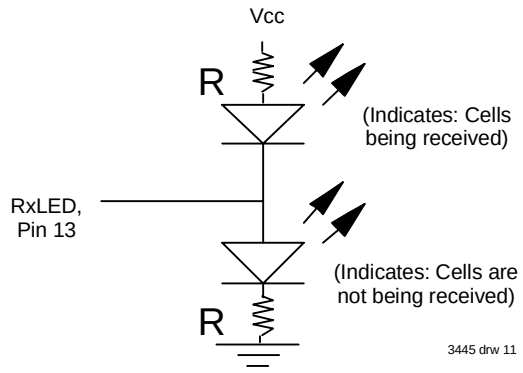


Figure 8

Diagnostic Functions

1. Loopback

There are two loopback modes supported by the 77105. The loopback mode is controlled via Register 0x02, bits 1 and 0:

0x02	Bit 1	Bit 0	
	0	0	Normal operating mode
	1	0	PHY Loopback
	1	1	Line Loopback

Normal Mode

This mode, Figure 9, supports normal operating conditions: data to be transmitted is transferred to the TC, where it is queued and formatted for transmission by the PMD. Receive data from the PMD is decoded along with its clock for transfer to the receiving "upstream system".

PHY Loopback

As Figure 10 illustrates below, this loopback mode provides a connection within the PHY between transmit and receive data. Note that while this mode is operating, no data is forwarded to or received from the line interface.

Line Loopback

Figure 11 might also be called “remote loopback” since it provides for a means to test the overall system, including the line. Since this mode will probably be entered under direction from another system (at a remote location), receive data is also decoded and transferred to the upstream system to allow it to listen for commands. A common example would be a command asking the upstream system to direct the TC to leave this loopback state, and resume normal operations.

Entering Loopback (Byte Mode)

In byte mode, the 77105 counts 53 bytes after each TxSOC, and after receiving a complete cell, the cell is transmitted.

1. Assert TxFull, via register 0x02, Bit 7. This stops the 77105 from receiving more data, and prevents the complete assembly of a cell for transmission.
2. Enter desired loopback mode.
3. De-assert TxFull using 0x02, Bit 7. The previously 'interrupted' cell will continue to be assembled in the transmit FIFO; on completion, it will be transmitted, as selected via the loopback mode. If this partial cell should be discarded, assertion of TxSOC will clear this 'short' cell from the internal FIFO, and normal operation will resume.

Entering Loopback (Cell Mode)

Under UTOPIA specification, cell transfer is initiated via the TxCLAV control, which indicates that the transmission device can receive an entire 53 byte cell for transmission. Therefore, a complete cell will automatically be received and transmitted by the 77105, even after TxCLAV assertion is inhibited:

1. De-assert TxCLAV, using 0x02, Bit 7. As described above, under normal UTOPIA operation it is assumed that the remainder of the cell will continue to be shipped to the 77105.
2. After waiting for complete cell to be transmitted, enable desired loopback mode. If loopback is entered prior to complete cell receipt, the cell will be looped back.
3. Re-assert TxCLAV using 0x02, Bit 7.

Exiting Loopback (Byte and Cell Modes)

The same conditions and concerns exist for exiting loopback, as for entering these modes. Therefore, follow the above instructions, except replace step #2 with 'disable loopback mode'.

2. Counters

Several condition counters are provided to assist external systems (e.g. software drivers) in evaluating communications conditions. It is anticipated that these counters will be polled from time-to-time (user selectable) to evaluate performance.

- Symbol Error Counter
  - *8 bit counter*
  - *counts all undefined 5 bit symbols in received data stream*
- TxCell Counter
  - *16 bit*
  - *counts all transmitted cells*
- RxCell Counter
  - *16 bit counter*
  - *counts all received cells*
- Receive HEC Error Counter
  - *5 bit counter*
  - *counts all received HEC errors*

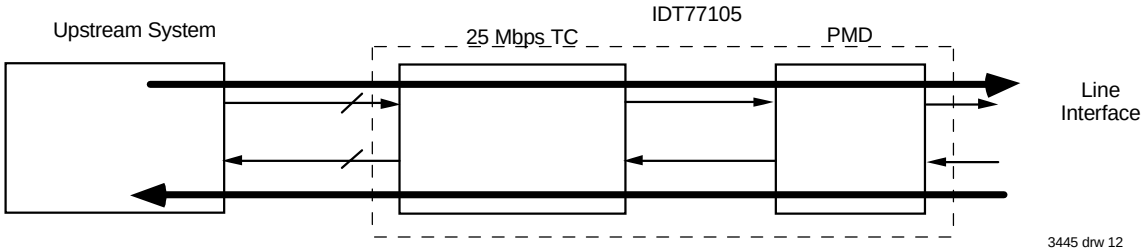


Figure 9 Normal Mode

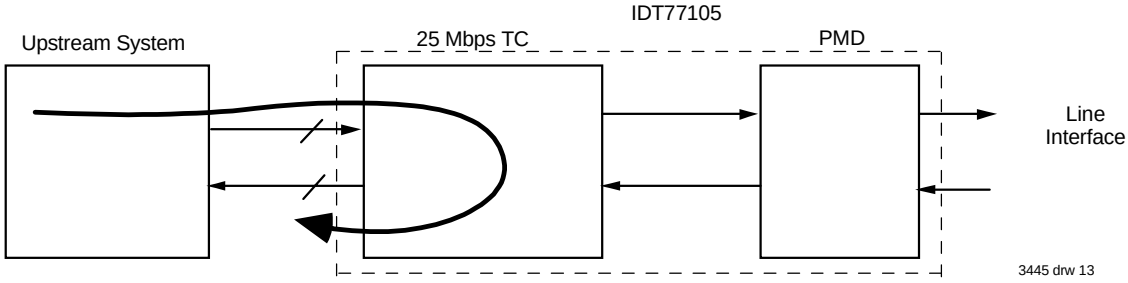


Figure 10 PHY Loopback

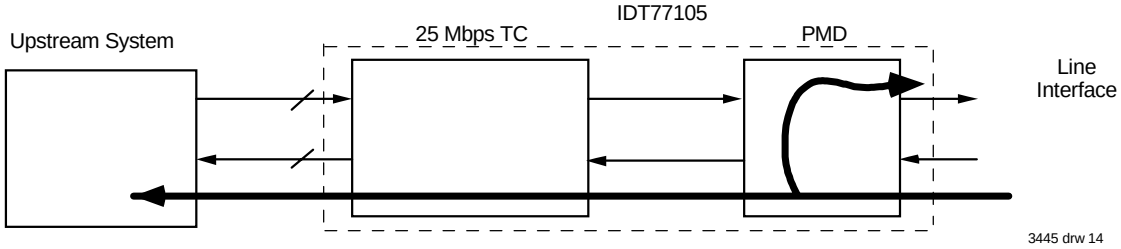


Figure 11 Line Loopback

The TxCell and RxCell counters are sized (16 bits) to provide a full cell count (without roll over) if the counter is read once/second. The Symbol Error counter and HEC Error counter were given sufficient size to indicate exact counts for low error-rate conditions. If these counters overflow, a gross condition is occurring, where additional counter resolution does not provide additional diagnostic benefit.

Reading Counters

1. Decide which counter value is desired. Write to register 0x06 to the bit location corresponding to the desired counter. This loads the Counter Read registers with the selected counter's value, and resets this counter to zero.

   Note: Only one counter (Selected bit in 0x06) may be enabled at any time.
2. Read registers 0x04 (low byte) and 0x05 (high byte) to get the value.

Further reads may be accomplished in the same manner by first writing to register 0x06.

Multi-Phy Operation

Multiple 77105's may be connected to a common bus when a multi-PHY system architecture is needed.

Both Transmit and Receive UTOPIA busses, as well as the utility bus, can attach to common busses.

Device selection is controlled via the UTOPIA "enable" control signals: TxEnb and RxEnb. In transmit, TxEnb tells the selected device that the data and control signals it sees are to be used for ATM cell transmission. In receive, when RxEnb is deasserted (high), RxData[7:0], RxParity, and RxSOC are all tri-stated, allowing them to share a common bus. When RxEnb is asserted, the selected device drives these outputs, transferring the data to the upstream hardware.

Note that while multiple transmit devices may be selected (e.g. for multicast) by asserting more than one TxEnb, multiple receive devices should not be enabled. Also, the output of RxRef is not affected by RxEnb; the same is also true for TxRef and TxEnb. These must be routed and/or multiplexed separately.

Figure 12 is an example of connecting multiple PHYs in the transmit direction. A separate TxEnb and TxClav signal is provided to each 77105 for device select.

Multi-Phy Receive is constructed in the same manner as transmit, in that each device has dedicated RxEnb and RxClav signals. (See Figure 13).

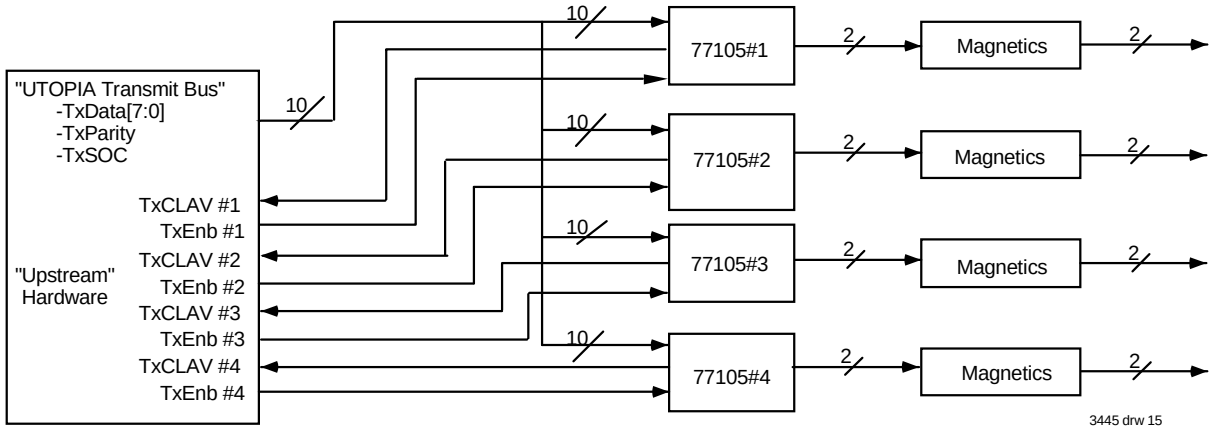


Figure 12 Multi-PHY: Transmit Example

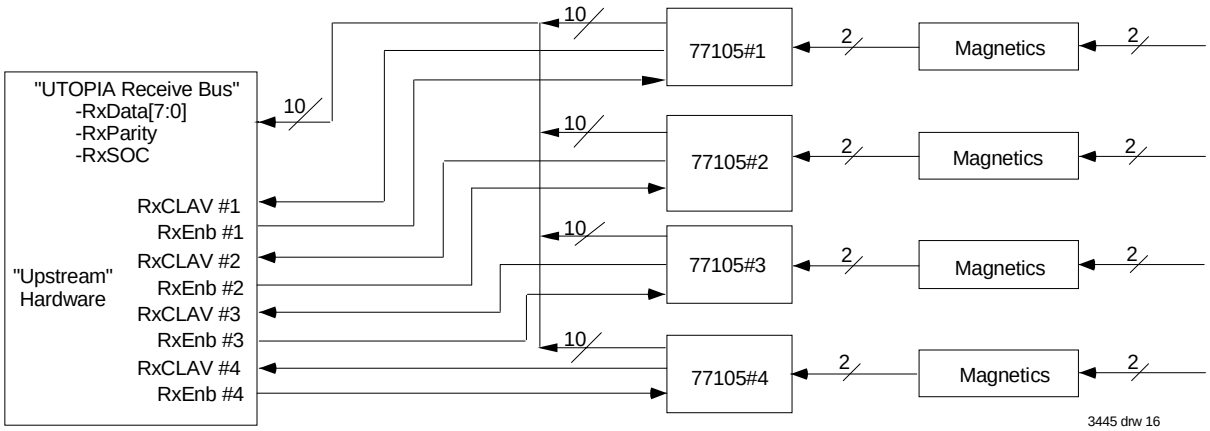


Figure 13 Multi-PHY Receive Example

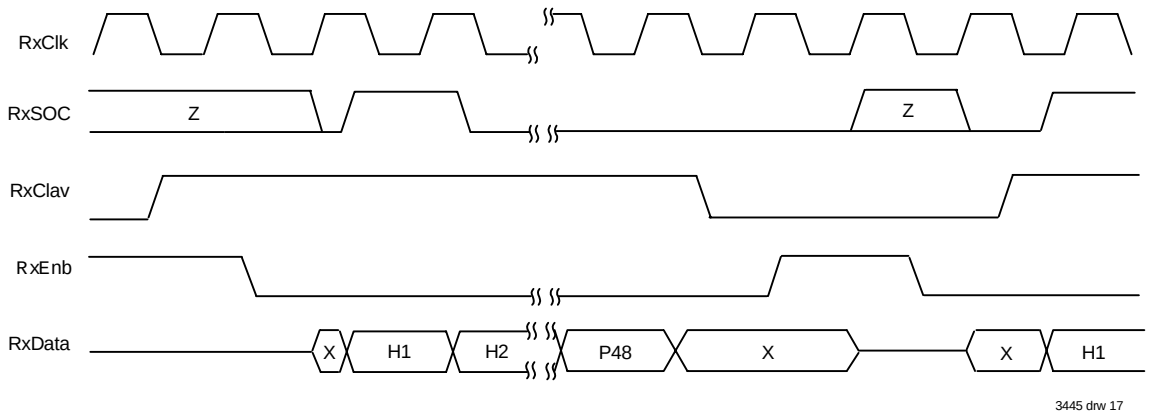


Figure 14 Multi-PHY Receive Waveform

PHY to Magnetics Interface

Figure 21 provides the appropriate connection scheme to the Magnetics Module. The set of values provided will ensure the return Loss specification is met.

Status and Control Register List

Nomenclature

R/W = register may be read and written via the utility bus;

R-only or W-only = register may be read-only or write-only via the utility bus;

sticky = register bit is cleared after the register containing it is read.

"0" = 'cleared' or 'not set'

"1" = 'set'

Master Control Register
Address: 0x00

Master	Type	Initial State	Function
Bit 7	R/W	0	**UPLO** Controls pin 11, User Programmable Output Latch. Note that the polarity of pin 11 is opposite the polarity of this register bit.
Bit 6	R/W	0 = disabled	**Discard Receive Error Cells** On receipt of any cell with an error (e.g. short cell, invalid symbol or HEC error (if enabled)), the cell will be discarded before entering the receive FIFO.
Bit 5	R/W	0 = disabled	**Enable Cell Error Interrupts Only** If Bit 0 in this register is set (Interrupts Enabled), setting of this bit enables only 'Received Cell Error' to trigger an interrupt. Received Cell Errors are: short cell, invalid symbol and HEC error.
Bit 4	R/W	0 = disabled	**Transmit Data Parity Check** Enable checking of TxData[7:0] parity against TxParity.
Bit 3	R/W	1 = enabled	**Discard Received Idle Cells** Enable discarding of received idle (VPI/VCI = 0) cells. There is no indication when such a discard takes place.
Bit 2	R/W	0 = disabled	**Halt Tx** Halts transmission of data and forces both TxD+/- signals to a logic low state.
Bit 1	R/W	0 = cell mode	**UTOPIA mode select:** 0 = cell mode, 1 = byte mode.
Bit 0	R/W	1 = enabled	**Enable Interrupt Pin (Interrupt Mask Bit)** Enables interrupt output pin. If cleared, INT (pin 53 is always high. If set, INT will drive low when an interrupt occurs.

Interrupt Status
Address: 0x01

Master	Type	Initial State	Function
Bit 7	—	—	Reserved
Bit 6	R	0 = Bad Signal	**Good Signal Bit** See definition on pages 10 and 11. 1 = Good Signal 0 = Bad Signal
Bit 5	sticky	0	**HEC Error** Interrupt sets when a HEC error is detected in a received cell.
Bit 4	sticky	0	**"Short Cell" Received** Interrupt signal which flags received cells with fewer than 53 bytes. This condition is detected by the TC receiving Start-of-Cell command bytes with fewer than 53 bytes between them.
Bit 3	sticky	0	**Transmit Parity Error** If Bit 4 of Register 0x00 is set (Transmit Data Parity Check), this interrupt flags a transmit data parity error condition. Odd parity is used.
Bit 2	sticky	0	**Receive signal Condition Change** This interrupt is set when the received 'signal' changes either from 'bad to good' or from 'good to bad'.
Bit 1	sticky	0	**Received** Symbol Error Set on receiving a cell with an undefined symbol.
Bit 0	sticky	0	**Receive FIFO Overrun** Interrupt sets to indicate when the receive FIFO has overflowed.

Diagnostic Control
Address: 0x02

Master	Type	Initial State	Function
Bit 7	R/W	0 = normal	**Force TxClav Deassert** Used during the loopback mode to prevent upstream system from continuing to send data to 77105.
Bit 6	R/W	0 = UTOPIA	**RxClav Operation Select** The UTOPIA standard dictates that during cell mode operation, if the receive FIFO no longer has a complete cell available for transfer from PHY, RxClav is deasserted following transfer of the last byte out of the PHY to the upstream system. With this bit set, early deassertion of this signal will occur at the end of Payload byte 44 (as in octet mode for TxFull). This provides early indication to the upstream system of this impending condition. "Standard UTOPIA RxClav" = 0 "Cell mode = Byte mode" = 1
Bit 5	R/W	0 = “multi-PHY”	**Single/Multi-PHY Configuration Select** 0 = Single-PHY mode: RxData, RxPrty and RxSOC never tri-state 1 = Multi-PHY mode: RxEnb = 1 then tri-state RxData, RxPrty, RxSOC
Bit 4	R/W	0 = normal	**RFLUSH = Clear Receive FIFO** This signal is used to tell the TC to flush (clear) all data in the receive FIFO. The TC signals this completion by clearing this bit.
Bit 3	R/W	0 = normal	**Insert Transmit Payload Error** Inserts cell payload errors in transmitted cells. This can be used to test error detection and recovery systems at destination station, or, under loopback control, the local receiving station. This payload error is generated by flipping bit 0 of the last cell payload byte.
Bit 2	R/W	0 = normal	**Insert Transmit HEC Error** Insert HEC error in Byte 5 of cell. This can be used to test error detection and recovery systems in down-stream switches, or, under loopback control, the local receiving station. This HEC error is generated by flipping bit 0 of the HEC byte.
Bit 1, 0	R/W	0 = normal	**Loopback Control** **bit# 1 0** 0 0 Normal mode (receive from network) 0 1 Reserved 1 0 PHY Loopback 1 1 Line Loopback

LED Driver and HEC Status/Control

Address: 0x03

Master	Type	Initial State	Function
Bit 7		0	Reserved
Bit 6	R/W	0 = enable	**Disable Receive HEC Checking (HEC Enable)** When not set, TC calculates HEC byte on first 4 bytes of received cell, and compares value against 5th byte with this HEC calculation result
Bit 5	R/W	0 = enable	**Disable Xmit HEC Calculate & Replace** Directs TC not to calculate HEC on first 4 bytes of cell queued for transmit and replace 5th byte with this HEC calculation result
Bit 4, 3	R/W	0 = 1 cycle	**RxRef pulse width select** **bit # . 4 3 .** 0 0 RxRef active for 1 RxClk cycle 0 1 RxRef active for 2 RxClk cycles0 1 0 RxRef active for 4 RxClk cycles 1 1 RxRef active for 8 RxClk cycles
Bit 2	R	1 = empty	FIFO Status 1 = TxFIFO empty 0 = TxFIFO not empty
Bit 1	R	0	TxLED Status 1 = Cell Transmitted 0 = Cell NOT Transmitted
Bit 0	R	0	RxLED Status 1 = Cell Received 0 = Cell NOT Received

Low Byte Counter Register [7:0]

Address: 0x04

Master	Type	Initial State	Function
Bit [7:0]	R	0x00	Provides low-byte of counter value selected via register 0x06.

High Byte Counter Register [15:8]

Address: 0x05

Master	Type	Initial State	Function
Bit [7:0]	R	0x00	Provides high-byte of counter value selected via register 0x06.

Counter Register Read Select

Note: Only one bit may set at any time for proper operation

Address: 0x06

Master	Type	Initial State	Function
Bit 7	—	—	Reserved
Bit 6	—	—	Reserved
Bit 5	—	—	Reserved
Bit 4	—	—	Reserved
Bit 3	W	0	Symbol Error Counter
Bit 2	W	0	TxCell Counter
Bit 1	W	0	RxCell Counter
Bit 0	W	0	Receive HEC Error Counter

LED Output

LED outputs are able to source and sink current, to enable driving two-color LEDs. The Tx and Rx LEDs are driven according to the following table:

	State	Pin Voltage
RxLED	Cells being received Cells not being received	Low High
RxLED	Cells being received Cells not being received	Low High

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 15

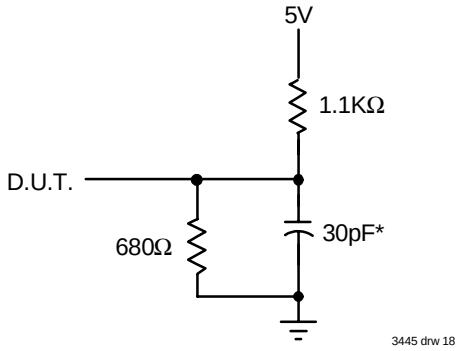


Figure 15 Output Load

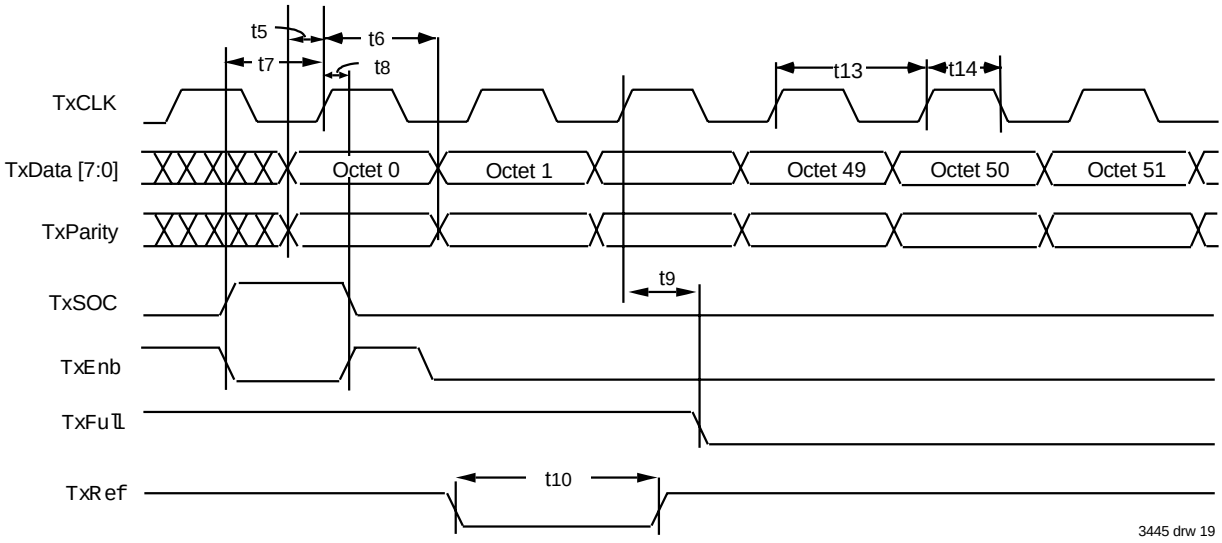


Figure 16 UTOPIA Transmit

UTOPIA Bus Timing Parameters

Symbol	Parameter	Min.	Max.	Unit
t1	RxEnb set up time to RxCLK	10	—	ns
t2	RxEnb hold time from RxCLK	2	—	ns
t3	tPD from RxCLK to RxSOC, RxData, and RxRef	3	10	ns
t4	RxEmpty delay from RxCLK	1	20	ns
t5	TxData[7:0], TxParity setup time to TxCLK	10	—	ns
t6	TxData[7:0], TxParity hold time from TxCLK	2	—	ns
t7	TxSOC, TxEnb setup time to TxCLK	10	—	ns
t8	TxSOC, TxEnb hold time from TxCLK	2	—	ns
t9	TxFull delay from TxCLK	1	20	ns
t10	TxRef pulse width	TxCLK Period +5ns	—	ns
t11	RxCLK period	30	400	ns
t12	RxCLK duty cycle (T of t11)	40	60	ns
t13	TxCLK period	30	400	ns
t14	TxCLK duty cycle (% of t13)	40	60	ns
t15	RxCLK to RxData [7:0], RxParity, and RxSOC low impedance	2	12	ns

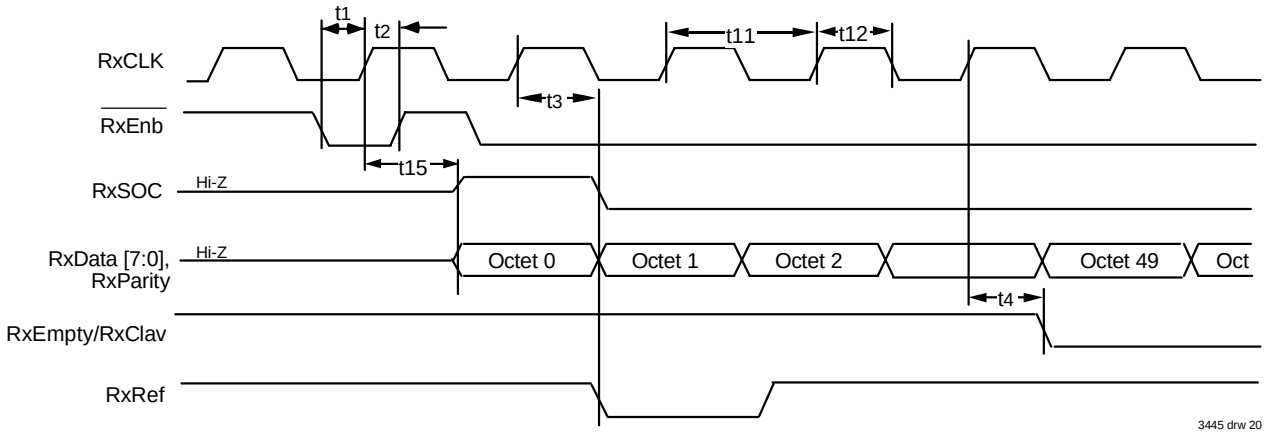


Figure 17 UTOPIA Receive

TxOSC and Reset Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
Tcyc	TxOSC frequency (25.6 Mbps)	31.5	32	32.5	MHz
Tch	TxOSC high duty cycle (% of Tcyc)	40	50	50	%
Tcl	TxOSC low duty cycle (% of Tcyc))	40	50	50	%
Trpw[1]	Minimum Resetpulse width	2* TxCLK period	—		
		2* RxCLK period	—		

1. Trpw must meet both minimum limits.

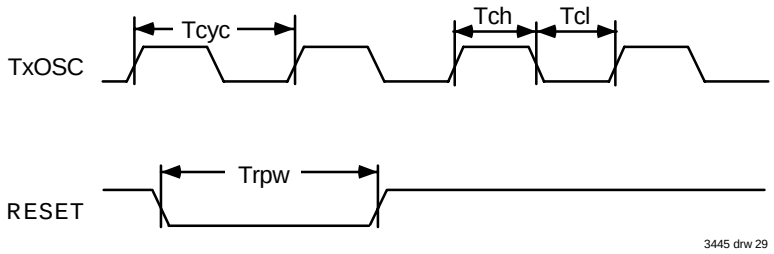


Figure 18 TxOSC and Reset Timing

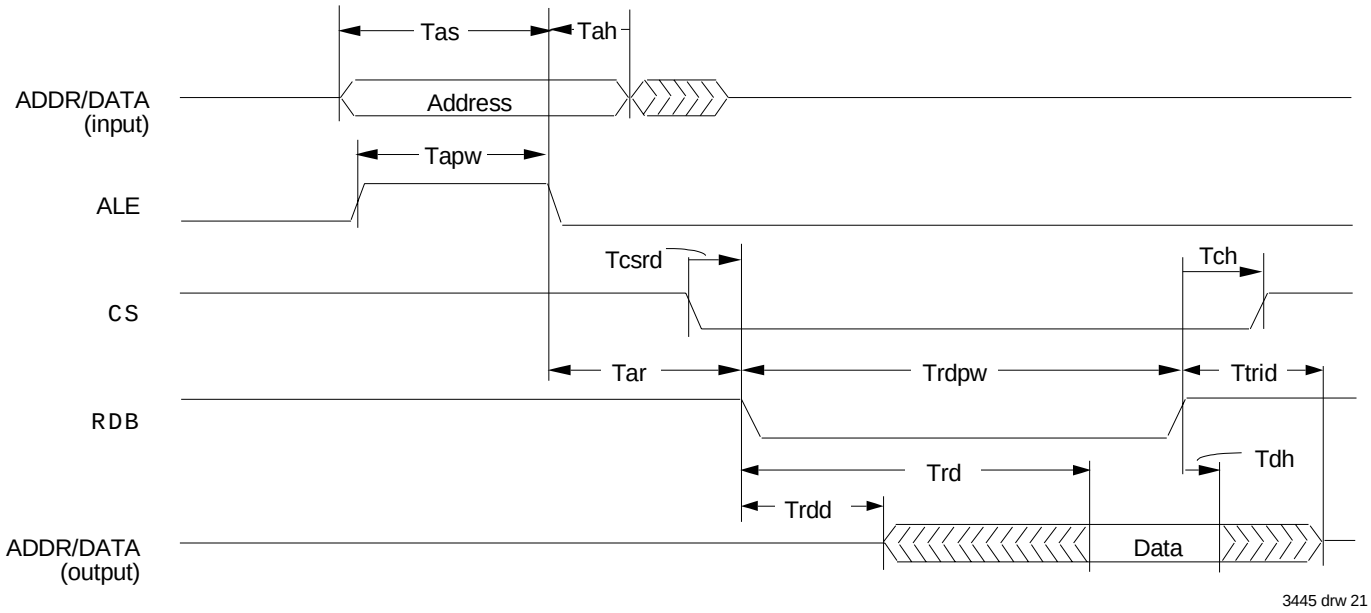


Figure 19 Utility Bus Read Cycle

Utility Bus Read Cycle

Name	Min.	Max.	Unit	Comment
Tas	10	—	ns	Address setup to ALE
Tcsrd	0	—	ns	Chip select to read enable
Tah	5	—	ns	Address hold to ALE
Tapw	10	—	ns	ALE min pulse width
Ttria	—	0	ns	Address tri-state to RDB assert
Trdpw	20	—	ns	Min. RDB pulse width
Tdh	0	—	ns	Data Valid hold time
Tch	0	—	ns	RDB deassert to CS deassert
Ttird	—	10	ns	RDB deassert to data tristate
Trd	5	18	ns	Read Data access
Tar	5	—	ns	ALE low to start of read
Trdd	0	—	ns	Start of read to Data low-Z

Utility Bus Write Cycle

Name	Min.	Max.	Unit	Comment
Tapw	10	—	ns	ALE min pulse width
Tas	10	—	ns	Address set up time to ALE
Tah	5	—	ns	Address hold time to ALE
Tcswr	0	—	ns	CS Assert to WRB
Twrpw	20	—	ns	Min. WRB pulse width
Tdws	20	—	ns	Write Data set up time
Tdwh	10	—	ns	Write Data hold time
Tch	0	—	ns	WRB deassert to CS deassert
Taw	20	—	ns	ALE low to end of write

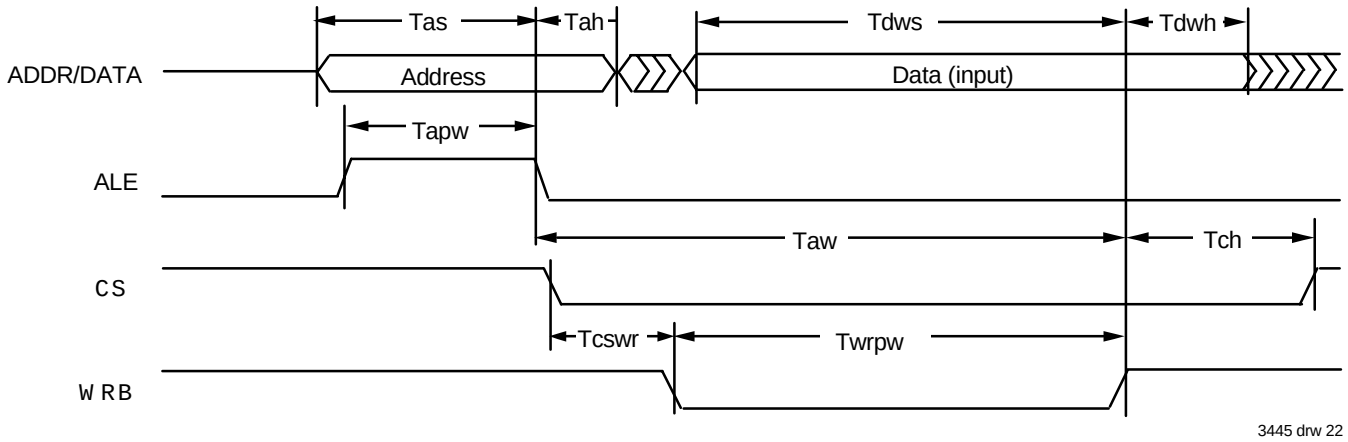


Figure 20 Utility Bus Write Cycle

Schematic for ATM User

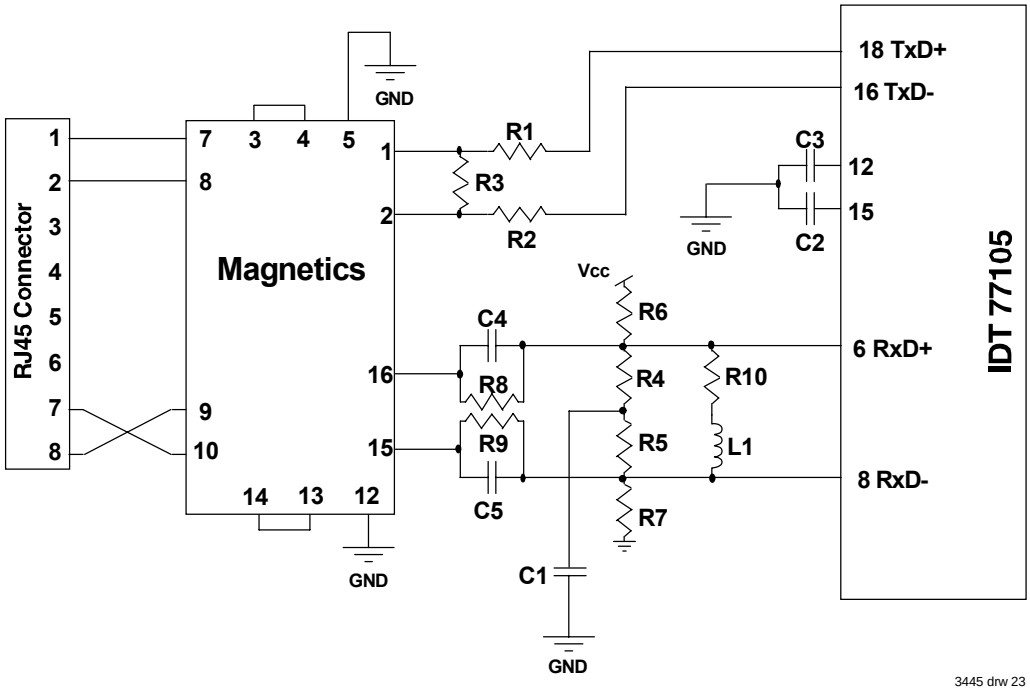


Figure 21

Note: 1. To configure for ATM network, refer to Figure 23.
2. Only the analog pins are shown on the IDT77105.
3. L1 should be TDK-NLC1210-3R3M or equivalent.

Analog Component Values

Component	Value	Tolerance
R1	82Ω	±10%
R2	82Ω	±10%
R3	267Ω	±10%
R4	55Ω	±10%
R5	55Ω	±10%
R6	5100Ω	±10%
R7	2000Ω	±10%
R8	33Ω	±10%
R9	33Ω	±10%
R10	82Ω	±10%
C1	.1µF	±20%
C2	120pF	±20%
C3	120pF	±20%
C4	470pF	±20%
C5	47 0pF	±20%
L1	3.3µH	±20%

Magnetics Modules for 25 Mbps

Pulse PE-67583	(610) 674-8100
TDK TLA-6M103	(847) 803-6100

A note about Figures 22 and 23: The ATM Forum and ITU-T standards for 25 Mbps ATM define "Network" and "User" interfaces. They are identical except that transmit and receive are switched between the two. A Network device can be connected directly to a User device with a straight-through cable. User-to-User or Network-to-Network connections require a cable with 1-to-7 and 2-to-8 crossovers.˜

PC Board Layout for ATM Network

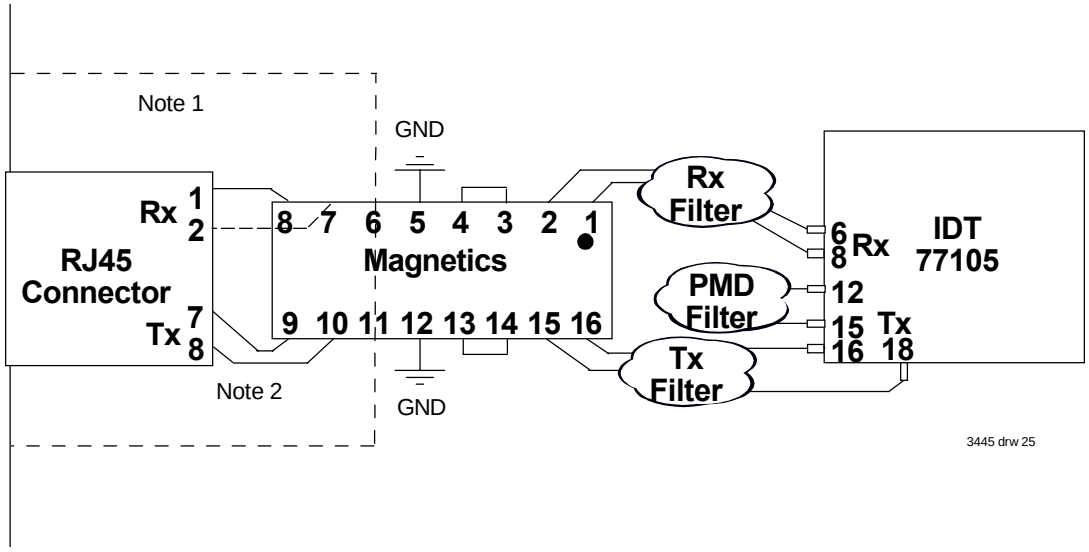


Figure 22

Note: 1.No power or ground plane inside this area.
2. All analog signal traces should avoid 90° corners.

PC Board Layout for ATM User

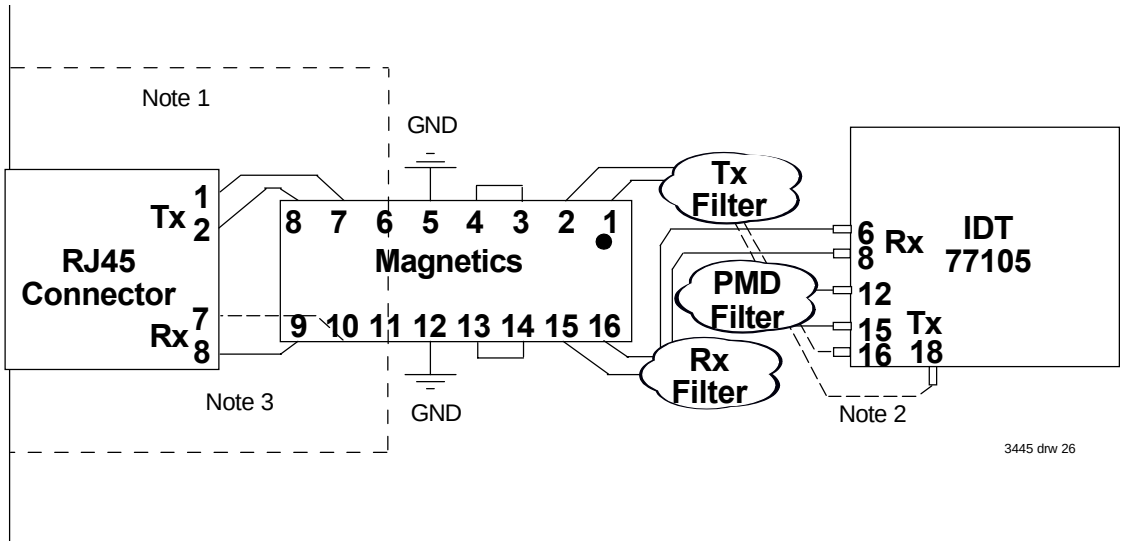
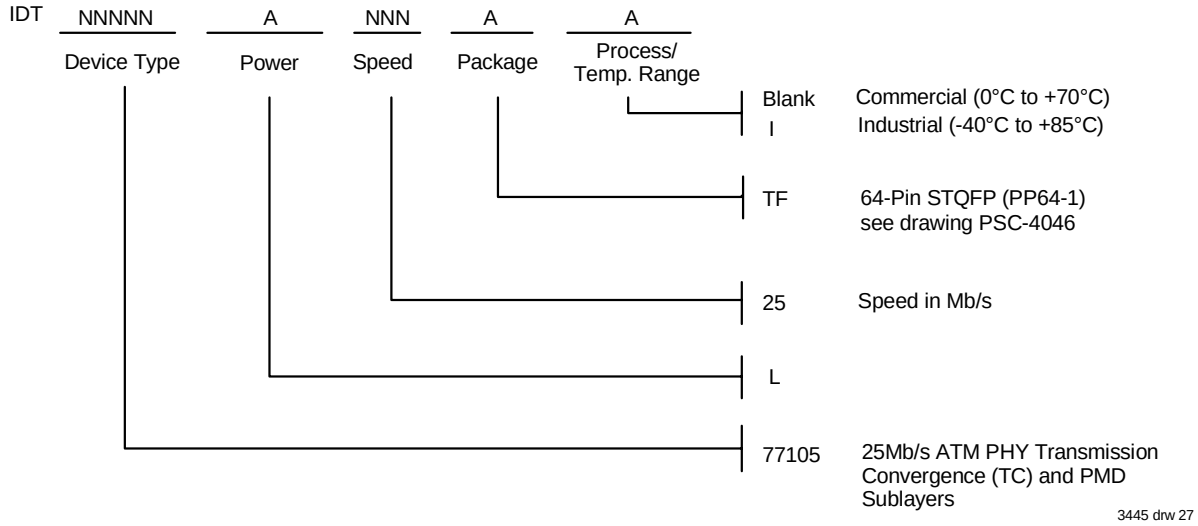


Figure 23

Note: 1. No power of ground plane inside this area.
2.Dotted signal traces (Tx) should be run on the back side of the PC Board.
3.All analog signal traces should avoid 90° corners.

Ordering Information



Revision History

9/8/95:	Initial Draft
9/13/95:	Revision
9/21/95:	Revision
10/30/05:	Corrected Typographical Errors
11/13/95:	Corrected Vcc and GND nomenclature and Figure 10
1/9/96:	Made Preliminary, added PCB layouts and package mechanical diagram
5/6/96:	Changed the capacitor values see Analog Component Values on page 22 (C2 and C3) and the pin for C3 on the diagram (page 22). Exchanged the Tx and Rx filters on PC board layout for ATM user.
7/31/96:	Corrected Board layouts and timing specs, added multi-PHY waveforms.
9/16/96:	Corrected Fig. 6, added note for utopia speed, corrected Counter Reg. Read Select table to write only, added Input and Output line signal tables.
11/26/96:	Added definition for Good Signal bit in the Interrupt Register (address 0x01) and information regarding cable disconnect and link establishment, component values changed on reference design to accommodate standard values.
2/23/98:	Addition of Industrial temperature grade. Additional timing parameters for RESET and UTOPIA bus. Deleted references to 77101. Added specification relating AVcc to Vcc. UPLO description improved. Additions to transmit and receive text.
12/21/98:	Add statements on standards compliance. Add timing parameters to utility bus read and write cycles (Figures 19 and 20). Correction to reset timing waveform (Figure 18). Revision to recommended 77105/magnetics interface (Figure 21) and component values. Add list of compatible magnetics. Corrections to Figures 7 and 17. Return loss information removed. Eliminate distinction between analog and digital power and ground pins. 51.2 Mbps operation added. TOSC specifications added.
6/21/00:	Updated to new format. Removed 51.2 Mbps operation. Remove more references to analog Vcc and ground. Misc. typos corrected.
9/11/00	Removed references to 77V101. Removed section Magnetics Modules for 51 Mbps.

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-330-1748
www.idt.com

for Tech Support:
email: atmhelp@idt.com
phone: 408-492-8208