

## CMOS 4-BIT MICROCONTROLLER

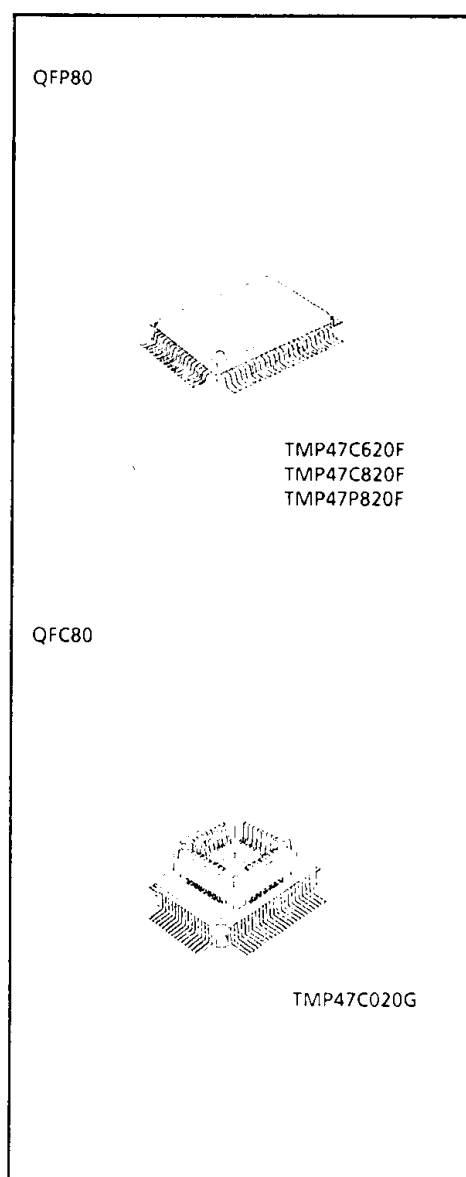
## TMP47C620F, TMP47C820F

The 47C620/820 are high speed and high performance 4-bit single chip microcomputers based on the TLC5470 series with a LCD driver and high speed timer/counters.

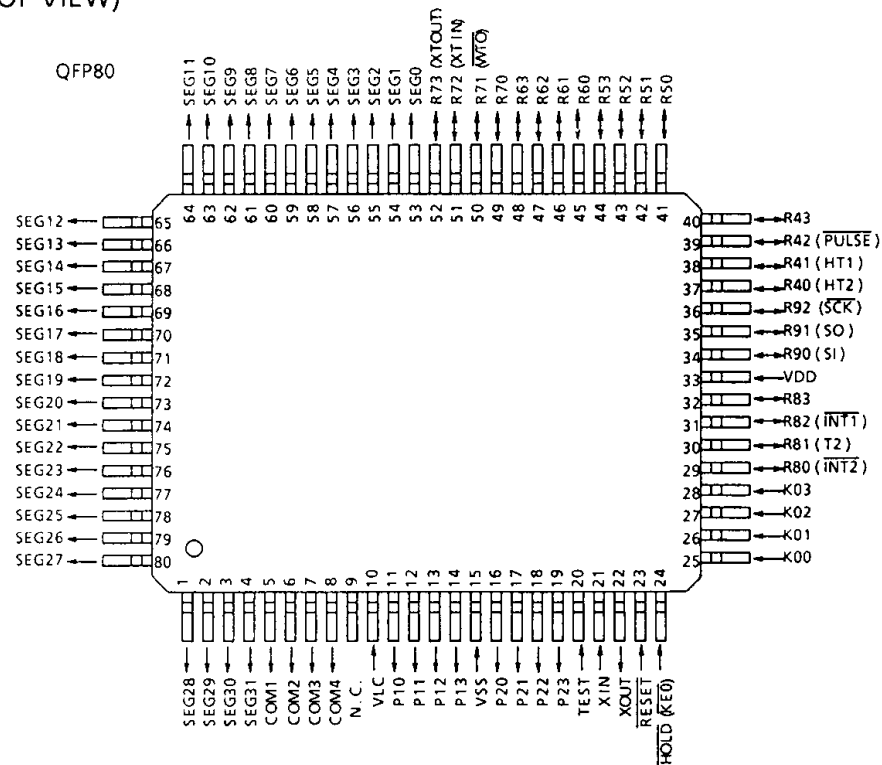
| PART No.   | ROM          | RAM         | PACKAGE | OTP version | PIGGYBACK  |
|------------|--------------|-------------|---------|-------------|------------|
| TMP47C620F | 6144 × 8-bit | 384 × 4-bit | QFP80   | TMP47P820F  | TMP47C020G |
| TMP47C820F | 8192 × 8-bit | 512 × 4-bit |         |             |            |

## FEATURES

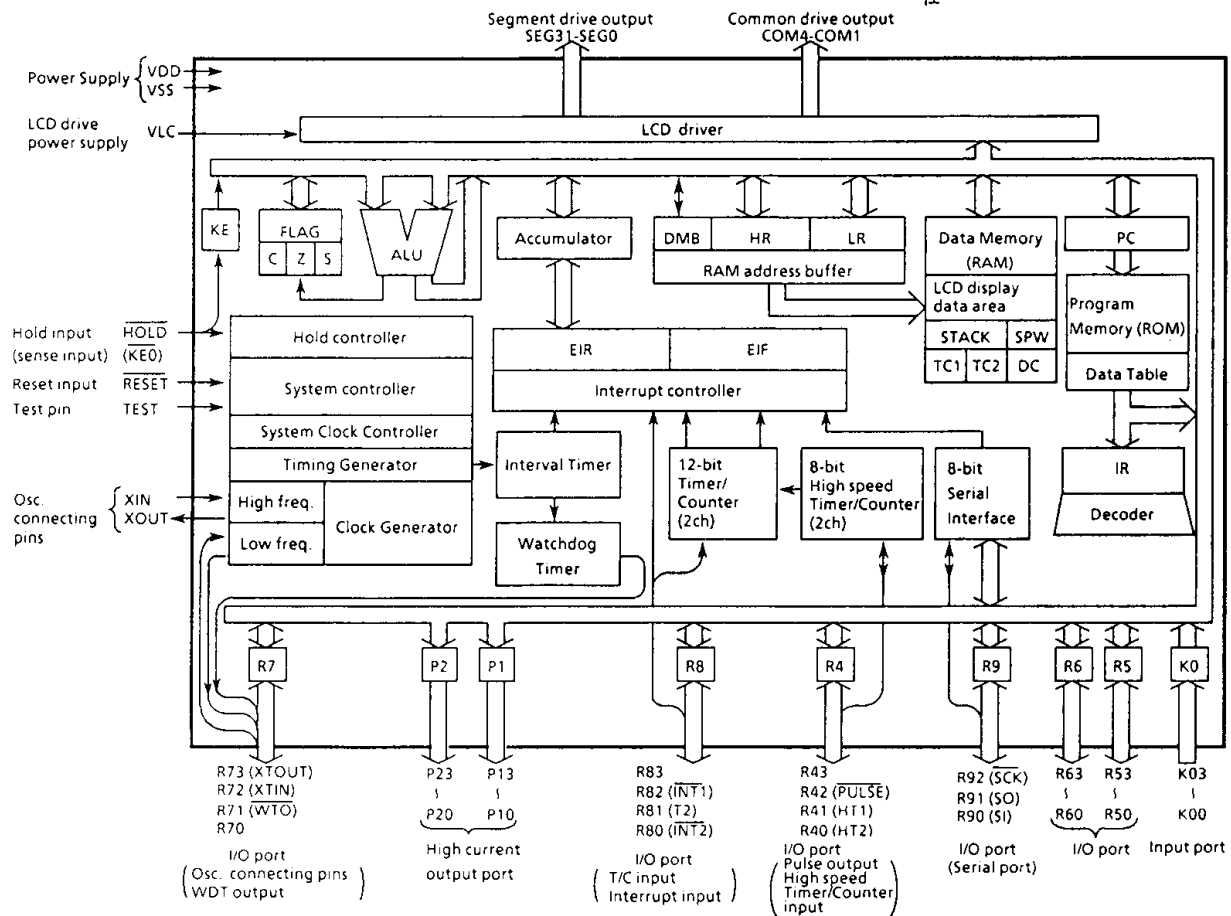
- ◆ 4-bit single chip microcomputer
- ◆ Instruction execution time :
  - 1.3μs (at 6MHz), 244μs (at 32.8KHz)
- ◆ 92 basic instructions
  - Table look-up instructions
  - 5-bit to 8-bit data conversion instruction
- ◆ Subroutine nesting : 15 levels max.
- ◆ 6 interrupt sources (External : 2, Internal : 4)
  - All sources have independent latches each, and multiple interrupt control is available.
- ◆ I/O port (36 pins)
  - Input     2 ports     5 pins
  - Output   2 ports     8 pins
  - I/O       6 ports     23 pins
- ◆ Interval Timer
- ◆ Two 12-bit Timer/Counters
  - Timer, event counter, and pulse width measurement mode
- ◆ Two 8-bit High speed Timer/Counters
  - Timer, event counter, frequency measurement, and pulse output mode
- ◆ Watchdog Timer
- ◆ Serial Interface with 8-bit buffer
  - Simultaneous transmission and reception capability.
  - External/internal clock, leading/trailing edge, and 4/8-bit mode
- ◆ High current outputs
  - LED direct drive capability (typ. 10mA × 8bits)
- ◆ LCD driver
  - LCD direct drive capability (max. 16-digit display at 1/4 duty LCD)
  - 1/4, 1/3 1/2 duties or static drive are programmably selectable.
- ◆ Dual-clock operation
  - High-speed/Low-power consumption operating mode
- ◆ Hold function
  - Battery/Capacitor back-up
- ◆ Real Time Emulator : BM47C820A



## PIN ASSIGNMENT (TOP VIEW)



## BLOCK DIAGRAM



## PIN FUNCTION

| PIN NAME     | Input/Output  | FUNCTIONS                                                                                                                 |                                                               |
|--------------|---------------|---------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------|
| K03 - K00    | Input         | 4-bit input port                                                                                                          |                                                               |
| P13 - P10    | Output        | 4-bit output port with latch.                                                                                             |                                                               |
| P23 - P20    |               | 8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL].                                       |                                                               |
| R43          | I/O           | 4-bit I/O port with latch.                                                                                                |                                                               |
| R42 (PULSE)  | I/O (Output)  | When used as input port or high speed Time/Counter, the latch must be set to "1".                                         | Pulse output (High speed T/C2)                                |
| R41 (HT1)    | I/O (Input)   |                                                                                                                           | High speed Timer/Counter 1 input                              |
| R40 (HT2)    |               |                                                                                                                           | High speed Timer/Counter 2 input                              |
| R53 - R50    | I/O           | 4-bit I/O port with latch.                                                                                                |                                                               |
| R63 - R60    |               | When used as input port, the latch must be set to "1".                                                                    |                                                               |
| R73 (XTOUT)  | I/O (Output)  | 4-bit I/O port with latch.                                                                                                | Resonator connecting pins.                                    |
| R72 (XTIN)   | I/O (Input)   | When used as input port, watchdog timer output, the latch must be set to "1".                                             | For inputting external clock, XIN is used and XOUT is opened. |
| R71 (WTO)    | I/O (Output)  |                                                                                                                           | Watchdog timer output                                         |
| R70          | I/O           |                                                                                                                           |                                                               |
| R83          | I/O           | 4-bit I/O port with latch.                                                                                                |                                                               |
| R82 (INT1)   | I/O (Input)   | When used as input port, external interrupt input pin, or Timer/Counter external input pin, the latch must be set to "1". | External interrupt 1 input                                    |
| R81 (T2)     |               |                                                                                                                           | Timer/Counter 2 external input                                |
| R80 (INT2)   |               |                                                                                                                           | External interrupt 2 input                                    |
| R92 (SCK)    | I/O (I/O)     | 3-bit I/O port with latch.                                                                                                | Serial clock I/O                                              |
| R91 (SO)     | I/O (Output)  | When used as input port, serial port the latch must be set to "1".                                                        | Serial data output                                            |
| R90 (SI)     | I/O (Input)   |                                                                                                                           | Serial data input                                             |
| SEG31 - SEG0 | Output        | LCD Segment drive output                                                                                                  |                                                               |
| COM4 - COM1  |               | LCD Common drive output                                                                                                   |                                                               |
| XIN          | Input         | Resonator connecting pins (high-frequency) .                                                                              |                                                               |
| XOUT         | Output        | For inputting external clock, XIN is used and XOUT is opened.                                                             |                                                               |
| RESET        | Input         | Reset signal input                                                                                                        |                                                               |
| HOLD (KE0)   | Input (Input) | Hold request/ release signal input                                                                                        | Sense input                                                   |
| TEST         | Input         | Test pin for out-going test. Be opened or fixed to low level.                                                             |                                                               |
| VDD          | Power supply  | + 5V                                                                                                                      |                                                               |
| VSS          |               | 0V (GND)                                                                                                                  |                                                               |
| VLC          |               | LCD drive power supply                                                                                                    |                                                               |

## OPERATIONAL DESCRIPTION

Concerning the 47C620/820 the configuration and functions of hardwares are described. As the description has been provided with priority on those parts differing from the 47C660/860, the technical data sheets for the 47C660/860 shall also be referred to.

### 1. SYSTEM CONFIGURATION

- (1) I/O Port
- (2) High speed Timer/Counter
- (3) LCD Driver

### 2. PERIPHERAL HARDWARE FUNCTION

#### 2.1 I/O Ports

The 47C620/820 have 10 I/O ports (36 pins) each as follows.

- (1) K0 ; 4-bit input
- (2) P1, P2 ; 4-bit output
- (3) R4 ; 4-bit input/output (shared with high speed timer/counter input and pulse output)
- (4) R5, R6 ; 4-bit input/output
- (5) R7 ; 4-bit input/output (shared with the Low-frequency resonator connecting pin and the Watchdog timer output)
- (6) R8 ; 4-bit input/output (shared with external interrupt and timer/counter input)
- (7) R9 ; 3-bit input/output (shared with serial port)
- (8) KE ; 1-bit sense input (shared with hold request/release signal input)

The description has been provide with priority on ports (3 and 6) changed from 47C800.

Table2-1 lists the port address assignments and the I/O instruction that can access the ports.

##### (1) Port R4 (R43-R40)

Port R4 is a 4-bit I/O port with output latch. The latch should be set to "1" for use as an input port. During reset, the latch is initialized to "1".

The R4 port is shared with the high speed Timer/Counter input pin and pulse output pin. The latches should be set to "1" when these pins are used for these functions. When used for normal I/O, the high speed Timer/Counter event counter mode, frequency measurement mode and pulse output mode should be disabled.

Port R4 (Port address OP04 / IP04)

| 3   | 2              | 1            | 0            |
|-----|----------------|--------------|--------------|
| R43 | R42<br>(PULSE) | R41<br>(HT1) | R40<br>(HT2) |

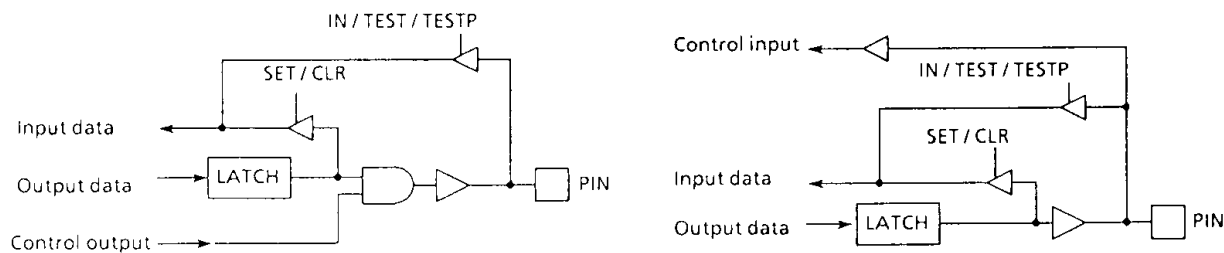


Figure 2-1. port R4

##### (2) R83 pin

Port R8 is shared with external interrupt input and Timer/Counter input. Timer/Counter 1 is connected to HTC1 ; therefore, there is no Timer/Counter 1 external input pin (TC1).

| Port Address<br>(**) | Port                                 |                                  | Input/Output instructions |                          |            |            |                        |                           |                             |
|----------------------|--------------------------------------|----------------------------------|---------------------------|--------------------------|------------|------------|------------------------|---------------------------|-----------------------------|
|                      | Input (IP**)                         | Output (OP**)                    | IN %p, A<br>IN %p, @HL    | OUT A, %p<br>OUT @HL, %p | OUT #k, %p | OUTB @HL   | SET %p, b<br>CLR %p, b | TEST %p, b<br>TESTP %p, b | SET @L<br>CLR @L<br>TEST @L |
| 00H                  | K0 input port                        | —                                | ○                         | —                        | —          | —          | —                      | ○                         | —                           |
| 01                   | P1 output latch                      | P1 output port                   | ○                         | —                        | —          | ○ (Note 2) | —                      | ○                         | —                           |
| 02                   | P2 output latch                      | P2 output port                   | ○                         | —                        | —          | ○          | —                      | ○                         | —                           |
| 03                   | —                                    | —                                | —                         | —                        | —          | —          | —                      | —                         | —                           |
| 04                   | R4 input port (HTC input)            | R4 output port (PULSE OUTPUT)    | ○                         | —                        | —          | —          | —                      | ○                         | ○                           |
| 05                   | R5 input port                        | R5 output port                   | ○                         | —                        | —          | —          | —                      | ○                         | ○                           |
| 06                   | R6 input port                        | R6 output port                   | ○                         | —                        | —          | —          | —                      | ○                         | ○                           |
| 07                   | R7 input port                        | R7 output port                   | ○                         | —                        | —          | —          | —                      | ○                         | ○                           |
| 08                   | R8 input port                        | R8 output port                   | ○                         | —                        | —          | —          | —                      | ○                         | ○                           |
| 09                   | R9 input port                        | R9 output port                   | ○                         | —                        | —          | —          | —                      | ○                         | ○                           |
| 0A                   | —                                    | —                                | —                         | —                        | —          | —          | —                      | —                         | —                           |
| 0B                   | —                                    | —                                | —                         | —                        | —          | —          | —                      | —                         | —                           |
| 0C                   | HTC1 counter                         | HTC1 register                    | ○                         | —                        | —          | —          | —                      | —                         | —                           |
| 0D                   | HTC2 counter                         | HTC2 register                    | ○                         | —                        | —          | —          | —                      | —                         | —                           |
| 0E                   | SIO, clock generator and Hold status | —                                | ○                         | —                        | —          | —          | —                      | ○                         | —                           |
| 0F                   | Serial receive buffer                | Serial transmit buffer           | ○                         | —                        | ○          | —          | —                      | —                         | —                           |
| 10H                  | Undefined                            | Hold operating mode control      | —                         | ○                        | —          | —          | —                      | —                         | —                           |
| 11                   | Undefined                            | —                                | —                         | —                        | —          | —          | —                      | —                         | —                           |
| 12                   | Undefined                            | —                                | —                         | —                        | —          | —          | —                      | —                         | —                           |
| 13                   | Undefined                            | —                                | —                         | —                        | —          | —          | —                      | —                         | —                           |
| 14                   | Undefined                            | —                                | —                         | —                        | —          | —          | —                      | —                         | —                           |
| 15                   | Undefined                            | Watchdog Timer control           | —                         | ○                        | —          | —          | —                      | —                         | —                           |
| 16                   | Undefined                            | System clock control             | —                         | ○                        | —          | —          | —                      | —                         | —                           |
| 17                   | Undefined                            | HTC1 control                     | —                         | ○                        | —          | —          | —                      | —                         | —                           |
| 18                   | Undefined                            | HTC2 control                     | —                         | ○                        | —          | —          | —                      | —                         | —                           |
| 19                   | Undefined                            | Interval Timer interrupt control | —                         | ○                        | —          | —          | —                      | —                         | —                           |
| 1A                   | Undefined                            | LCD driver control 1             | —                         | ○                        | —          | —          | —                      | —                         | —                           |
| 1B                   | Undefined                            | LCD driver control 2             | —                         | ○                        | —          | —          | —                      | —                         | —                           |
| 1C                   | Undefined                            | Timer/Counter 1 control          | —                         | ○                        | —          | —          | —                      | —                         | —                           |
| 1D                   | Undefined                            | Timer/Counter 2 control          | —                         | ○                        | —          | —          | —                      | —                         | —                           |
| 1E                   | Undefined                            | Serial interface control 1       | —                         | ○                        | —          | —          | —                      | —                         | —                           |
| 1F                   | Undefined                            | Serial interface control 2       | —                         | ○                        | —          | —          | —                      | —                         | —                           |

Note1. "—" means the reserved state. Unavailable for the user programs.

Note2. The 5-bit to 8-bit data conversion instruction [OUTB @HL], automatic access to ports P1 and P2.

Table 2-1. Port Address Assignments and Available I/O Instructions

## 2.2 High Speed Timer/Counter (HTC1, HTC2)

The 47C620/820 have two 8-bit high speed timer/counters for counting times or events. The event counter mode, timer mode, frequency measurement mode, and pulse output mode can be selected for the high speed timer/counters (HTC1 and HTC2).

The HTC1 can also be operated in conjunction with TC1 as a 20-bit counter. HTC2 can also output pulses. External input pins HT1 and HT2 are shared with ports R41 and R40. Pulse output pin (PULSE) is shared with port R42, the corresponding R4 output latch should be set to "1" when used as external input pins and pulse output pin. R41 can be used as the normal input/output pin when HTC1 is used in the timer mode, and R40 can be used as the normal input/output pin when HTC2 is used in the pulse output mode.

### 2.2.1 Circuit configuration

The high speed timer/counter consists of 8-bit binary counter, preset register and clock source selector.

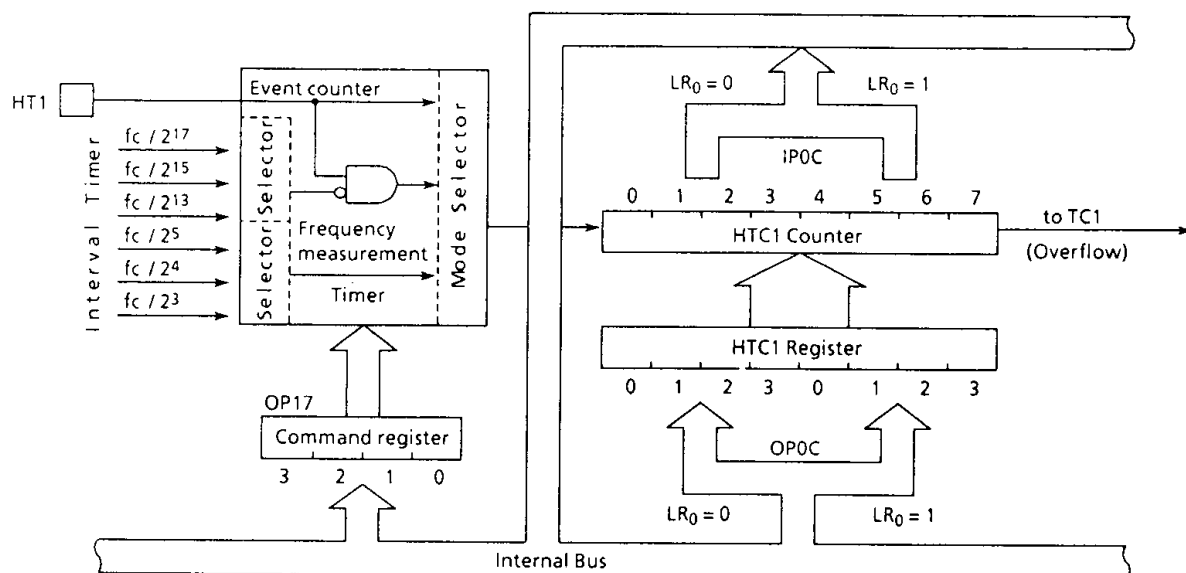


Figure 2.2. High Speed Timer/Counter 1

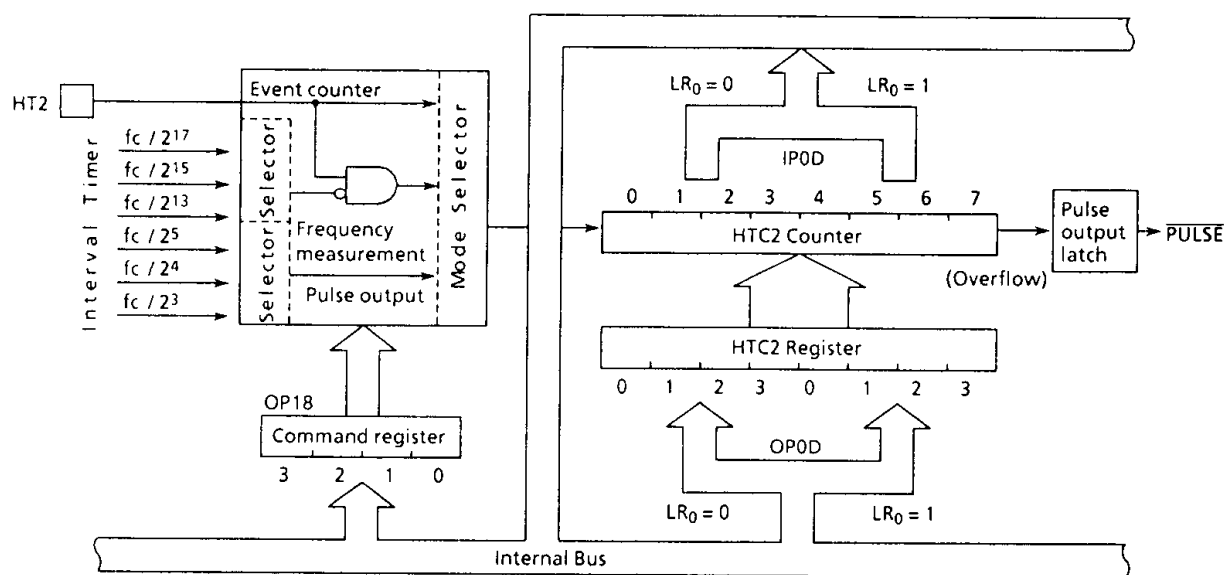
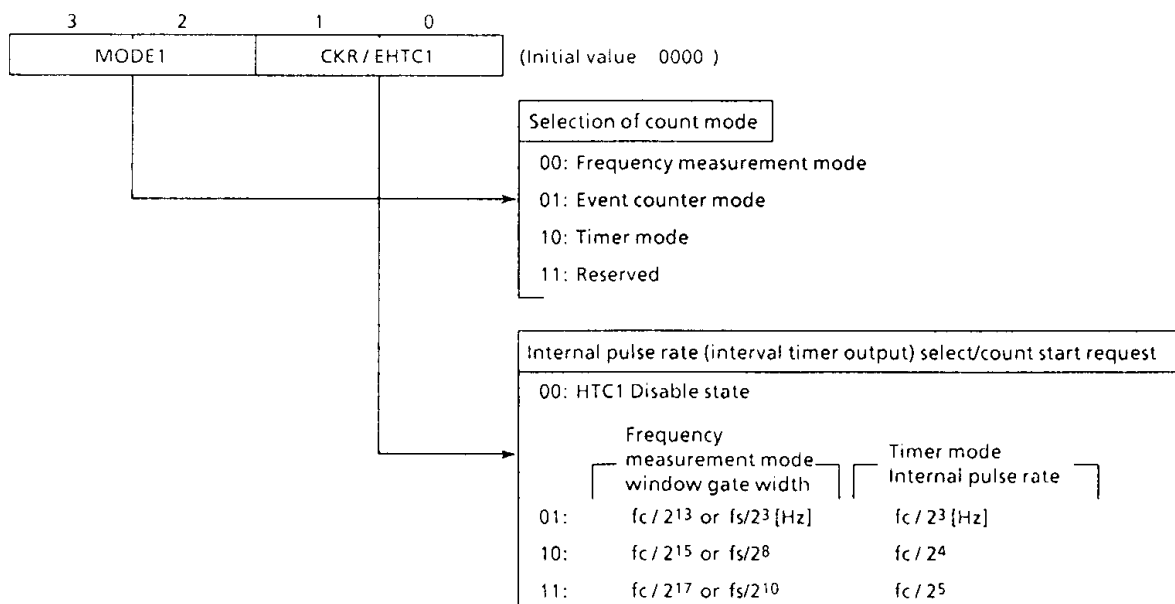


Figure 2.3. High Speed Timer/Counter 2

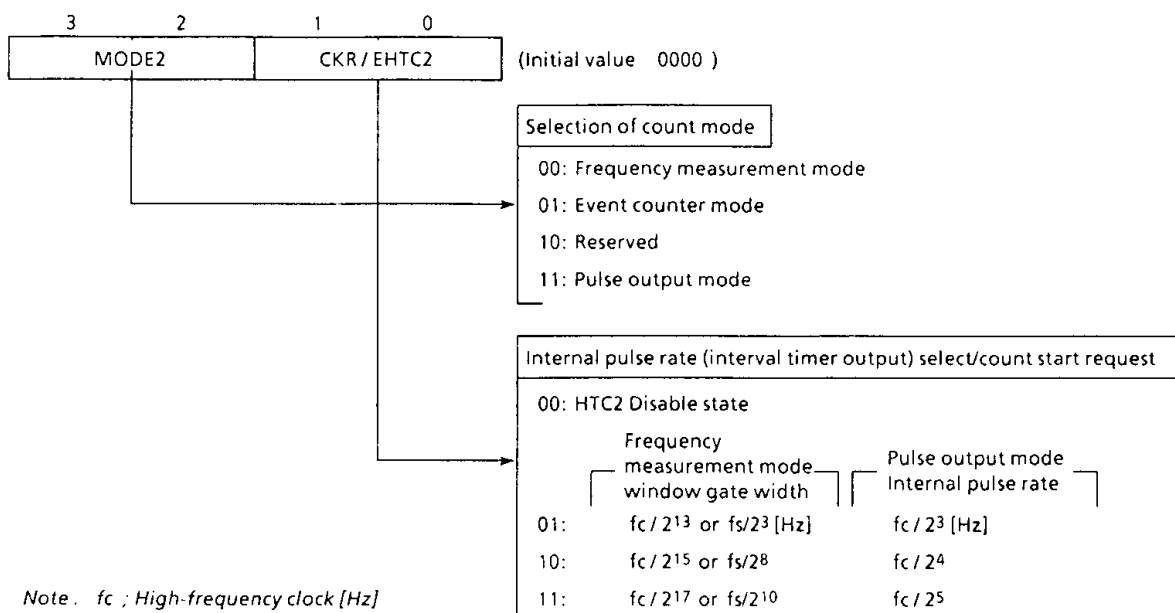
### 2.2.2 Control of High Speed Timer/Counter

The High Speed Timer/Counter is controlled by the command registers (OP17, OP18). These registers are initialized to "0" during reset.

HTC1 control command register (Port address OP17)



HTC2 control Command register (Port address OP18)



Note.  $f_c$  ; High-frequency clock [Hz]  
 $f_s$  ; Low-frequency clock [Hz]

Figure 2-4. HTC1, HTC2 control Command register

### 2.2.3 Function of High Speed Timer/Counter

The High Speed Timer/Counters (HTC1 and HTC2) consist of presettable 8-bit binary counters and clock source selectors. Either internal or external pulses can be selected by command register as the clock source for the event counter, timer, frequency measurement and pulse output modes. HTC1 and HTC2 increment at the rising edges of the clock pulses. Counting starts at the first rise of the clock pulse after a command is loaded into the command register.

#### (1) Setting of preset value

Values can be preset in the 8-bit binary counter. Values can be loaded to the binary counter when counting starts or when an overflow occurs by writing them to the HTC1 and HTC2 registers. Thus, preset values can be changed when the next overflow occurs by writing them during counting. Port addresses OP0C and OP0D are used for writing preset values as shown in Table 2-2. Preset values are written to the lower 4 bits when LR<sub>0</sub> (bit 0 of L register) = 0 and to the upper 4 bits when LR<sub>0</sub> = 1. The register is initialized to "0" during reset.

| Port address | LR <sub>0</sub> | Access register                   |
|--------------|-----------------|-----------------------------------|
| OP0C         | 0               | The Lower 4-bits of HTC1 register |
|              | 1               | The upper 4-bits of HTC1 register |
| OP0D         | 0               | The Lower 4-bits of HTC2 register |
|              | 1               | The upper 4-bits of HTC2 register |

Table 2-2. Writing of preset value

#### (2) Reading of Count Value

Count values of the 8-bit binary counter are read out from port addresses IP0C and IP0D as shown in Table 2-3. The lower 4 bits are read out when LR<sub>0</sub> = 0 and the upper 4 bits are read out when LR<sub>0</sub> = 1. Read out is unstable during counting, so stop counting before reading out. The counter is initialized to "0" during reset.

| Port address | LR <sub>0</sub> | Reading count values             |
|--------------|-----------------|----------------------------------|
| IP0C         | 0               | The Lower 4-bits of HTC1 counter |
|              | 1               | The upper 4-bits of HTC1 counter |
| IP0D         | 0               | The Lower 4-bits of HTC2 counter |
|              | 1               | The upper 4-bits of HTC2 counter |

Table 2-3. Reading of count value

#### (3) 20-bit Counter Function

The HTC1 counter is connected to TC1 (12-bit Timer/Counter) and can operate as 20-bit counter when TC1 is set to the event counter mode. In this case, TC1 increments when HTC1 overflows. The TC1 input (T1) is connected to HTC1 and can only be used as an event counter when set to the event counter mode (linked to HTC1) or a timer when set to the timer mode.

When used as a 20-bit counter in the timer, event counter and frequency measurement mode described later, the HTC1 tends to overflow more often when applied frequencies are high and preset values are large; therefore, there may be counting errors. Consequently, it is necessary to set the applied frequency and preset value so that HTC1 overflows occur at the rate of no more than once per 8 instruction cycles.

## 2.2.4 Function of High Speed Timer/Counter

### (1) Event counter mode

The counter increments for each rising edge of the external pin (HT1, HT2) input. The maximum applied frequency for HT1 and HT2 is  $f_c$  [Hz].

Example : Reading count values and Enable of Event Count mode

```
LD      A, #0100B      ; Sets the Event count mode of HTC2
OUT     A, %OP18
:
LD      A, #0000B      ; Stops the Event counter mode of HTC2
OUT     A, %OP18
LD      HL, #50H       ; RAM [50H] ← Lower 4-bit by HTC2 register
IN      %IP0D, @HL
INC     L               ; RAM [51H] ← Upper 4-bit by HTC2 register
IN      %IP0D, @HL
```

### (2) Timer mode (HTC1)

The counter increments at the rising edges of internal pulses generated by the interval timer. Three different internal pulse rates can be selected using the command register. HTC1 is connected to TC1; therefore, optional high-resolution times can be obtained by loading the initial values into the HTC1 register (OP0C) or TC1 counter register (addresses F4-F6H of DMB0) and generating overflow interrupt of TC1.

Example : After setting preset value, sets the timer mode of HTC1 and the Event Counter mode of TC1.

```
LD      L, #0000B      ; LR0 ← 0
OUT     #5H, %OP0C     ; Sets "5" in Lower 4-bit of HTC1 register
LD      L, #0001B      ; LR0 ← 1
OUT     #0AH, %OP0C    ; Sets "A" in Upper 4-bit of HTC1 register
LD      A, #0100B      ; Sets the Event counter mode of TC1
OUT     A, %OP1C
LD      A, #1001B      ; Sets the Timer mode of HTC1
OUT     A, %OP17
:
:                       ; Counting
```

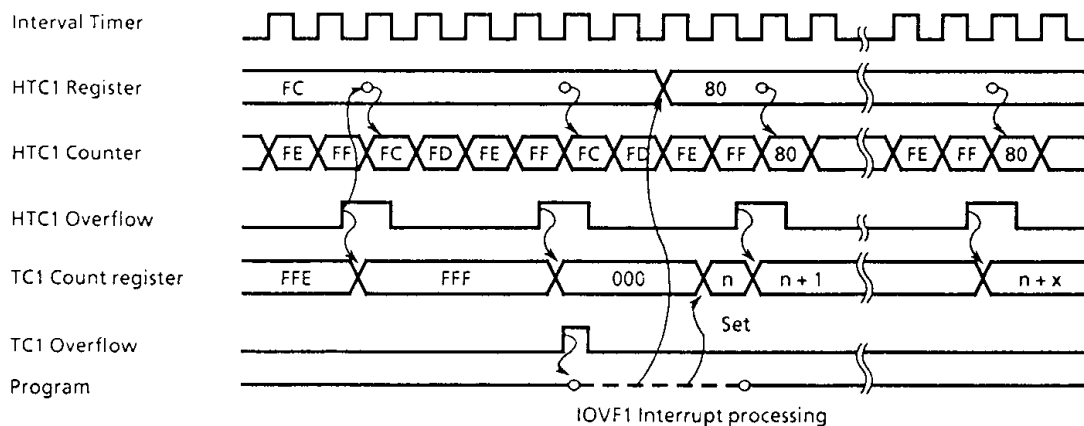


Figure 2-5. Timer mode

## (3) Frequency measurement mode

The window gate width (from interval timer output fall to rise) interval specified by the command register and the rising edges of pulses applied to HT1 and HT2 are counted in this mode. The value of the window gate width setting is the same as the interval timer interrupt frequency; therefore, by enabling interval timer interrupt, an ITMR interrupt request can be generated when counting ends. Normally, the content of the HTC counter is read and initialized in the ITMR interrupt service routine in preparation for the next count.

Maximum input frequency of HT1, HT2 are  $f_c$  [Hz].

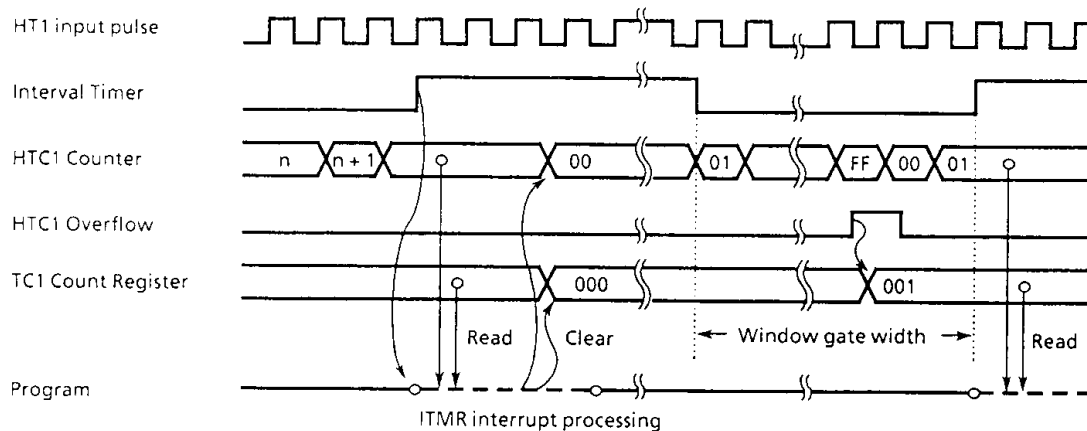


Figure 2-6. Frequency measurement mode

## (4) Pulse output mode (HTC2)

Pulses of optional frequency are output to the  $\overline{\text{PULSE}}$  pin in this mode. HTC2 counter overflows repeatedly set and clear the pulse output latch. The  $\overline{\text{PULSE}}$  output pin is shared by the R42 output pin, in which case the R42 output latch should be set to "1". The pulse output latch is initialized to "0" and the  $\overline{\text{PULSE}}$  output becomes "H" during reset.

A total of 765 different output frequencies ( $f_o$ ) can be set using clock sources (3 can be selected with the command register) and preset values. One pulse output cycle ( $1/f_o$ ) is expressed with the following formula.

$$\frac{1}{f_o} = 2 \times \frac{1}{(\text{Internal pulse rate})} \times \{256 - (\text{preset value})\}$$

(Preset value = 0 to 254)

Example: Calculating maximum output frequency (at  $f_c = 4\text{MHz}$ )

$$f_o \text{ max.} = \frac{1}{2} \times \frac{f_c}{2^3} \times \frac{1}{256 - 254} = \frac{4 \times 10^6}{32} = 125 \text{ [KHz]}$$

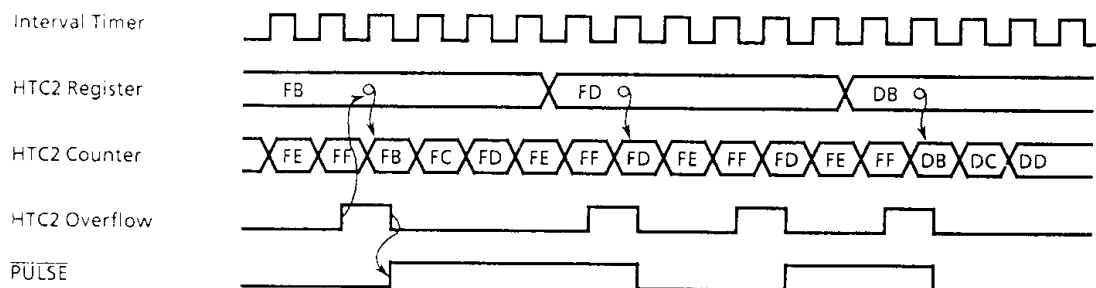


Figure 2-7. Pulse output mode

## 2.3 LCD Driver

The 47C620/820 have the circuit that directly drives the liquid crystal display (LCD) and its control circuit.

The 47C620/820 have the following connecting pins with LCD.

- ① Segment output port 32 pins (SEG31-SEG0)
- ② Common output port 4 pins (COM4-COM1)

In addition, VLC pin is provided as the drive power pin.

The devices that can be directly driven is selectable from LCD of the following drive methods.

- ① 1/4 Duty (1/3 Bias) LCD ..... Max. 128 Segment (16 digits × 8 segments)
- ② 1/3 Duty (1/3 Bias) LCD ..... Max. 96 Segment (12 digits × 8 segments)
- ③ 1/3 Duty (1/2 Bias) LCD ..... Max. 96 Segment (12 digits × 8 segments)
- ④ 1/2 Duty (1/2 Bias) LCD ..... Max. 64 Segment ( 8 digits × 8 segments)
- ⑤ Static LCD ..... Max. 32 Segment ( 4 digits × 8 segments)

### 2.3.1 Configuration of LCD driver

Figure 2-8 shows the configuration of the LCD driver.

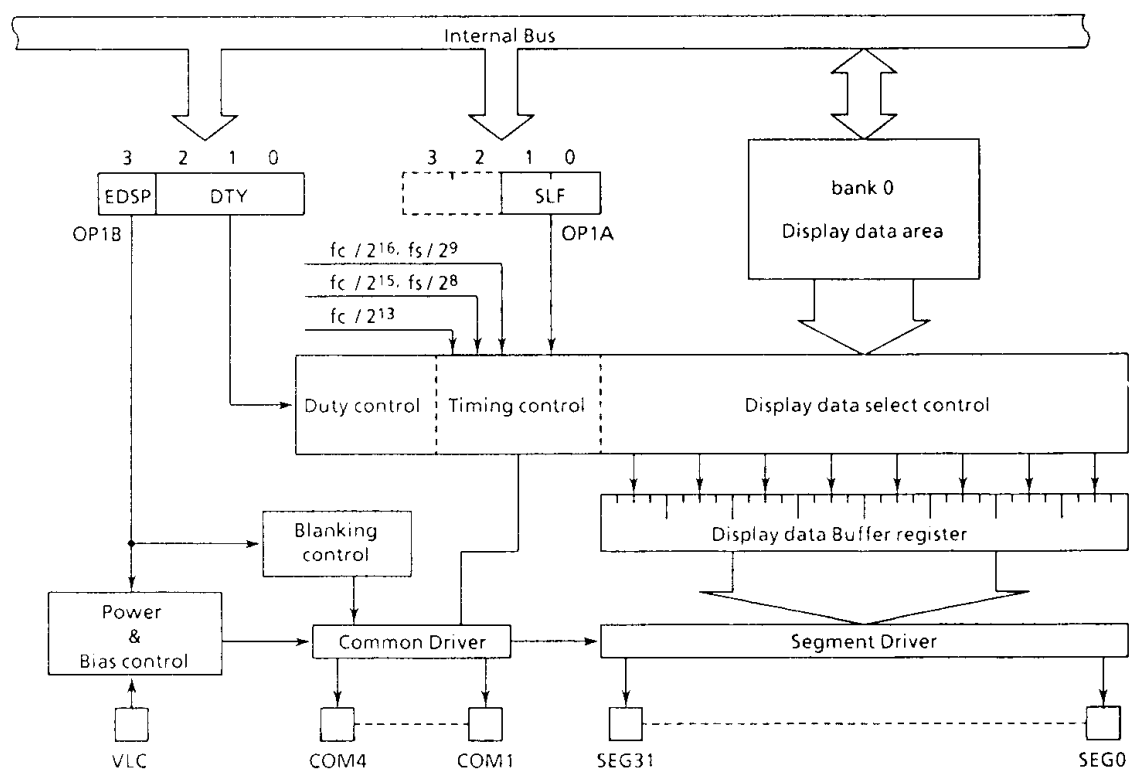
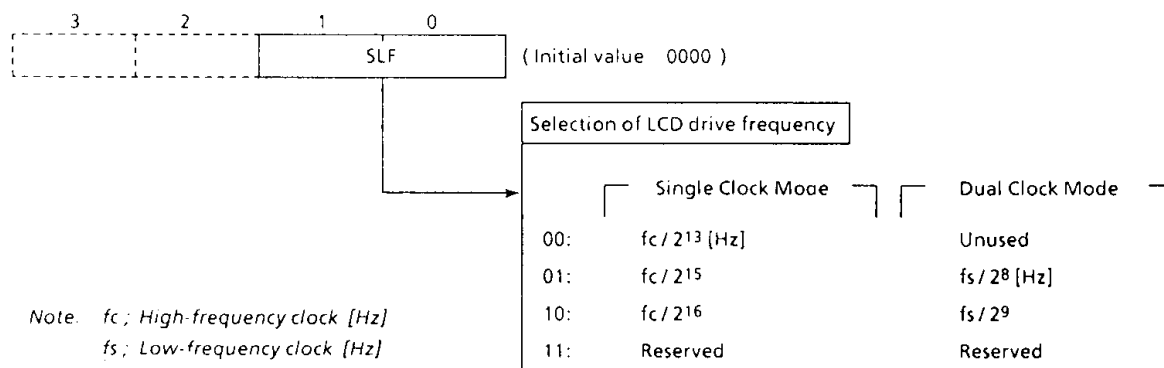


Figure 2-8. LCD Driver

### 2.3.2 Control of LCD driver circuit

The LCD driver is controlled by the command register 1,2 (OP1A, OP1B). Further, when the command register 1 is accessed, the most significant bit of the command register 2 must be set to "0" (Blanking).

LCD Driver control command register 1 (Port address OP1A)



LCD Driver control command register 2 (Port address OP1B)

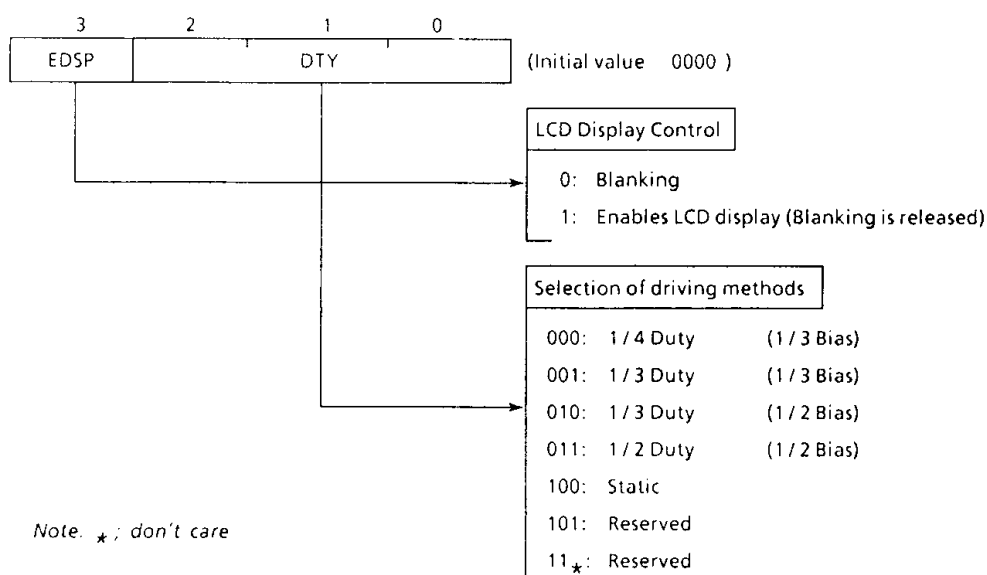


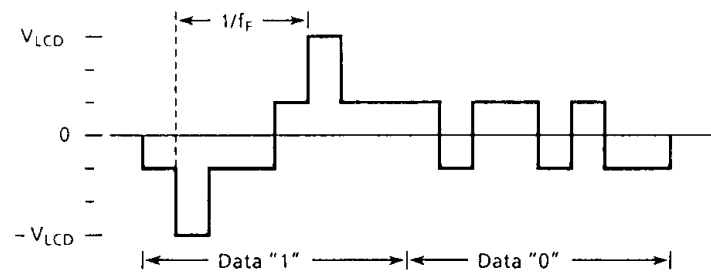
Figure 2-9. LCD Driver control Command Register

#### (1) Driving methods of LCD driver

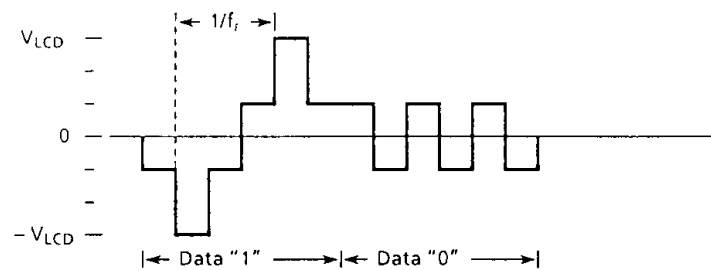
Driving methods of LCD is selected 5 kind of DTY (bit 2-0 of command register 2). The drive method is initialized according to LCD used in the initial program.

Example of LCD and their drive waveform are shown in Figure 2-10.

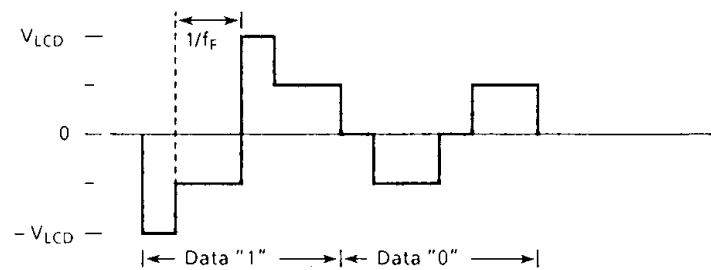
① 1/4 Duty (1/3 Bias)



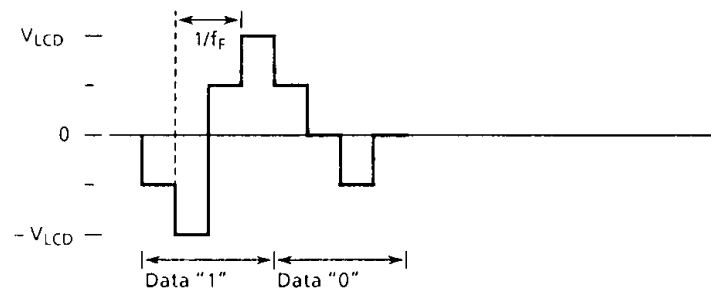
② 1/3 Duty (1/3 Bias)



③ 1/3 Duty (1/2 Bias)



④ 1/2 Duty (1/2 Bias)



⑤ Static

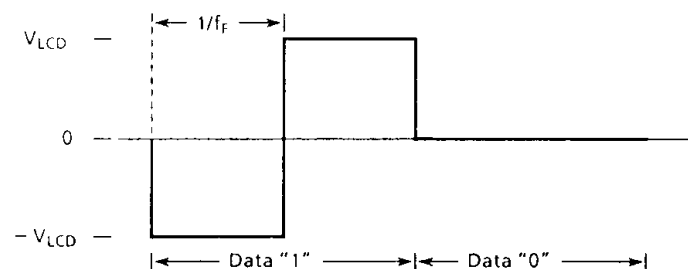


Figure 2-10. LCD drive waveform (COM-SEG pins)

## (2) Frame frequency

Frame frequency ( $f_F$ ) is set according to the drive method and base frequency as shown in the following table 2-4.

## a. At the single clock mode

| SLF | BASE FREQUENCY [Hz]  | FRAME FREQUENCY [Hz] |                                        |                                        |                      |
|-----|----------------------|----------------------|----------------------------------------|----------------------------------------|----------------------|
|     |                      | 1/4 DUTY             | 1/3 DUTY                               | 1/2 DUTY                               | STATIC               |
| 10  | $\frac{f_c}{2^{16}}$ | $\frac{f_c}{2^{16}}$ | $\frac{4}{3} \cdot \frac{f_c}{2^{16}}$ | $\frac{4}{2} \cdot \frac{f_c}{2^{16}}$ | $\frac{f_c}{2^{16}}$ |
|     | $f_c = 4\text{MHz}$  | 61                   | 81                                     | 122                                    | 61                   |
| 01  | $\frac{f_c}{2^{15}}$ | $\frac{f_c}{2^{15}}$ | $\frac{4}{3} \cdot \frac{f_c}{2^{15}}$ | $\frac{4}{2} \cdot \frac{f_c}{2^{15}}$ | $\frac{f_c}{2^{15}}$ |
|     | $f_c = 4\text{MHz}$  | 122                  | 163                                    | 244                                    | 122                  |
| 00  | $\frac{f_c}{2^{13}}$ | $\frac{f_c}{2^{13}}$ | $\frac{4}{3} \cdot \frac{f_c}{2^{13}}$ | $\frac{4}{2} \cdot \frac{f_c}{2^{13}}$ | $\frac{f_c}{2^{13}}$ |
|     | $f_c = 1\text{MHz}$  | 122                  | 163                                    | 244                                    | 122                  |

Note .  $f_c$ ; High-frequency clock [Hz]

## b. At the dual clock mode

| SLF | BASE FREQUENCY [Hz]  | FRAME FREQUENCY [Hz] |                                     |                                     |                   |
|-----|----------------------|----------------------|-------------------------------------|-------------------------------------|-------------------|
|     |                      | 1/4 DUTY             | 1/3 DUTY                            | 1/2 DUTY                            | STATIC            |
| 10  | $\frac{f_s}{2^9}$    | $\frac{f_s}{2^9}$    | $\frac{4}{3} \cdot \frac{f_s}{2^9}$ | $\frac{4}{2} \cdot \frac{f_s}{2^9}$ | $\frac{f_s}{2^9}$ |
|     | $f_s = 32\text{KHz}$ | 61                   | 83                                  | 125                                 | 61                |
| 01  | $\frac{f_s}{2^8}$    | $\frac{f_s}{2^8}$    | $\frac{4}{3} \cdot \frac{f_s}{2^8}$ | $\frac{4}{2} \cdot \frac{f_s}{2^8}$ | $\frac{f_s}{2^8}$ |
|     | $f_s = 32\text{KHz}$ | 125                  | 167                                 | 250                                 | 125               |

Note .  $f_s$ ; Low-frequency clock [Hz]

Table 2-4. Setting of LCD Frame Frequency

## (3) LCD drive voltage

The LCD drive voltage ( $V_{LCD}$ ) is given by the difference in potential ( $V_{DD}-V_{LC}$ ) between pins VDD and VLC. Therefore, when the CPU operating voltage and LCD drive voltage are the same, the VLC pin is connected to the VSS pin.

The LCDs light only when the difference in potential between the segment output and common output is  $\pm V_{LCD}$ , and turn off at all other times.

During reset, the power switch of the LCD driver is turned off automatically, shutting off the VLC voltage.

Both the segment output and common output become  $V_{DD}$  level at this time and the LCDs turn off.

The power switch is turned on to supply VLC voltage to the LCD driver by setting EDSP (bit 3 of the command register 2) to "1<sub>B</sub>". After that, the power switch will not turn off even during blanking (setting EDSP to "01<sub>B</sub>") and the VLC voltage continues to flow.

The power switch is turned off during hold operation low power consumption by turning off the LCD. When hold operation is released the status in effect immediately before the hold operation is reinstated.

### 2.3.3 LCD display operation

#### (1) Display data setting

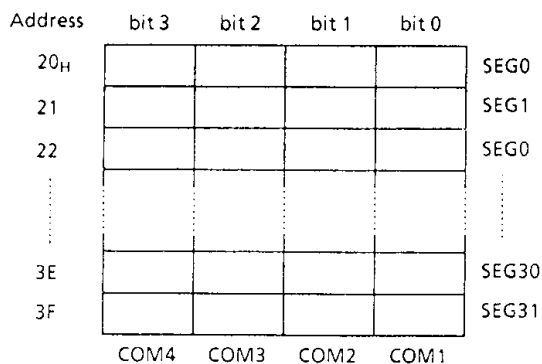
Display data are stored to the display data area (Max 32 words) in the data memory (bank0).

The display data stored to the display data area (address 20-3F<sub>H</sub>) are read automatically and sent to the LCD driver by the hardware.

The LCD driver generates the segment signals and common signals in accordance with the display data and drive method. Therefore, display patterns can be changed by only overwriting the contents of the display data area with a program. The table look up instruction is mainly used for this overwriting.

Figure 2-11 shows the correspondence between the display data area and the SEG/COM pins. The LCD light when the display data is "1" and turn off when "0".

The number of segment which can be driven differs depending on the LCD drive method therefore, the number of display data area bits used to store the data also differs. Consequently, data memory not used to store display data and data memory for which the addresses are not connected to LCD can be used to store ordinary user's processing data.



| Driving methods | bit 3 | bit 2 | bit 1 | bit 0 |
|-----------------|-------|-------|-------|-------|
| 1 / 4 Duty      | COM4  | COM3  | COM2  | COM1  |
| 1 / 3 Duty      | —     | COM3  | COM2  | COM1  |
| 1 / 2 Duty      | —     | —     | COM2  | COM1  |
| Static          | —     | —     | —     | COM1  |

Note. — ; This bit is not used for display data.

Figure 2-11. LCD Display Data Area (Bank 0)

Table 2-5. Drivinig Method and Bit for Display Data

#### (2) Blanking

Blanking is applied by setting EDSP to "0" and turns off the LCD by outputting the non light operation level to the COM pin.

The SEG pin continuously outputs the signal level in accordance with the display data and drive method.

With static drive, no voltage is applied between the COM and SEG pins when the LCD is turned off by data (display data cleared to "0"), but the COM pin output becomes constant at the  $V_{LCD}/2$  level when turning off the LCD by blanking, so the COM and SEG pins are then driven by  $V_{LCD}/2$ .

### 2.3.4 Control method of LCD driver

#### (1) Initial Setting

Flow chart of initial setting are as shown in Figure 2-12.

Example : When operating the 47C820 with 1/4 duty LCD using a from frequency of  $f_c/2^{16}$  [HZ] .

```
LD      A, #0000B ; Sets the 1/4 duty drive
OUT     A, %OP1B
LD      A, #0010B ; Setting of base frequency
OUT     A, %OP1A
:
:           ; Setting of clear or initial value of
:           ; display area in the data memory
LD      A, #1000B ; Display enable
OUT     A, %OP1B
:
```

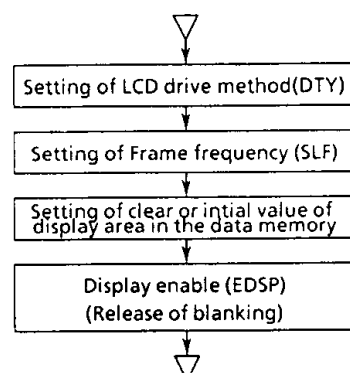


Figure 2-12. Initial setting of LCD driver

Example of numeric display data using the 1/4 duty LCD are given in Table 2-6.

The COM pin and SEG pin connection method is as shown in Figure 2-13.

| Num<br>eric | Display | Display data          |                      | Num<br>eric | Display | Display data          |                      |
|-------------|---------|-----------------------|----------------------|-------------|---------|-----------------------|----------------------|
|             |         | High order<br>address | Low order<br>address |             |         | High order<br>address | Low order<br>address |
| 0           | 0.      | 1101                  | 1111                 | 5           | 5       | 1011                  | 0101                 |
| 1           | 1       | 0000                  | 0110                 | 6           | 6       | 1111                  | 0101                 |
| 2           | 2       | 1110                  | 0011                 | 7           | 7       | 0001                  | 0111                 |
| 3           | 3       | 1010                  | 0111                 | 8           | 8       | 1111                  | 0111                 |
| 4           | 4       | 0011                  | 0110                 | 9           | 9       | 1011                  | 0111                 |

Table 2-6. Example of display data (1/4 Duty LCD)

Further, example numeric display data (in the same way as in Table 2-6) using the 1/3 duty LCD are given in Table 2-7. The COM and SEG pin connection method is as shown in Figure 2-14 or 2-15.

| Numeric | Display data       |                      |                   | Numeric | Display data       |                      |                   |
|---------|--------------------|----------------------|-------------------|---------|--------------------|----------------------|-------------------|
|         | High order address | Middle order address | Low order address |         | High order address | Middle order address | Low order address |
| 0       | **11               | *101                 | *111              | 5       | **01               | *111                 | *010              |
| 1       | **00               | *000                 | *011              | 6       | **11               | *111                 | *010              |
| 2       | **10               | *111                 | *001              | 7       | **01               | *001                 | *011              |
| 3       | **00               | *111                 | *011              | 8       | **11               | *111                 | *011              |
| 4       | **01               | *101                 | *011              | 9       | **01               | *111                 | *011              |

Note. \* ; don't care

Table 2-7. Example of display data (1/3 Duty LCD)

(2) Example of LCD drive output

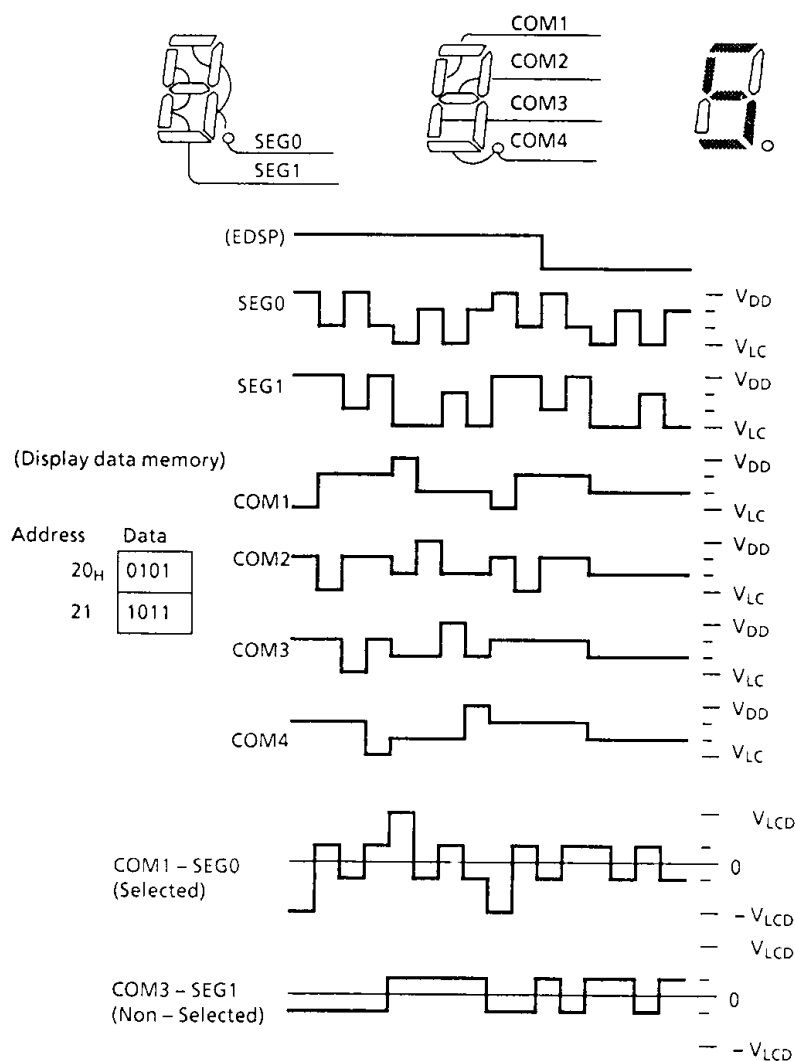


Figure 2-13. 1/4 Duty (1/3 Bias) Drive

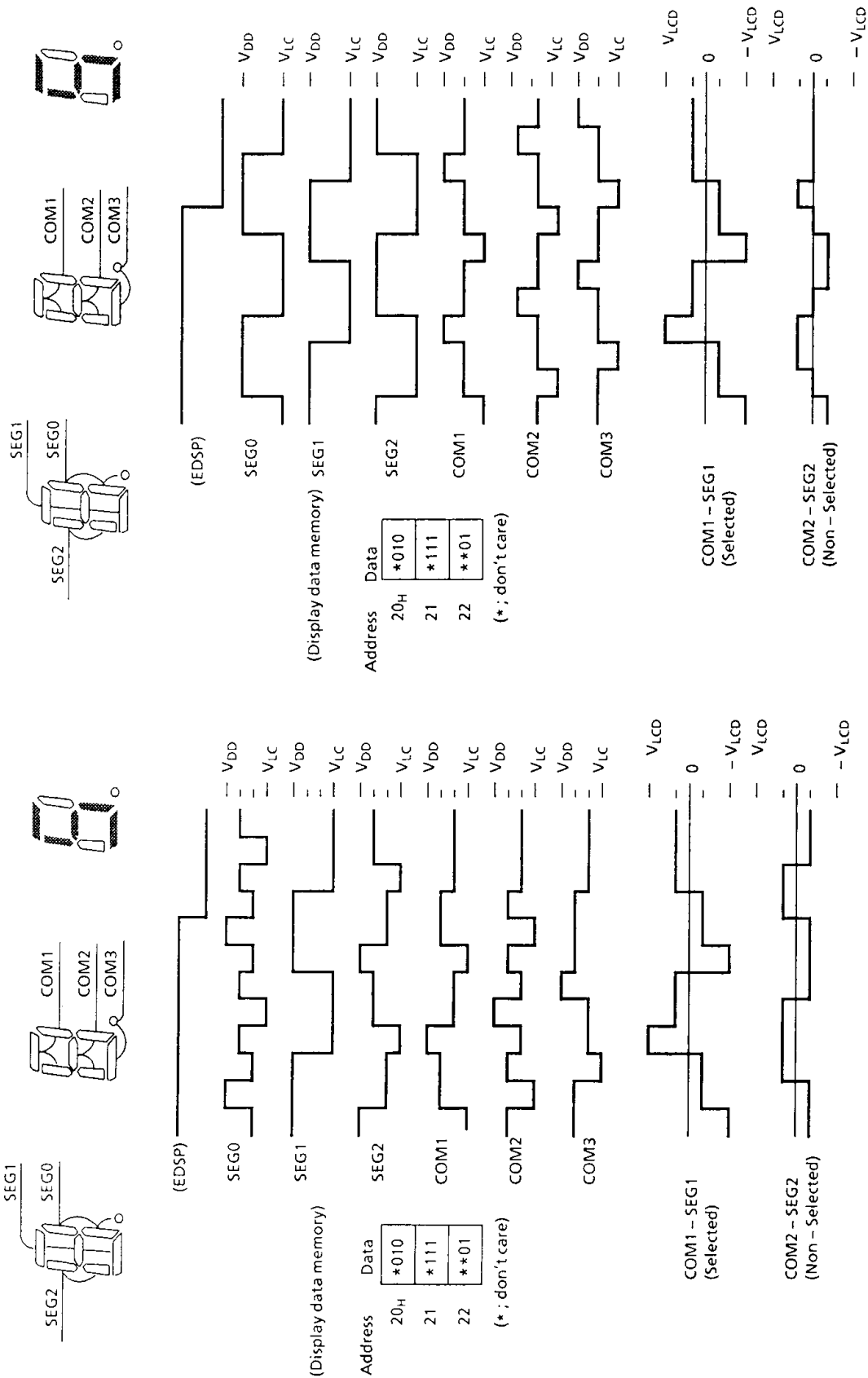


Figure 2-15. 1/3 Duty (1/2 Bias) Drive

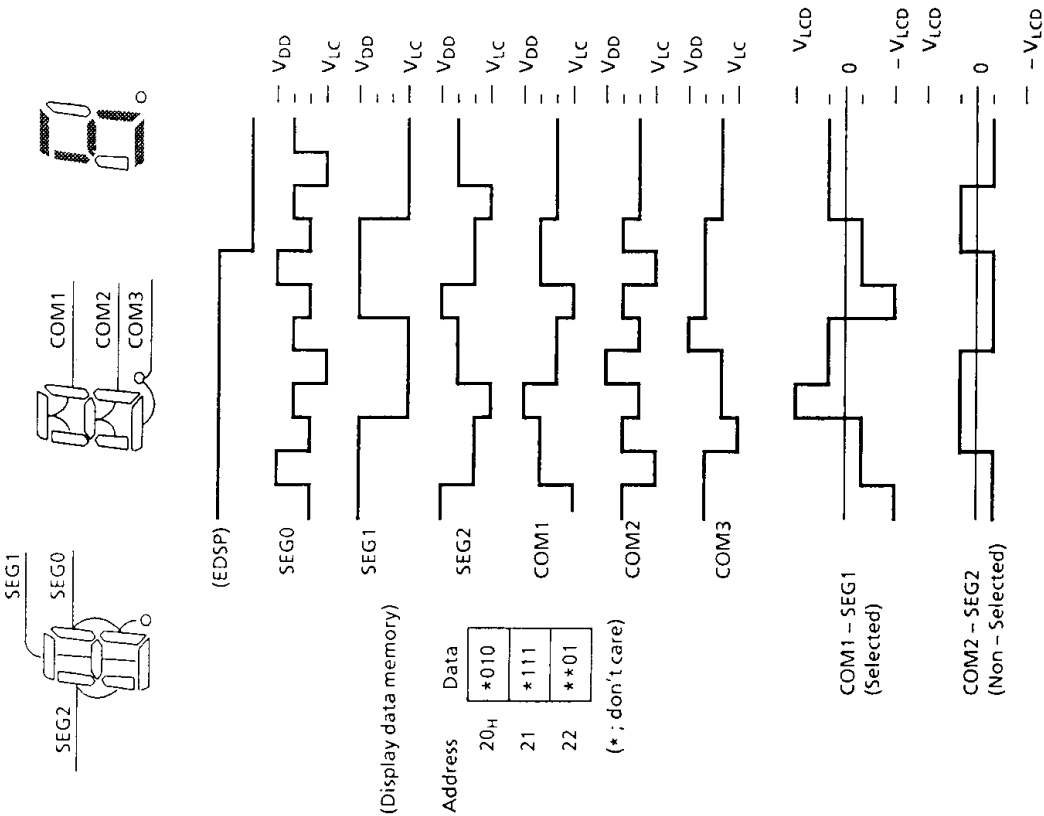


Figure 2-14. 1/3 Duty (1/3 Bias) Drive

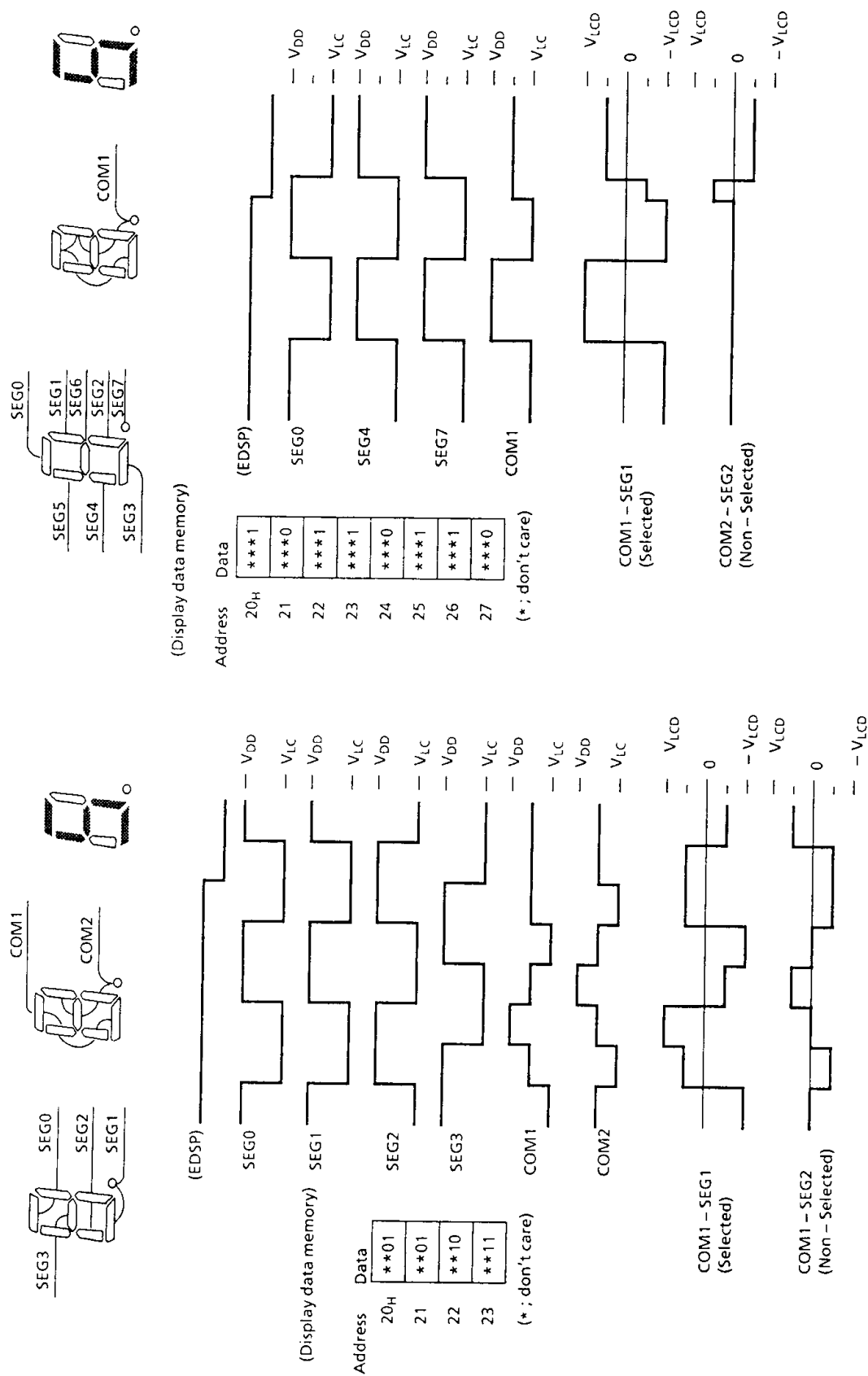


Figure 2-17. Static Drive

Figure 2-16. 1/2 Duty (1/2 Bias) Drive

## ELECTRICAL CHARACTERISTICS

## ABSOLUTE MAXIMUM RATINGS

(V<sub>SS</sub> = 0V)

| PARAMETER                                   | SYMBOL             | PINS                       | RATINGS                        | UNIT |
|---------------------------------------------|--------------------|----------------------------|--------------------------------|------|
| Supply Voltage                              | V <sub>DD</sub>    |                            | - 0.3 to 7                     | V    |
| Supply Voltage (LCD drive)                  | V <sub>LC</sub>    |                            | - 0.3 to V <sub>DD</sub> + 0.3 | V    |
| Input Voltage                               | V <sub>IN</sub>    |                            | - 0.3 to V <sub>DD</sub> + 0.3 | V    |
| Output Voltage                              | V <sub>OUT1</sub>  | Except sink open drain pin | - 0.3 to V <sub>DD</sub> + 0.3 | V    |
|                                             | V <sub>OUT2</sub>  | Sink open drain pin        | - 0.3 to 10                    |      |
| Output Current (Per 1 pin)                  | I <sub>OUT1</sub>  | Ports P1, P2               | 15                             | mA   |
|                                             | I <sub>OUT2</sub>  | Ports R4 to R9             | 3.2                            |      |
| Output Current (Total)                      | ΣI <sub>OUT1</sub> | Ports P1, P2               | 60                             | mA   |
| Power Dissipation [T <sub>opr</sub> = 70°C] | PD                 |                            | 600                            | mW   |
| Soldering Temperature (time)                | T <sub>sld</sub>   |                            | 260 (10sec)                    | °C   |
| Storage Temperature                         | T <sub>stg</sub>   |                            | - 55 to 125                    | °C   |
| Operating Temperature                       | T <sub>opr</sub>   |                            | - 40 to 70                     | °C   |

## RECOMMENDED OPERATING CONDITIONS

(V<sub>SS</sub> = 0V, T<sub>opr</sub> = - 40 to 70°C)

| PARAMETER          | SYMBOL           | PINS                    | CONDITIONS             | Min.                   | Max.                   | UNIT |
|--------------------|------------------|-------------------------|------------------------|------------------------|------------------------|------|
| Supply Voltage     | V <sub>DD</sub>  |                         | In the Normal mode     | 4.5                    | 6.0                    | V    |
|                    |                  |                         | In the SLOW mode       | 2.7                    |                        |      |
|                    |                  |                         | In the HOLD mode       | 2.0                    |                        |      |
| Input High Voltage | V <sub>IH1</sub> | Except Hysteresis Input | V <sub>DD</sub> ≥ 4.5V | V <sub>DD</sub> × 0.7  | V <sub>DD</sub>        | V    |
|                    | V <sub>IH2</sub> | Hysteresis Input        |                        | V <sub>DD</sub> × 0.75 |                        |      |
|                    | V <sub>IH3</sub> |                         | V <sub>DD</sub> < 4.5V | V <sub>DD</sub> × 0.9  |                        |      |
| Input Low Voltage  | V <sub>IL1</sub> | Except Hysteresis Input | V <sub>DD</sub> ≥ 4.5V | 0                      | V <sub>DD</sub> × 0.3  | V    |
|                    | V <sub>IL2</sub> | Hysteresis Input        |                        |                        | V <sub>DD</sub> × 0.25 |      |
|                    | V <sub>IL3</sub> |                         | V <sub>DD</sub> < 4.5V |                        | V <sub>DD</sub> × 0.1  |      |
| Clock Frequency    | f <sub>c</sub>   | XIN, XOUT               |                        | 0.4                    | 6.0                    | MHz  |
|                    | f <sub>s</sub>   | XTIN, XTOUT             |                        | 30.0                   | 34.0                   | KHz  |

Note. Input Voltage V<sub>IH3</sub>, V<sub>IL3</sub> : in the SLOW and HOLD mode.

## D.C. CHARACTERISTICS

(V<sub>SS</sub> = 0V, T<sub>opr</sub> = -40 to 70°C)

| PARAMETER                           | SYMBOL            | PINS                                                                | CONDITIONS                                                                              | Min. | Typ. | Max. | UNIT |     |   |
|-------------------------------------|-------------------|---------------------------------------------------------------------|-----------------------------------------------------------------------------------------|------|------|------|------|-----|---|
| Hysteresis Voltage                  | V <sub>HS</sub>   | Hysteresis Input                                                    |                                                                                         | —    | 0.7  | —    | V    |     |   |
| Input Current                       | I <sub>IN1</sub>  | Port K0, TEST, $\overline{\text{RESET}}$ , $\overline{\text{HOLD}}$ | V <sub>DD</sub> = 5.5V,                                                                 | —    | —    | ± 2  | μA   |     |   |
|                                     | I <sub>IN2</sub>  | Open drain R port                                                   | V <sub>IN</sub> = 5.5V / 0V                                                             |      |      |      |      |     |   |
| Input Low Current                   | I <sub>IL</sub>   | Push-pull R port                                                    | V <sub>DD</sub> = 5.5V, V <sub>IN</sub> = 0.4V                                          | —    | —    | — 2  | mA   |     |   |
| Input Registance                    | R <sub>IN1</sub>  | Port K0 with pull-up/pull-down                                      |                                                                                         | 30   | 70   | 150  | KΩ   |     |   |
|                                     | R <sub>IN2</sub>  | $\overline{\text{RESET}}$                                           |                                                                                         | 100  | 220  | 450  |      |     |   |
| Output Leakage Current              | I <sub>LO</sub>   | Open drain ports P, R                                               | V <sub>DD</sub> = 5.5V, V <sub>OUT</sub> = 5.5V                                         | —    | —    | 2    | μA   |     |   |
| Output High Voltage                 | V <sub>OH</sub>   | Push-pull R port                                                    | V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = — 200μA                                       | 2.4  | —    | —    | V    |     |   |
| Output Low Voltage                  | V <sub>OL2</sub>  | Except XOUT XTOUT and ports P1, P2                                  | V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 1.6mA                                         | —    | —    | 0.4  | V    |     |   |
| Output Low Current                  | I <sub>OL1</sub>  | Ports P1, P2                                                        | V <sub>DD</sub> = 4.5V, V <sub>OL</sub> = 1.0V                                          | —    | 10   | —    | mA   |     |   |
| Segment Output Registance           | R <sub>OS</sub>   | SEG pin                                                             | V <sub>DD</sub> = 5V, V <sub>DD</sub> – V <sub>LC</sub> = 3V                            | —    | 20   | —    | KΩ   |     |   |
| Common Output Registance            | R <sub>OC</sub>   | COM pin                                                             |                                                                                         |      |      |      |      |     |   |
| Segment/Common Output Registance    | V <sub>O2/3</sub> | SEG / COM pin                                                       |                                                                                         |      |      | 3.8  | 4.0  | 4.2 | V |
|                                     | V <sub>O1/2</sub> |                                                                     |                                                                                         |      |      | 3.3  | 3.5  | 3.7 |   |
|                                     | V <sub>O1/3</sub> |                                                                     |                                                                                         |      |      | 2.8  | 3.0  | 3.2 |   |
| Supply Current (in the Normal mode) | I <sub>DD</sub>   |                                                                     | V <sub>DD</sub> = 5.5V, V <sub>LC</sub> = V <sub>SS</sub><br>f <sub>c</sub> = 4MHz      | —    | 3    | 6    | mA   |     |   |
| Supply Current (in the SLOW mode)   | I <sub>DDs</sub>  |                                                                     | V <sub>DD</sub> = 3.0V, V <sub>LC</sub> = V <sub>SS</sub><br>f <sub>s</sub> = 32.768KHz | —    | 30   | —    | μA   |     |   |
| Supply Current (in the HOLD mode)   | I <sub>DDH</sub>  |                                                                     | V <sub>DD</sub> = 5.5V                                                                  | —    | 0.5  | 10   | μA   |     |   |

Note 1. Typ. values show those at T<sub>opr</sub> = 25°C, V<sub>DD</sub> = 5V.

Note 2. Input Current I<sub>IN1</sub> ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. Output Resistance R<sub>OS</sub>, R<sub>OC</sub> ; Shows on-resistance at the level switching.

Note 4. V<sub>O2/3</sub> ; Shows 2/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.

V<sub>O1/2</sub> ; Shows 1/2 level output voltage, when the 1/2 duty or static LCD is used.

V<sub>O1/3</sub> ; Shows 1/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.

Note 5. Supply Current I<sub>DD</sub>, I<sub>DDH</sub> ; V<sub>IN</sub> = 5.3V/0.2V

The K0 port is open when the input resistor is contained.

The voltage applied to the R port is within the valid range.

Note 6. Supply Current I<sub>DDS</sub> ; V<sub>IN</sub> = 2.8V/0.2V. Only low frequency clock is only oscillated (connecting XTIN, XTOUT).

## A.C. CHARACTERISTICS

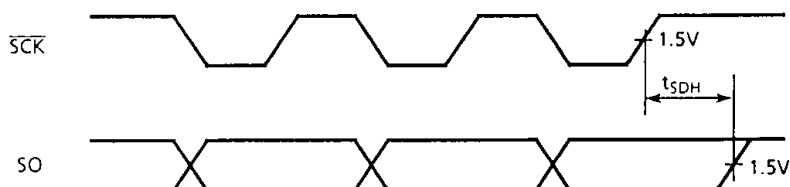
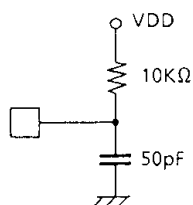
(V<sub>SS</sub> = 0V, V<sub>DD</sub> = 4.5 to 6.0V, T<sub>opr</sub> = -40 to 70°C)

| PARAMETER                                | SYMBOL           | CONDITIONS                   | Min.                     | Typ. | Max.           | UNIT |
|------------------------------------------|------------------|------------------------------|--------------------------|------|----------------|------|
| Instruction Cycle Time                   | t <sub>cy</sub>  | in the Normal mode           | 1.9                      | —    | 20             | μs   |
|                                          |                  | in the SLOW mode             | 235                      | —    | 267            | μs   |
| High Level Clock Pulse Width             | t <sub>WCH</sub> | For external clock operation | 80                       | —    | —              | ns   |
| Low Level Clock Pulse Width              | t <sub>WCL</sub> |                              |                          |      |                |      |
| Shift data Hold Time                     | t <sub>SDH</sub> |                              | 0.5t <sub>cy</sub> - 300 | —    | —              | ns   |
| High Speed Timer/Counter input frequency | f <sub>HT</sub>  |                              | —                        | —    | f <sub>c</sub> | MHz  |

Note: Shift data Hold time :

External circuit for  $\overline{SCK}$  pin and SO pin

Serial port (completion of transmission)

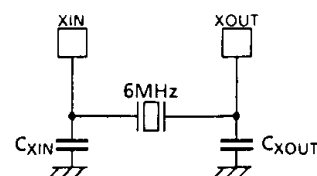


## RECOMMENDED OSCILLATING CONDITIONS

(V<sub>SS</sub> = 0V, V<sub>DD</sub> = 4.5 to 6.0V, T<sub>opr</sub> = -40 to 70°C)

## (1) 6MHz

Ceramic Resonator

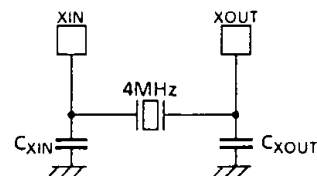
CSA6.00MGU (MURATA) C<sub>XIN</sub> = C<sub>XOUT</sub> = 30pFKBR-6.00MS (KYOCERA) C<sub>XIN</sub> = C<sub>XOUT</sub> = 30pF

## (2) 4MHz

Ceramic Resonator

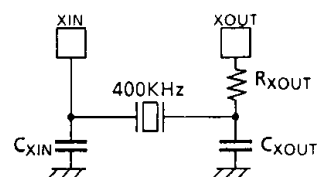
CSA4.00MG (MURATA) C<sub>XIN</sub> = C<sub>XOUT</sub> = 30pFKBR-4.00MS (KYOCERA) C<sub>XIN</sub> = C<sub>XOUT</sub> = 30pF

Crystal Oscillator

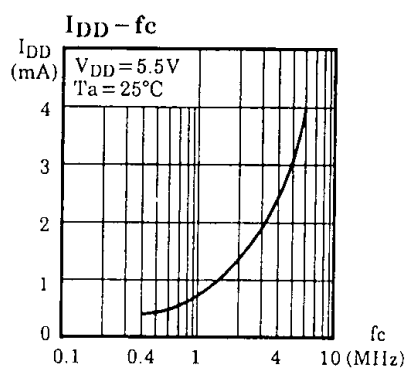
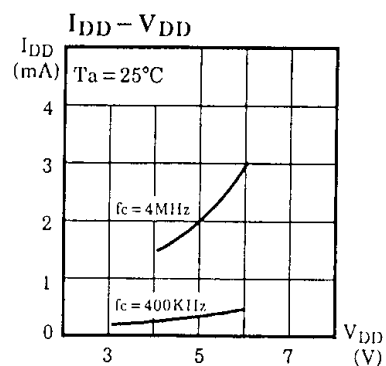
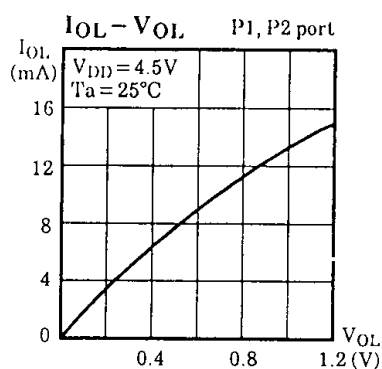
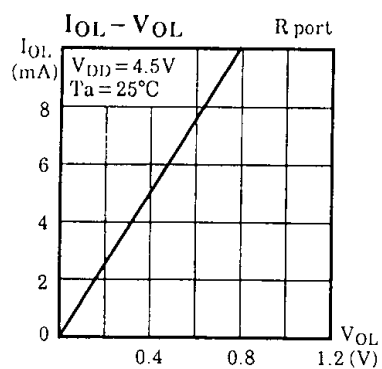
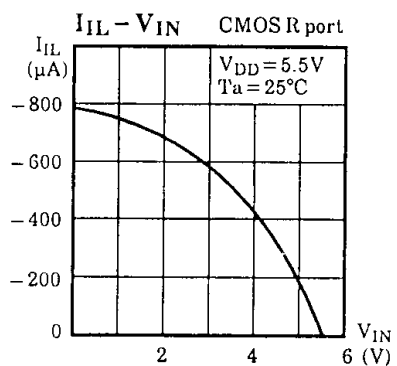
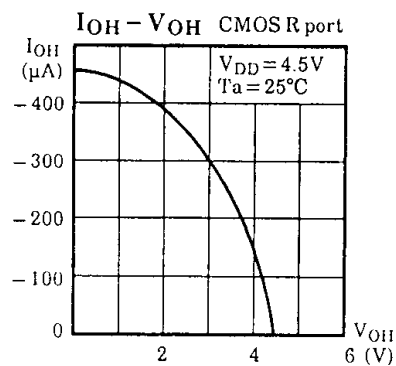
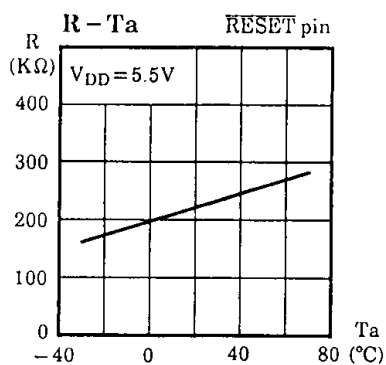
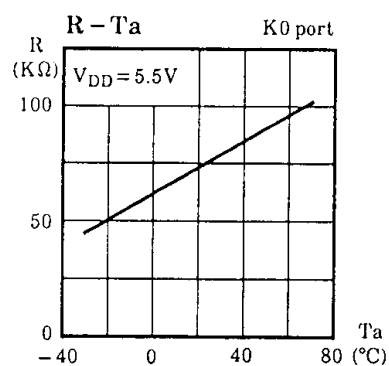
204B-6F 4.0000 (TOYOCOM) C<sub>XIN</sub> = C<sub>XOUT</sub> = 20pF

## (3) 400KHz

Ceramic Resonator

CSB400B (MURATA) C<sub>XIN</sub> = C<sub>XOUT</sub> = 220pF,R<sub>XOUT</sub> = 6.8KΩKBR-400B (KYOCERA) C<sub>XIN</sub> = C<sub>XOUT</sub> = 100pF, R<sub>XOUT</sub> = 10KΩ

## TYPICAL CHARACTERISTICS



## INPUT/OUTPUT CIRCUITRY

## (1) Control pins

The input/output circuitries of the 47C620/820 control pins are similar to those of the 47C660/860.

## (2) I/O Ports

The input/output circuitries of the 47C620/820 I/O ports are shown as belows, any one of the circuitries can be chosen by a code (GA to GF) as a mask option.

| PORT             | I/O    | INPUT/OUTPUT CIRCUITRY and CODE |                    |        | REMARKS                                                                                             |
|------------------|--------|---------------------------------|--------------------|--------|-----------------------------------------------------------------------------------------------------|
| K0               | Input  | GA, GD                          | GB, GE             | GC, GF | Pull-up/pull-down resistor<br><br>$R_{IN} = 70K\Omega$ (typ.)<br>$R = 1K\Omega$ (typ.)              |
|                  |        |                                 |                    |        |                                                                                                     |
| P1<br>P2         | Output |                                 |                    |        | Sink open drain output<br>Initial "Hi-Z"<br><br>High current<br>$I_{OL} = 10mA$ (typ.)              |
| R40<br>R41       | I/O    |                                 |                    |        | Sink open drain output<br>Initial "Hi-Z"<br><br>(Hysteresis) = Input (HTC)<br>$R = 1K\Omega$ (typ.) |
| R42<br>R43<br>R7 | I/O    |                                 |                    |        | Sink open drain output<br>Initial "Hi-Z"<br><br>$R = 1K\Omega$ (typ.)                               |
| R6<br>R5         | I/O    | GA, GB, GC                      | GD, GE, GF         |        | Sink open drain output<br>or<br>Push-pull output<br><br>$R = 1K\Omega$ (typ.)                       |
|                  |        | Initial "Hi-Z"<br>              | Initial "High"<br> |        |                                                                                                     |
| R8<br>R9         | I/O    |                                 |                    |        | Sink open drain output<br>Initial "Hi-Z"<br><br>Hysteresis input<br>$R = 1K\Omega$ (typ.)           |