μA96177 • μA96178
Differential Bus Repeaters

Description

The μA96177 and μA96178 Differential Bus Repeaters are monolithic integrated devices each designed for one-way data communications on multipoint bus transmission lines. These devices are designed for balanced transmission bus line applications and meet EIA Standard RS-485 and RS-422A. Each device is designed to improve the performance of the data communication over long bus lines. The μA96177 and μA96178 are identical except for the Enable inputs, which are complementary. The μA96177 is an active high Enable. The μA96178 is an active low Enable. These complementary Enables allow the devices to be used in pairs for bidirectional communication.

The μA96177 and μA96178 feature positive and negative current limiting and three-state outputs for the receiver and driver. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of −12 V to +12 V. The driver features thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 160°C. The driver is designed to drive current loads up to 60 mA maximum.

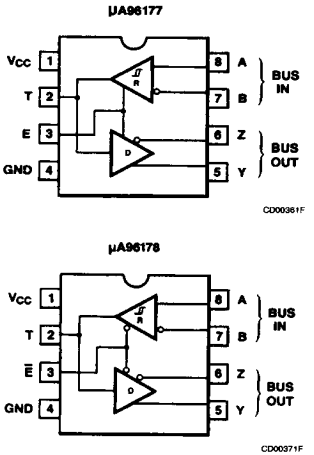
The μA96177 and μA96178 are designed for optimum performance when used on transmission buses employing the μA96172 and μA96174 differential line drivers, μA96173 and μA96175 differential line receivers, or μA96176 differential bus transceiver.

- **Meets EIA Standard RS-422A And RS-485**
- **Designed For Multipoint Transmission On Long Bus Lines In Noisy Environments**
- **Three-State Outputs**
- **Bus Voltage Range −7.0 V To 12 V**
- **Positive And Negative Current Limiting**
- **Driver Output Capability ±60 mA Max**
- **Driver Thermal Shutdown Protection**
- **Receiver Input High Impedance**
- **Receiver Input Sensitivity Of ±200 mV**
- **Receiver Input Hysteresis Of 50 mV Typical**
- **Operates From Single 5.0 V Supply**
- **Low Power Requirements**

Function Table μA96177

Differential Inputs A-B	Enable E	Outputs T	Y	Z
$V_{ID} \geq 0.2$ V	H	H	H	L
-0.2 V $< V_{ID} < 0.2$ V	H	?	?	?
$V_{ID} \leq -0.2$ V	H	L	L	H
X	L	Z	Z	Z

Connection Diagram
8-Lead DIP
(Top View)



Order Information

Device Code	Package Code	Package Description
μA96177RC	6T	Ceramic DIP
μA96177TC	9T	Molded DIP
μA96178RC	6T	Ceramic DIP
μA96178TC	9T	Molded DIP

Function Table μA96178

Differential Inputs A-B	Enable Ē	Outputs T	Y	Z
$V_{ID} \geq 0.2$ V	L	H	H	L
-0.2 V $< V_{ID} < 0.2$ V	L	?	?	?
$V_{ID} \leq -0.2$ V	L	L	L	H
X	H	Z	Z	Z

H = High Level
L = Low Level
? = Indeterminate
X = Immaterial
Z = High Impedance (off)

Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1,2]	
8L-Ceramic DIP	1.30 W
8L-Molded DIP	0.93 W
Supply Voltage[3]	7.0 V
Input Voltage	5.5 V

Notes
1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Ceramic DIP at 8.7 mW/°C, and the 8L-Molded DIP at 7.5 mW/°C.
3. All voltage values are with respect to network ground terminal.

Recommended Operating Conditions

Symbol	Characteristic		Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
V_I or V_{CM}	Voltage at any Bus Terminal (Separately or Common mode)		−7.0[1]		12	V
V_{ID}	Differential Input Voltage[2]				±12	V
I_{OH}	Output Current HIGH	Driver			−60	mA
		Receiver			−400	μA
I_{OL}	Output Current LOW	Driver			60	mA
		Receiver			16	
T_A	Operating Temperature		0	25	70	°C

Notes
1. The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.
2. Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

μA96177, μA96178
Electrical Characteristics Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified.

Driver Section

Symbol	Characteristic	Condition		Min	Typ[1]	Max	Unit
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{IC}	Input Clamp Voltage	$I_I = -18$ mA				−1.5	V
$\|V_{OD1}\|$	Differential Output Voltage	$I_O = 0$ mA				6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	$R_L = 100\ \Omega$ Fig. 2		2.0	2.25		V
		$R_L = 54\ \Omega$ Fig. 1		1.5	2.0		
$\Delta\|V_{OD}\|$	Change in Magnitude of Differential Output Voltage[2]	$R_L = 54\ \Omega$ or $100\ \Omega$, Fig.1				±0.2	V
V_{OC}	Common Mode Output Voltage[3]					3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage[2]					±0.2	V
I_O	Output Current with Power off	$V_{CC} = 0$ V, $V_O = -7.0$ V to 12 V				±100	μA
I_{OZ}	High Impedance State Output Current	$V_O = -7.0$ V to 12 V			±50	±200	μA
I_{IH}	Input Current HIGH	$V_I = 2.7$ V				20	μA
I_{IL}	Input Current LOW	$V_I = 0.5$ V				−100	μA
I_{OS}	Short Circuit Output Current	$V_O = -7.0$ V				−250	mA
		$V_O = 0$ V				−150	
		$V_O = V_{CC}$				150	
		$V_O = 12$ V				250	
I_{CC}	Supply Current	No Load	Outputs Enabled			35	mA
			Outputs Disabled			40	

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μA96177, μA96178 (Cont.)
Electrical Characteristics Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified.

Drive Switching Characteristics V_{CC} = 5.0 V, T_A = 25°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{DD}	Differential Output Delay Time	R_L = 60 Ω, Fig. 4		15	25	ns
t_{TD}	Differential Output Transition Time	R_L = 60 Ω, Fig. 4		15	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27 Ω, Fig. 5		12	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 27 Ω, Fig. 5		12	20	ns
t_{PZH}	Output Enable Time to High Level	R_L = 110 Ω, Fig. 6		25	45	ns
t_{PZL}	Output Enable Time to Low Level	R_L = 110 Ω, Fig. 7		25	40	ns
t_{PHZ}	Output Disable Time from High Level	R_L = 110 Ω, Fig. 6		20	25	ns
t_{PLZ}	Output Disable Time from Low Level	R_L = 110 Ω, Fig. 7		29	35	ns

Receiver Section

Symbol	Characteristic	Condition		Min	Typ[1]	Max	Unit
V_{TH}	Differential Input High Threshold Voltage	V_O = 2.7 V, I_O = −0.4 mA				0.2	V
V_{TL}	Differential Input Low Threshold Voltage	V_O = 0.5 V, I_O = 8.0 mA		−0.2[5]			V
$V_{T+}-V_{T-}$	Hysteresis[6]	V_{CM} = 0 V			50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{ID} = 200 mV, I_{OH} = −400 μA, Fig. 3		2.7			V
V_{OL}	Low Level Output Voltage	V_{ID} = −200 mV, Fig. 3	I_{OL} = 8.0 mA			0.45	V
			I_{OL} = 16 mA			0.50	
I_{OZ}	High-Impedance State Output	V_O = 0.4 V				−360	μA
		V_O = 2.4 V				20	
I_I	Line Input Current[7]	Other Input = 0 V	V_I = 12 V			1.0	mA
			V_I = −7.0 V			−0.8	
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7 V				20	μA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4 V				−100	μA
R_I	Input Resistance				12		kΩ
I_{OS}	Short Circuit Output Current			−15		−85	mA
I_{CC}	Supply Current (total package)	No Load	Outputs Enabled			35	mA
			Outputs Disabled			40	

μA96177, μA96178 (Cont.)
Electrical Characteristics Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified.

Receiver Switching Characteristics V_{CC} = 5.0 V, T_A = 25°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{ID} = 0 V to 3.0 V, C_L = 15 pF, Fig. 8		16	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			16	25	ns
t_{PZH}	Output Enable Time to High Level	C_L = 15 pF, Fig. 9		15	22	ns
t_{PZL}	Output Enable Time to Low Level			15	22	ns
t_{PHZ}	Output Disable Time from High Level	C_L = 5.0 pF, Fig. 9		14	30	ns
t_{PLZ}	Output Disable Time from Low Level			24	40	ns

Notes
1. 1. All typical values are at V_{CC} = 5.0 V and T_A = 25°C.
2. $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
3. In EIA Standard RS-422A and RS-485, V_{OC}, which is the average of the two output voltages with respect to GND, is called output offset voltage, V_{OS}.
4. The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.
5. Hysteresis is the difference between the positive-going input threshold voltage, V_{T+} and the negative-going input threshold voltage, V_{T-}.
6. Refer to EIA Standard RS-485 for exact conditions.

Parameter Measurement Information

Figure 1 Driver V_{OD2} and V_{OC}

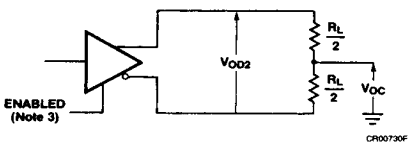


Figure 2 Driver V_{OD2} with Varying Common Mode Voltage

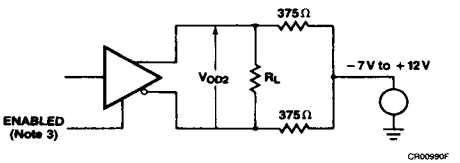
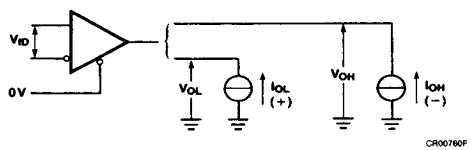


Figure 3 Receiver V_{OH} and V_{OL}



Parameter Measurement Information (Cont.)

Figure 4 Driver Differential Output Delay and Transition Times

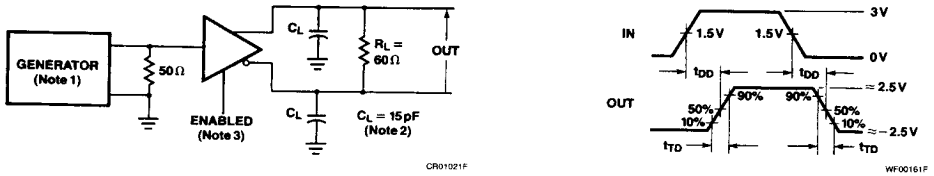


Figure 5 Drive Propagation Times

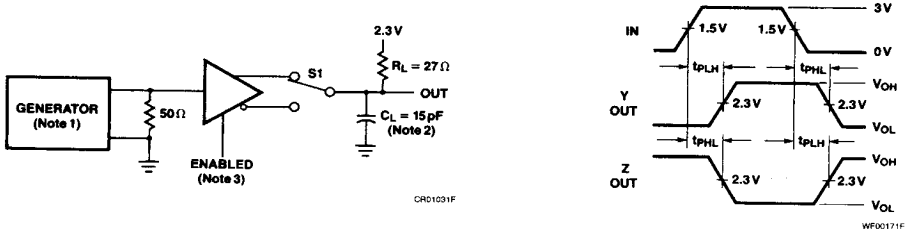


Figure 6 Driver Enable and Disable Times (t_{PZH}, t_{PHZ})

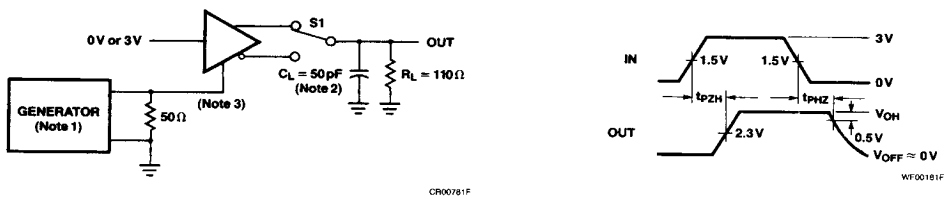
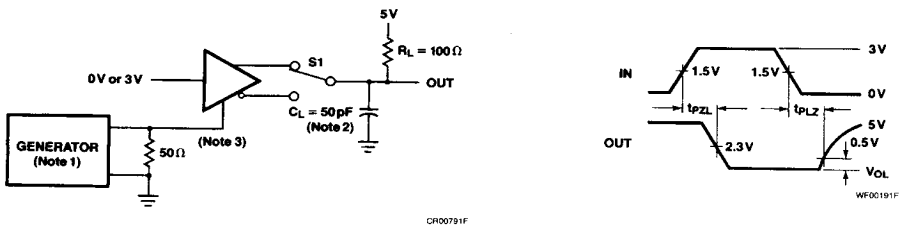
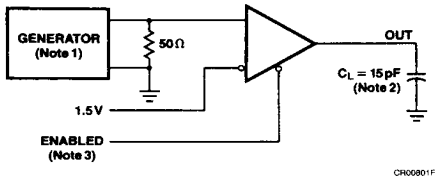


Figure 7 Driver Enable and Disable Times (t_{PZL}, t_{PLZ})



Parameter Measurement Information (Cont.)

Figure 8 Receiver Propagation Delay Times



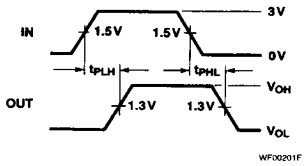
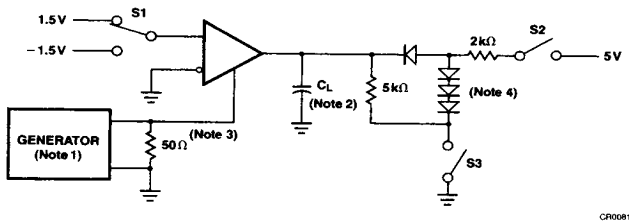
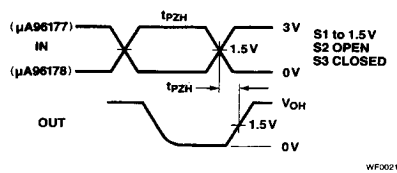
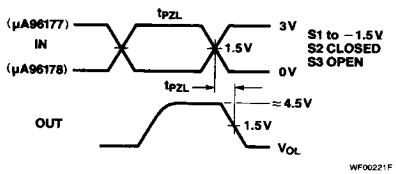
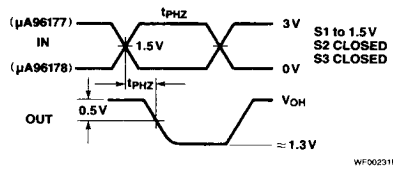


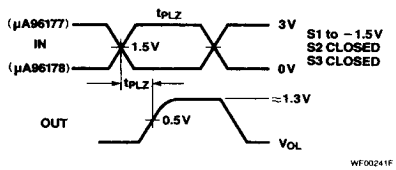
Figure 9 Receiver Enable and Disable Times







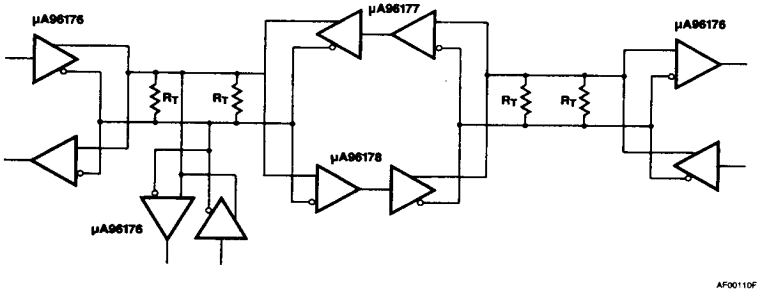




Notes

1. The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, duty cycle≈50%, $t_r \leqslant 6.0$ ns, $t_f \leqslant 6.0$ ns, $Z_O = 50\ \Omega$.
2. C_L includes probe and stray capacitance.
3. μA96178 Enable is active low, μA96177 Enable is active high.
4. All diodes are 1N916 or equivalent.

Typical Application



Note
The line length should be terminated at both ends in its characteristic impedance.
Stub lengths off the main line should be kept as short as possible.