

FEATURES

- Low skew
- Extended 100E VEE range of $-4.2V$ to $-5.5V$
- Guaranteed skew limits
- Differential design
- VBB output
- Enable input
- Fully compatible with industry standard 10KH, 100K I/O levels
- 75K Ω input pulldown resistors
- ESD protection of 2000V
- Fully compatible with Motorola MC10E/100E111

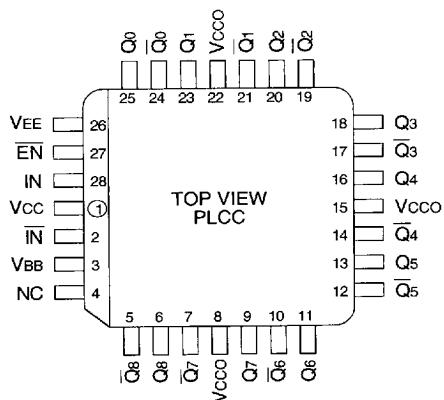
DESCRIPTION

The SY10/100E111 are low skew 1-to-9 differential drivers designed for clock distribution in new, high-performance ECL systems. They accept one differential or single-ended input, with VBB used for single-ended operation. The signal is fanned out to nine identical differential outputs. An enable input is also provided such that a logic HIGH disables the device by forcing all Q outputs LOW and all \bar{Q} outputs HIGH.

The device is specifically designed and produced for low skew. The interconnect scheme and metal layout are carefully optimized for minimal gate-to-gate skew within the device. Wafer characterization and process control ensure consistent distribution of propagation delay from lot to lot. Since the E111 shares a common set of "basic" processing with the other members of the ECLinPS family, wafer characterization at the point of device personalization allows for tighter control of parameters, including propagation delay.

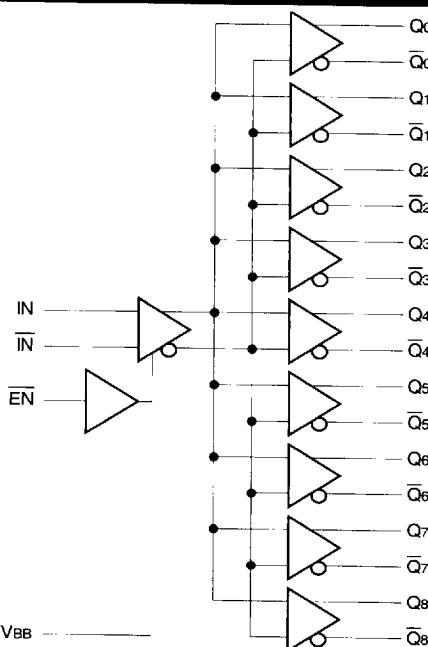
To ensure that the skew specification is met, it is necessary that both sides of the differential output are terminated into 50 Ω , even if only one side is being used. In most applications, all nine differential pairs will be used and, therefore, terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i.e. sharing the same VCCO as the pair(s) being used on that side) in order to maintain minimum skew.

The VBB output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When using VBB for this purpose, it is recommended that VBB is decoupled to VCC via a 0.01 μ F capacitor.

PIN CONFIGURATION

PIN NAMES

Pin	Function
IN, \bar{IN}	Differential Input Pair
EN	Enable Input
Q0, $\bar{Q}0$ — Q8, $\bar{Q}8$	Differential Outputs
VBB	VBB Output
VCCO	Vcc to Output

BLOCK DIAGRAM



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DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
VBB	Output Reference Voltage	10E	-1.38	—	-1.27	-1.35	—	-1.25	-1.31	—	V	—
		100E	-1.38	—	-1.26	-1.38	—	-1.26	-1.38	—	-1.19	-1.26
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I _{EE}	Power Supply Current	10E	—	48	60	—	48	60	—	48	mA	—
		100E	—	48	60	—	48	60	—	55	69	—

TIMING DIAGRAMS

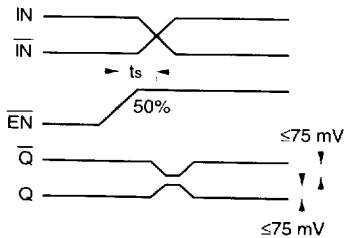


Figure 1. Set-up Time

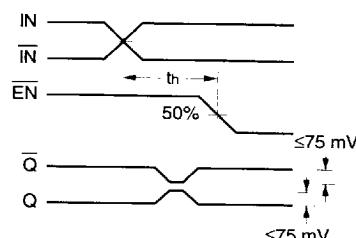


Figure 2. Hold Time

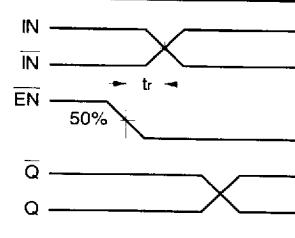


Figure 3. Release Time

AC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition ⁽¹⁻⁹⁾
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
tPLH tPHL	Propagation Delay to Output	430	—	630	430	—	630	430	—	630	ps	1
	IN (differential)	330	—	730	330	—	730	330	—	730		2
	IN (single-ended)	450	—	850	450	—	850	450	—	850		3
	Enable	450	—	850	450	—	850	450	—	850		3
tsKEW	Within-Device Skew	—	25	50	—	25	50	—	25	50	ps	4
ts	Set-up Time, EN to IN	200	0	—	200	0	—	200	0	—	ps	5
tH	Hold Time, IN to EN	0	-200	—	0	-200	—	0	-200	—	ps	6
tR	Release Time, EN to IN	300	100	—	300	100	—	300	100	—	ps	7
VPP	Minimum Input Swing	250	—	—	250	—	—	250	—	—	mV	8
VCMR	Common Mode Range	-1.6	—	-0.4	-1.6	—	-0.4	-1.6	—	-0.4	V	9
tr tf	Rise/Fall Times 20% to 80%	275	375	600	275	375	600	275	375	600	ps	—

NOTES:

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
3. Enable is defined as the propagation delay from the 50% point of a **negative** transition on EN to the 50% point of a **positive** transition on Q (or a negative transition on \bar{Q}). Disable is defined as the propagation delay from the 50% point of a **positive** transition on EN to the 50% point of a **negative** transition on Q (or a positive transition on \bar{Q}).
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. The set-up time is the minimum time that EN must be asserted prior to the next transition of IN/IN to prevent an output response greater than $\pm 75mV$ to that IN/IN transition (see Figure 1).
6. The hold time is the minimum time that EN must remain asserted after a negative going IN or a positive going \bar{IN} to prevent an output response greater than $\pm 75mV$ to that IN/IN transition (see Figure 2).
7. The release time is the minimum time that EN must be de-asserted prior to the next IN/ \bar{IN} transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times (see Figure 3).
8. VPP (min.) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The VPP (min.) is AC limited for the E111, as a differential input as low as 50mV will still produce full ECL levels at the output.
9. VCMR is defined as the range within which the V_{IL} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to VPP (min.).

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E111JC	J28-1	Commercial
SY10E111JCTR	J28-1	Commercial
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SY100E111JCTR	J28-1	Commercial