To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M62230FP

LCD MATRIX REGULATOR

DESCRIPTION

The M62230FP is a semiconductor circuit for LCD matrix regulator, which will generate the diveded-voltage to drive LCD matrix.

By changing the connection of R pin(i.e.,Change the internal resistor ratio), M62230FP can support divided voltage ratio ranging from 1/5 bias to 1/13 bias.

The high stability and any desired voltage levels is possible, since the variable voltage regulator for Vref is built-in.

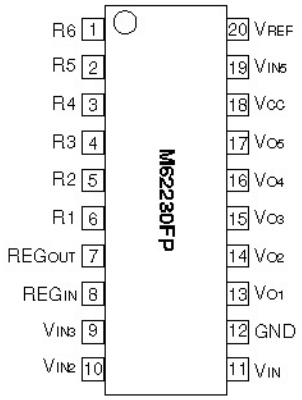
FEATURES

- Adjustable type voltage divider.
  (The setting range of internal resistor is from 1/5 bias to 1/13 bias)
- 5 resident buffer-Amp. (5 divided output)
- Low power dissipation(1.8 mA Typ.)
- Resident voltage-variable regulator for Vref.

APPLICATION

To drive LCD.

PIN CONFIGURATION (TOP VIEW)



Outline 20P2N-A

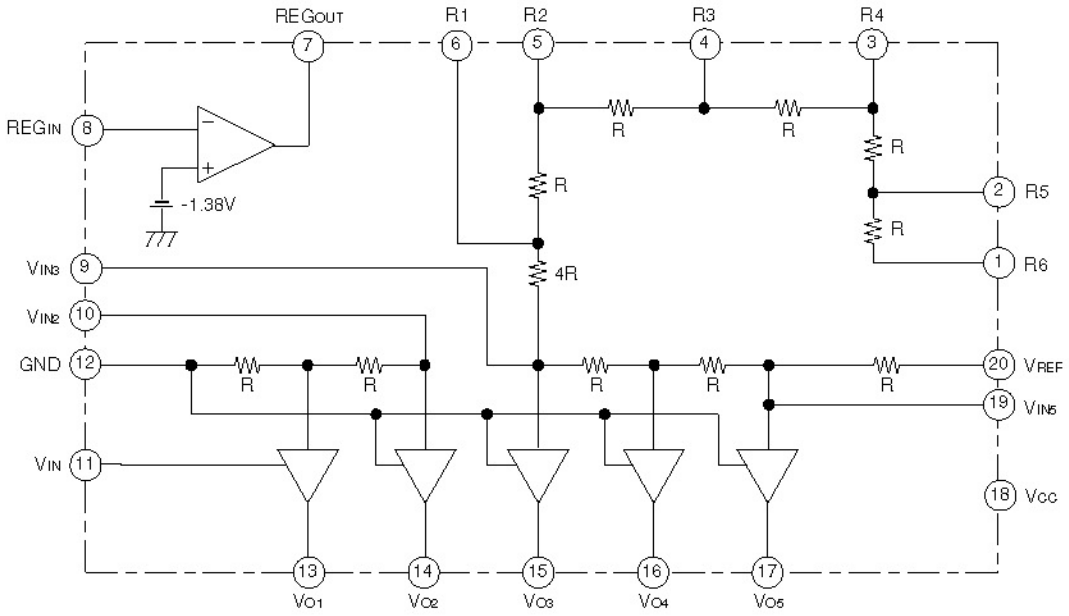
RECOMMEND OPERATING CONDITIONS (Ta=25°C)

Supply voltage range : GND-Vcc :(if V 1 > -1V, it is necessary to support V IN)..... -30 to -10V

Recommend input voltage GND-VREF :VREF ≥ Vcc..... -30 to -6V

(To set Vcc, VREF, in order that both I 0-V2 I & I Vcc-V5 I are larger than 1V)

BLOCK DIAGRAM



EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
①	R6	If the voltage of each pin can satisfy the following condition: $V_{O6} \geq V_{O5} \geq V_{O4} \geq V_{O3} \geq V_{O2} \geq V_{O1}$ these pins will be used. Please refer to page. 4 to set the bias ratio.
②	R5	
③	R4	
④	R3	
⑤	R2	
⑥	R1	
⑦	REGOUT	Regulator output for V_{REF} to use
⑧	REGIN	The inverting input pin of REG OP-Amp
⑨	V_{IN3}	V_{IN3} Input
⑩	V_{IN2}	V_{IN2} Input
⑪	V_{IN}	V_{IN} Power — if V1 > -1.0V, it is necessary to support V_{IN} if V1 < -1.0V, this pin connect to GND
⑫	GND	GND Pin
⑬	V_{O1}	Divided-voltage output pin To set Vcc & V_{REF}, in order that $0 - V_2 \geq 1V$ To set Vcc & V_{REF}, in order that $V_5 - Vcc \geq 1V$
⑭	V_{O2}	
⑮	V_{O3}	
⑯	V_{O4}	
⑰	V_{O5}	
⑱	Vcc	Vcc Power (-Power)
⑲	V_{IN5}	V_{IN5} input
⑳	V_{REF}	Reference voltage input pin

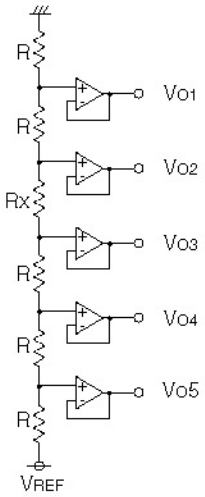
ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-36 to 0	V
I_{OUT}	Maximum output current		30	mA
P_d	Power dissipation	Ta=25°C	550	mW
K_θ	Thermal derating	Ta>25°C	5.5	mW/°C
T_{opr}	Operating temperature		-20 to +75	°C
T_{stg}	Storage temperature		-40 to +125	°C

ELECTRICAL CHARACTERISTICS (V_{CC}=-16V, V_{IN}=GND, V_{REF}=-12V, Resistor setting=5R, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage		-35		-10	V
I_{CC}	Dissipation current	V_{REF}= -16V		1.80		mA
R_{VO1}	Output voltage ratio 1	V2/V1	1.98	2.00	2.02	
R_{VO2}	Output voltage ratio 2	(V5-V3)/(V5-V4)	1.98	2.00	2.02	
R_{VO3}	Output voltage ratio 3	V5/V1	8.90	9.00	9.10	
R_{VO4}	Output voltage ratio 4	V5/V2	4.45	4.50	4.55	
R_{VO5}	Output voltage ratio 5	V5/(V5-V3)	4.45	4.50	4.55	
R_{VO6}	Output voltage ratio 6	V5/(V5-V4)	8.90	9.00	9.10	
R_{R1}	Resistor ratio 1	Resistor between V_{IN3} and R_1/ resistor between R_1 and R_2		4		
R_{R2}	Resistor ratio 2	Resistor between V_{IN3} and R_2/ resistor between R_1 and R_2		5		
R_{R3}	Resistor ratio 3	Resistor between V_{IN3} and R_3/ resistor between R_1 and R_2		6		
R_{R4}	Resistor ratio 4	Resistor between V_{IN3} and R_4/ resistor between R_1 and R_2		7		
R_{R5}	Resistor ratio 5	Resistor between V_{IN3} and R_5/ resistor between R_1 and R_2		8		
R_{R6}	Resistor ratio 6	Resistor between V_{IN3} and R_6/ resistor between R_1 and R_2		9		
R	Resistance	Resistor between R_1 and R_2		20		kΩ
ΔV1	Load regulation of output voltage 1	+200μA<I_{OUT1}<+10mA			20	mV
ΔV2-1	Load regulation of output voltage 2-1	+200μA<I_{OUT2}<+10mA			20	mV
ΔV3-1	Load regulation of output voltage 3-1	+200μA<I_{OUT3}<+10mA			20	mV
ΔV2-2	Load regulation of output voltage 2-2	-10mA<I_{OUT2}<-200μA			20	mV
ΔV3-2	Load regulation of output voltage 3-2	-10mA<I_{OUT3}<-200μA			20	mV
ΔV4	Load regulation of output voltage 4	-20mA<I_{OUT4}<-200μA			20	mV
ΔV5	Load regulation of output voltage 5	-20mA<I_{OUT5}<-200μA			20	mV
V_{REG}	Output voltage of regulator	Buffer output	-1.45	-1.38	-1.31	V
R_{EG-L}	Load regulation of V_{REF}	-10mA<I_{REG}<+2mA			50	mV

THE SETTING METHOD OF DIVIDED-VOLTAGE



Rx	Bias ratio	Example of setting
R	1/5	⑨pin-⑥pin short, ⑩pin-⑤pin short
2R	1/6	⑨pin-⑥pin short, ⑩pin-④pin short
3R	1/7	⑨pin-⑥pin short, ⑩pin-③pin short
4R	1/8	⑩pin-⑥pin short
5R	1/9	⑩pin-⑤pin short
6R	1/10	⑩pin-④pin short
7R	1/11	⑩pin-③pin short
8R	1/12	⑩pin-②pin short
9R	1/13	⑩pin-①pin short