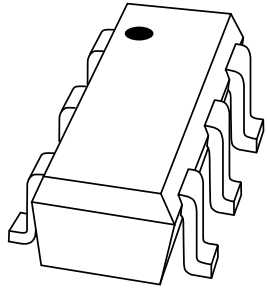


# DATA SHEET



**BF1204**

Dual N-channel dual gate  
MOS-FET

Product specification  
Supersedes data of 2001 Apr 25

2010 Sep 16



## Dual N-channel dual gate MOS-FET

BF1204

## FEATURES

- Two low noise gain controlled amplifiers in a single package
- Superior cross-modulation performance during AGC
- High forward transfer admittance
- High forward transfer admittance to input capacitance ratio.

## APPLICATIONS

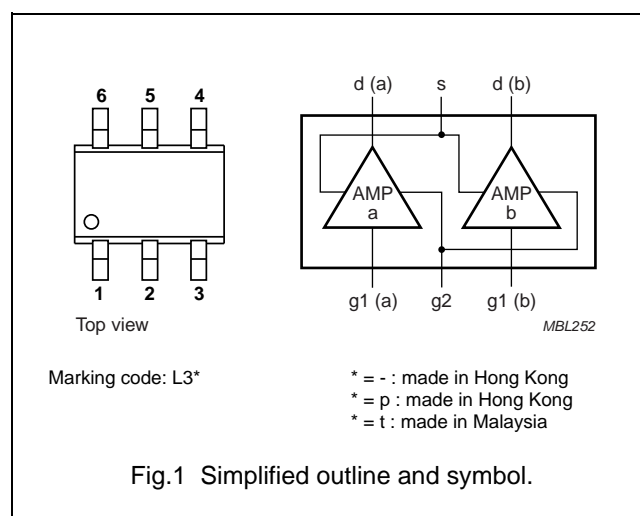
- Gain controlled low noise amplifiers for VHF and UHF applications with 3 to 9 V supply voltage, such as digital and analog television tuners and professional communications equipment.

## DESCRIPTION

The BF1204 is a combination of two equal dual gate MOS-FET amplifiers with shared source and gate 2 leads. The source and substrate are interconnected. Internal bias circuits enable DC stabilization and a very good cross-modulation performance during AGC. Integrated diodes between the gates and source protect against excessive input voltage surges. The transistor has a SOT363 micro-miniature plastic package.

## PINNING - SOT363

PIN	DESCRIPTION
1	gate 1 (a)
2	gate 2
3	gate 1 (b)
4	drain (b)
5	source
6	drain (a)



## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per MOS-FET; unless otherwise specified						
$V_{DS}$	drain-source voltage		–	–	10	V
$I_D$	drain current (DC)		–	–	30	mA
$P_{tot}$	total power dissipation	$T_s \leq 102\text{ }^\circ\text{C}$ ; note 1	–	–	200	mW
$ y_{fs} $	forward transfer admittance	$I_D = 12\text{ mA}$ ; $f = 1\text{ MHz}$	25	30	40	mS
$C_{ig1-s}$	input capacitance at gate 1	$I_D = 12\text{ mA}$ ; $f = 1\text{ MHz}$	–	1.7	2.2	pF
$C_{rss}$	reverse transfer capacitance	$f = 1\text{ MHz}$	–	15	–	fF
NF	noise figure	$f = 800\text{ MHz}$	–	1.1	1.8	dB
$X_{mod}$	cross-modulation	input level for $k = 1\%$ at 40 dB AGC	100	105	–	dB $\mu$ V
$T_j$	operating junction temperature		–	–	150	$^\circ\text{C}$

## Note

1.  $T_s$  is the temperature at the soldering point of the source lead.

## CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling.

## Dual N-channel dual gate MOS-FET

BF1204

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per MOS-FET; unless otherwise specified</b>					
$V_{DS}$	drain-source voltage		–	10	V
$I_D$	drain current (DC)		–	30	mA
$I_{G1}$	gate 1 current		–	$\pm 10$	mA
$I_{G2}$	gate 2 current		–	$\pm 10$	mA
$P_{tot}$	total power dissipation	$T_s \leq 102\text{ }^{\circ}\text{C}$	–	200	mW
$T_{stg}$	storage temperature		–65	+150	$^{\circ}\text{C}$
$T_j$	operating junction temperature		–	150	$^{\circ}\text{C}$

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	240	K/W

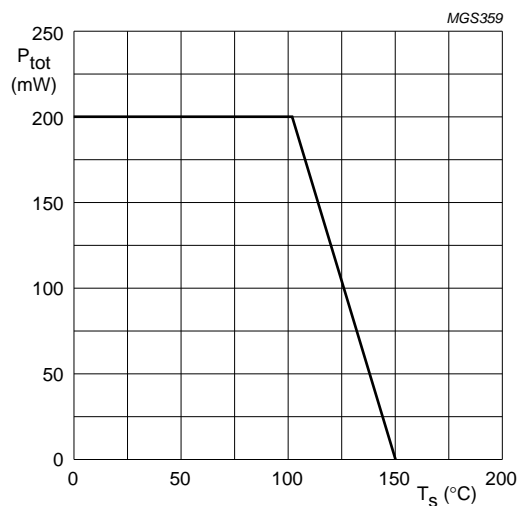


Fig.2 Power derating curve.

## Dual N-channel dual gate MOS-FET

BF1204

## STATIC CHARACTERISTICS

 $T_j = 25\text{ }^{\circ}\text{C}$ ; per MOS-FET; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0$ ; $I_D = 10\text{ }\mu\text{A}$	10	–	V
$V_{(BR)G1-SS}$	gate-source breakdown voltage	$V_{GS} = V_{DS} = 0$ ; $I_{G1-S} = 10\text{ mA}$	6	10	V
$V_{(BR)G2-SS}$	gate-source breakdown voltage	$V_{GS} = V_{DS} = 0$ ; $I_{G2-S} = 10\text{ mA}$	6	10	V
$V_{(F)S-G1}$	forward source-gate voltage	$V_{G2-S} = V_{DS} = 0$ ; $I_{S-G1} = 10\text{ mA}$	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate voltage	$V_{G1-S} = V_{DS} = 0$ ; $I_{S-G2} = 10\text{ mA}$	0.5	1.5	V
$V_{G1-S(th)}$	gate-source threshold voltage	$V_{DS} = 5\text{ V}$ ; $V_{G2-S} = 4\text{ V}$ ; $I_D = 100\text{ }\mu\text{A}$	0.3	1	V
$V_{G2-S(th)}$	gate-source threshold voltage	$V_{DS} = 5\text{ V}$ ; $V_{G1-S} = 4\text{ V}$ ; $I_D = 100\text{ }\mu\text{A}$	0.3	1.2	V
$I_{DSX}$	drain-source current	$V_{G2-S} = 4\text{ V}$ ; $V_{DS} = 5\text{ V}$ ; $R_G = 120\text{ k}\Omega$ ; note 1	8	16	mA
$I_{G1-S}$	gate cut-off current	$V_{G1-S} = 5\text{ V}$ ; $V_{G2-S} = V_{DS} = 0$	–	50	nA
$I_{G2-S}$	gate cut-off current	$V_{G2-S} = 4\text{ V}$ ; $V_{G1-S} = V_{DS} = 0$	–	20	nA

## Note

1.  $R_{G1}$  connects gate 1 to  $V_{GG} = 5\text{ V}$ .

## DYNAMIC CHARACTERISTICS

Common source;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $V_{DS} = 5\text{ V}$ ;  $I_D = 12\text{ mA}$ ; per MOS-FET <sup>(1)</sup>; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	$T_j = 25\text{ }^{\circ}\text{C}$	25	30	40	mS
$C_{ig1-ss}$	input capacitance at gate 1	$f = 1\text{ MHz}$	–	1.7	2.2	pF
$C_{ig2-ss}$	input capacitance at gate 2	$f = 1\text{ MHz}$	–	3.3	–	pF
$C_{oss}$	output capacitance	$f = 1\text{ MHz}$	–	0.85	–	pF
$C_{rss}$	reverse transfer capacitance	$f = 1\text{ MHz}$	–	15	–	fF
$G_{tr}$	power gain	$f = 200\text{ MHz}$ ; $G_S = 2\text{ mS}$ ; $B_S = B_{S(opt)}$ ; $G_L = 0.5\text{ mS}$ ; $B_L = B_{L(opt)}$ ; note 1	30	34	38	dB
		$f = 400\text{ MHz}$ ; $G_S = 2\text{ mS}$ ; $B_S = B_{S(opt)}$ ; $G_L = 1\text{ mS}$ ; $B_L = B_{L(opt)}$ ; note 1	26	30	34	dB
		$f = 800\text{ MHz}$ ; $G_S = 3.3\text{ mS}$ ; $B_S = B_{S(opt)}$ ; $G_L = 1\text{ mS}$ ; $B_L = B_{L(opt)}$ ; note 1	21	25	29	dB
NF	noise figure	$f = 10.7\text{ MHz}$ ; $G_S = 20\text{ mS}$ ; $B_S = 0$	–	9	11	dB
		$f = 400\text{ MHz}$ ; $Y_S = Y_{S(opt)}$	–	0.9	1.5	dB
		$f = 800\text{ MHz}$ ; $Y_S = Y_{S(opt)}$	–	1.1	1.8	dB
$X_{mod}$	cross-modulation	input level for $k = 1\%$ at 0 dB AGC; $f_w = 50\text{ MHz}$ ; $f_{unw} = 60\text{ MHz}$ ; note 2	90	–	–	dB $\mu$ V
		input level for $k = 1\%$ at 10 dB AGC; $f_w = 50\text{ MHz}$ ; $f_{unw} = 60\text{ MHz}$ ; note 2	–	92	–	dB $\mu$ V
		input level for $k = 1\%$ at 40 dB AGC; $f_w = 50\text{ MHz}$ ; $f_{unw} = 60\text{ MHz}$ ; note 2	100	105	–	dB $\mu$ V

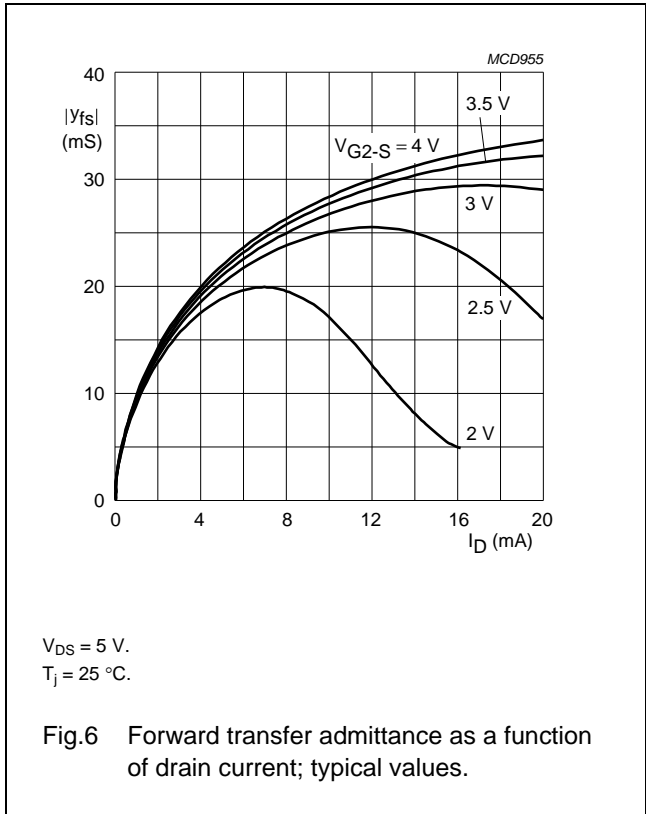
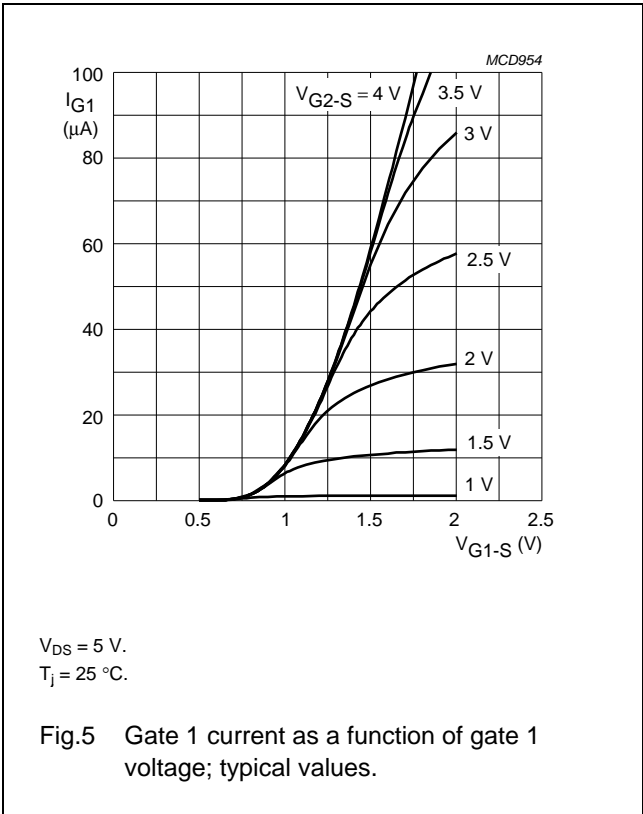
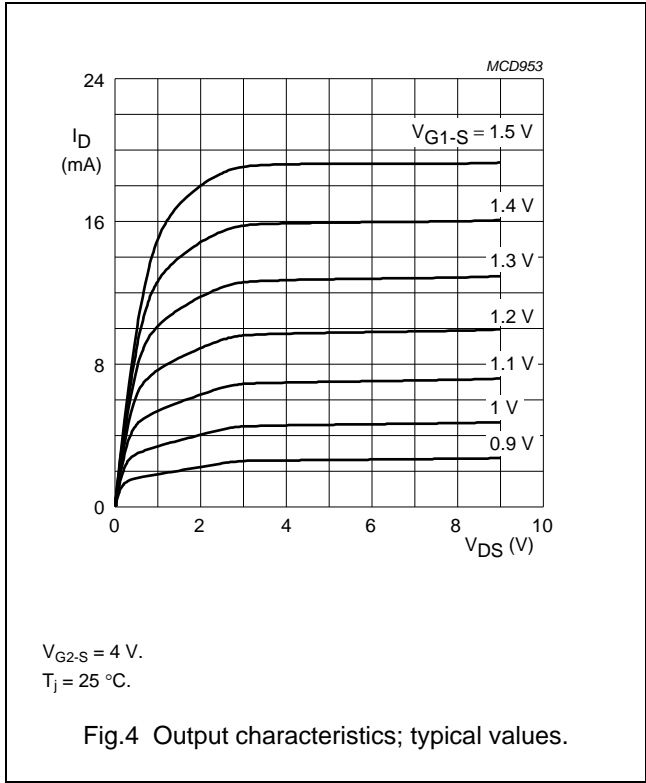
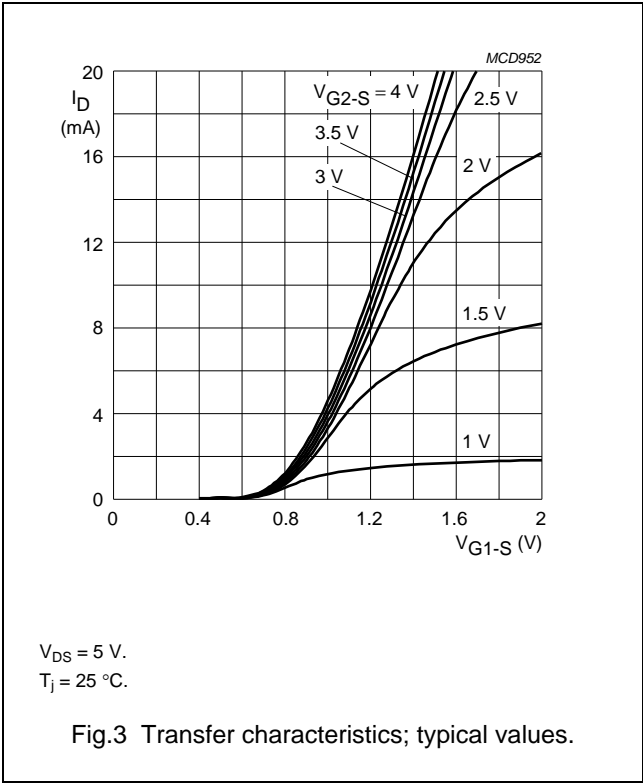
## Notes

1. For the MOS-FET not in use:  $V_{G1-S} = 0$ ;  $V_{DS} = 0$ .
2. Measured in Fig.19 test circuit.

Dual N-channel dual gate MOS-FET

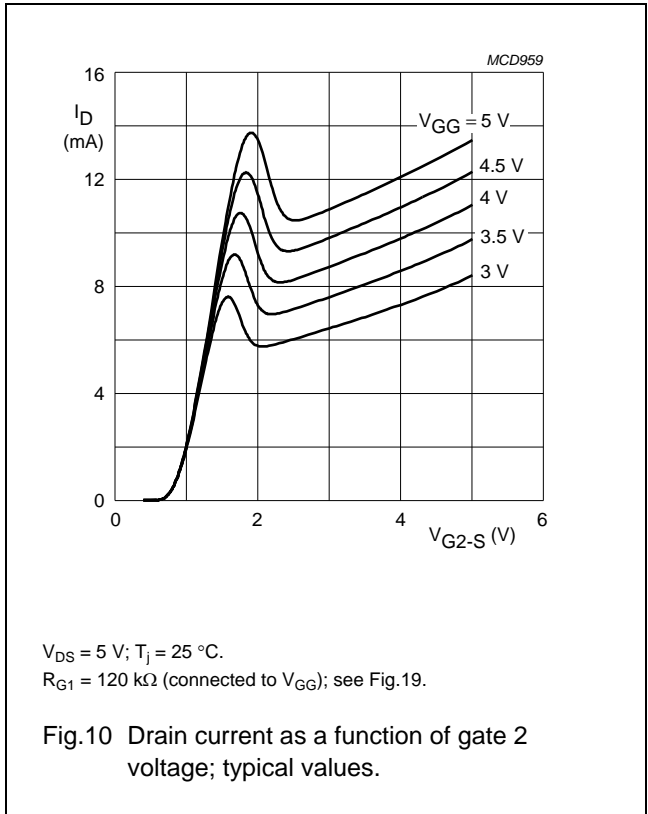
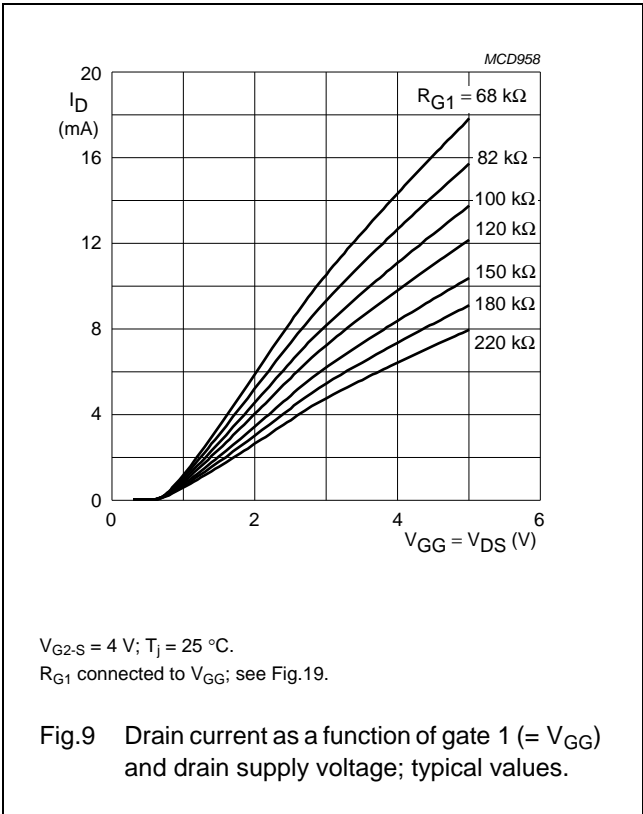
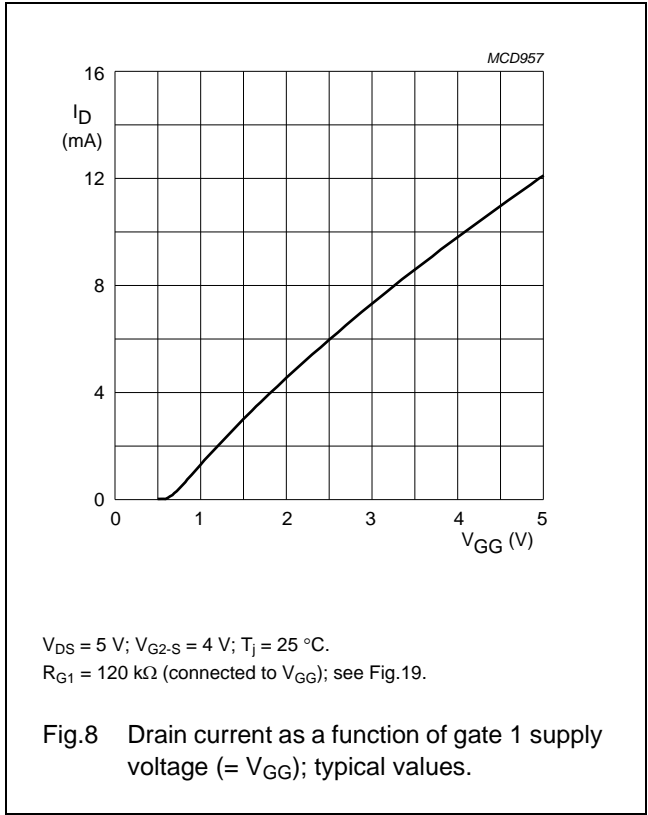
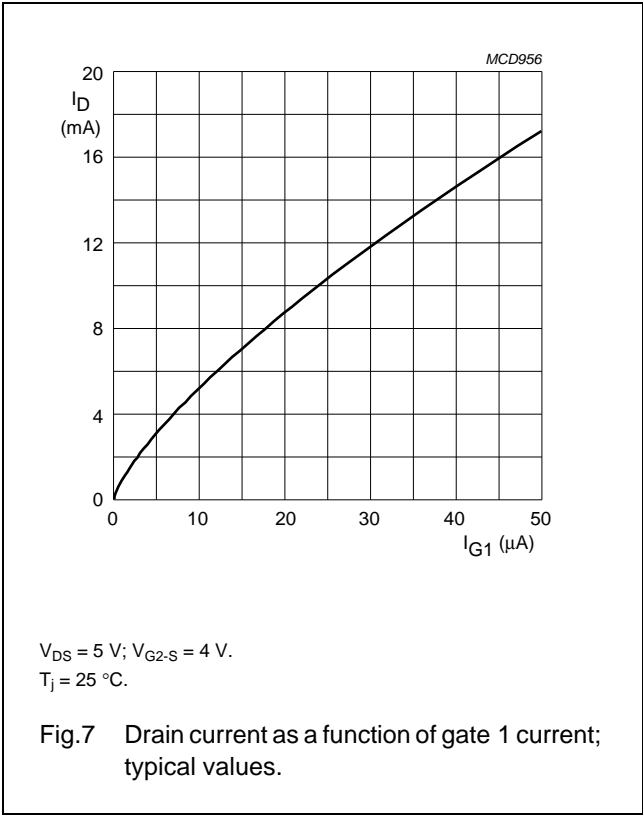
BF1204

ALL GRAPHS FOR ONE MOS-FET



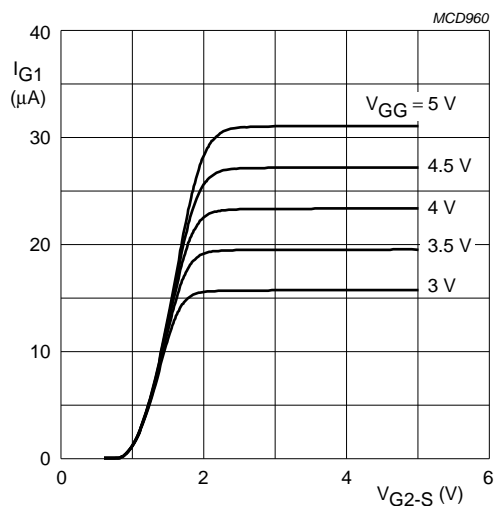
Dual N-channel dual gate MOS-FET

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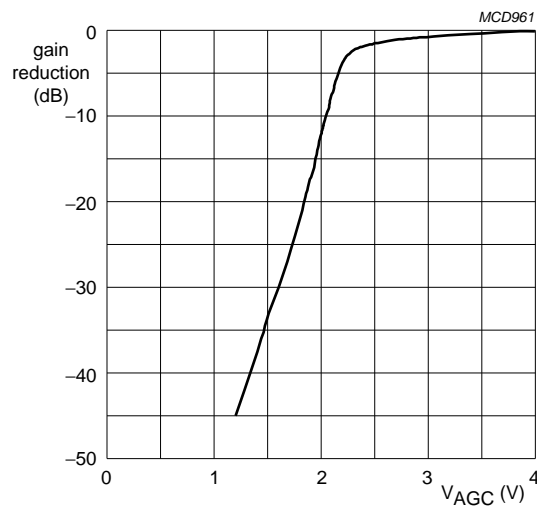
## Dual N-channel dual gate MOS-FET

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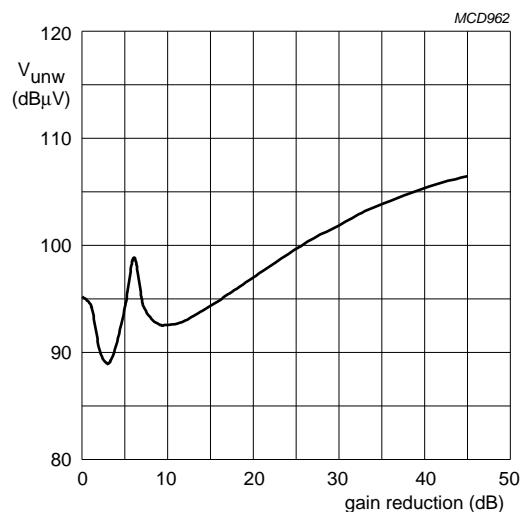
$V_{DS} = 5 V$ ;  $T_j = 25 ^\circ C$ .  
 $R_{G1} = 120 k\Omega$  (connected to  $V_{GG}$ ); see Fig.19.

Fig.11 Gate 1 current as a function of gate 2 voltage; typical values.



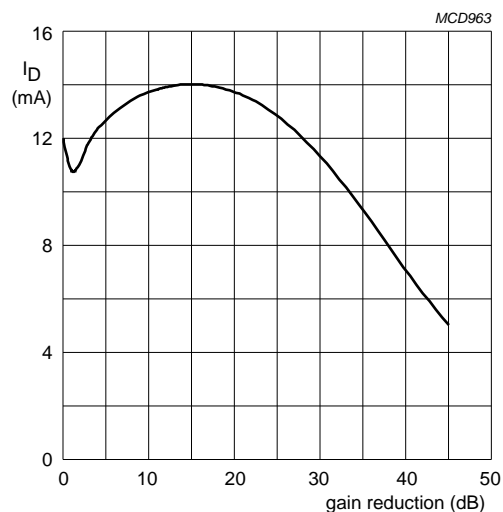
$V_{DS} = 5 V$ ;  $V_{GG} = 5 V$ ;  $R_{G1} = 120 k\Omega$ ;  
 $f = 50 MHz$ ;  $T_{amb} = 25 ^\circ C$ .

Fig.12 Typical gain reduction as a function of AGC voltage; see Fig.19.



$V_{DS} = 5 V$ ;  $V_{GG} = 5 V$ ;  $R_{G1} = 120 k\Omega$ ;  
 $f = 50 MHz$ ;  $f_{unw} = 60 MHz$ ;  $T_{amb} = 25 ^\circ C$ .

Fig.13 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.19.

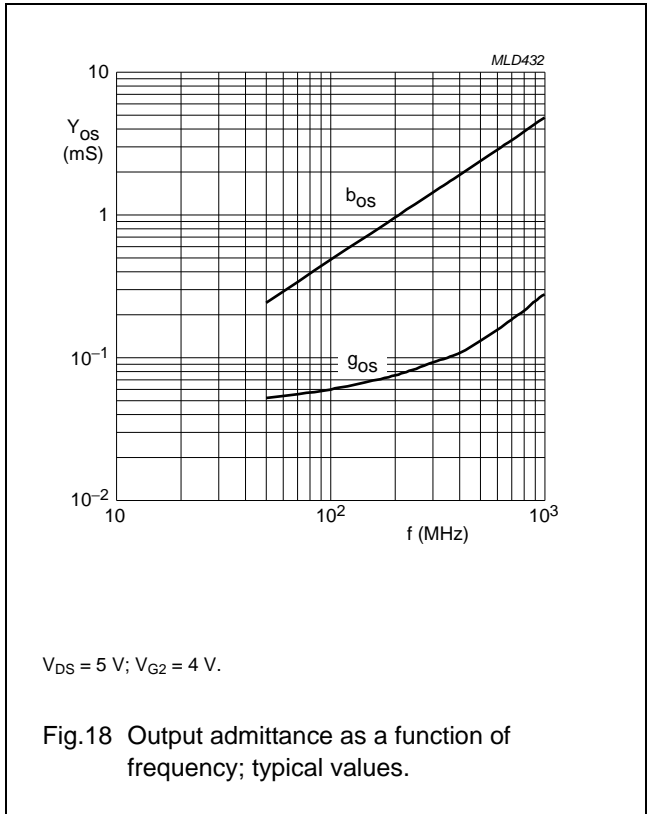
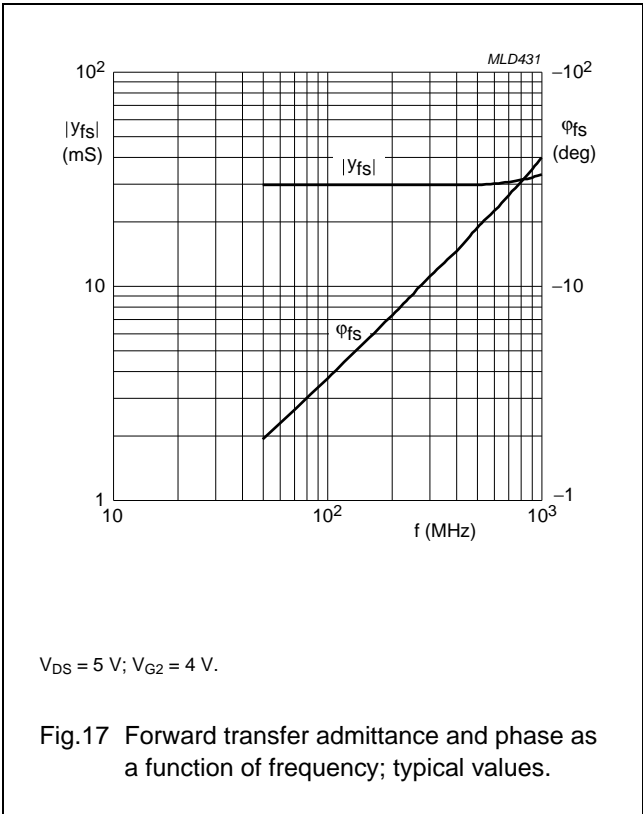
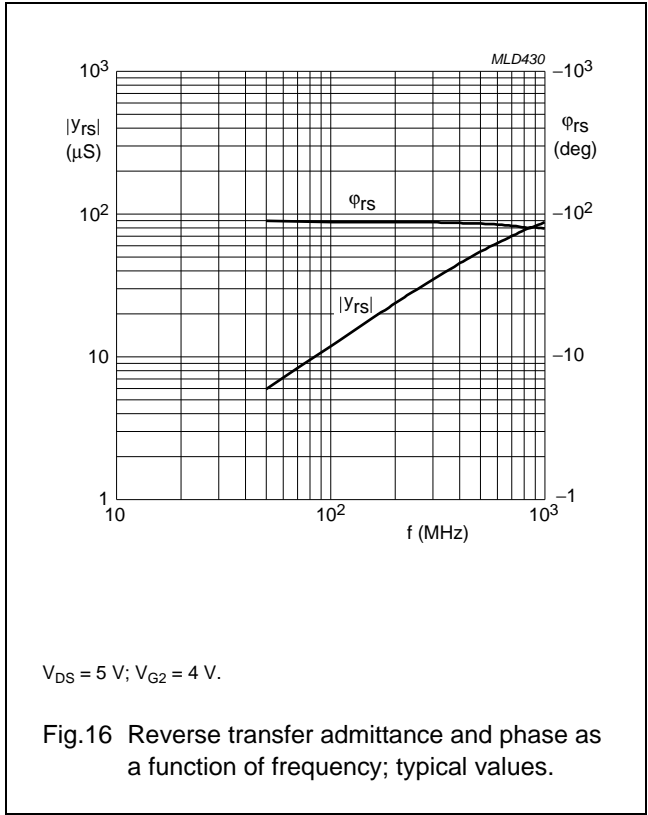
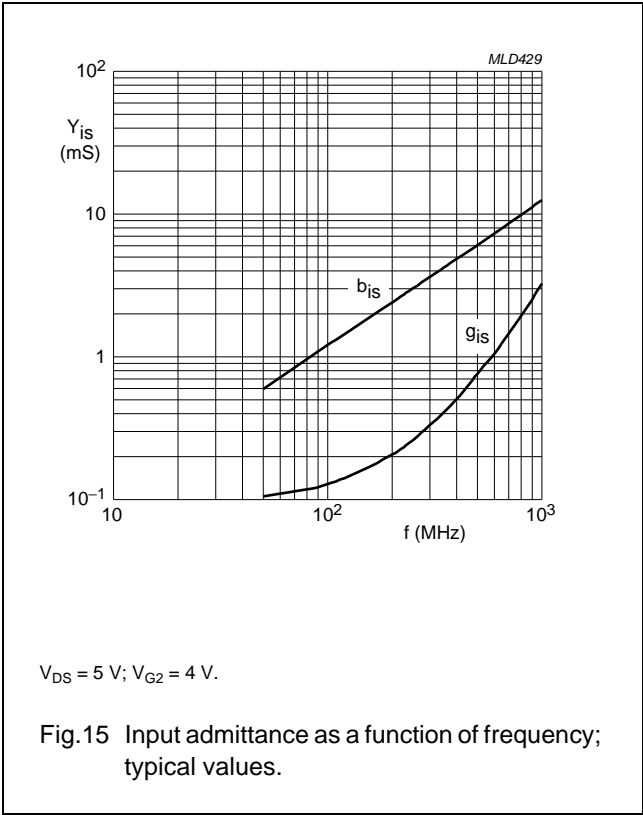


$V_{DS} = 5 V$ ;  $V_{GG} = 5 V$ ;  $R_{G1} = 120 k\Omega$ ;  
 $f = 50 MHz$ ;  $T_{amb} = 25 ^\circ C$ .

Fig.14 Drain current as a function of gain reduction; typical values; see Fig.19.

Dual N-channel dual gate MOS-FET

BF1204





Dual N-channel dual gate MOS-FET

BF1204

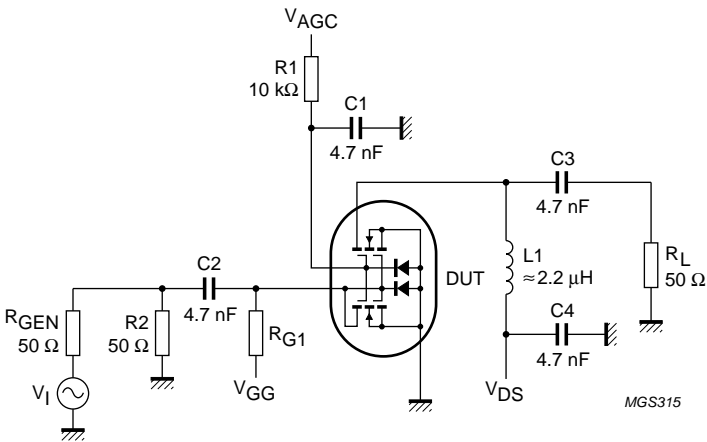


Fig.19 Cross-modulation test set-up (for one MOS-FET).

Scattering parameters

$V_{DS} = 5\text{ V}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $I_D = 12\text{ mA}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

f (MHz)	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.991	−3.29	2.95	175.78	0.00060	85.25	0.995	−1.44
100	0.987	−7.12	2.90	171.61	0.00119	84.74	0.994	−2.90
200	0.981	−14.21	2.86	163.45	0.00234	80.85	0.992	−5.70
300	0.969	−21.22	2.83	155.11	0.00339	75.77	0.989	−8.50
400	0.958	−28.14	2.79	147.37	0.00429	72.23	0.987	−11.25
500	0.939	−35.01	2.74	139.04	0.00508	68.24	0.983	−13.96
600	0.921	−41.75	2.68	131.35	0.00565	64.97	0.981	−16.67
700	0.898	−48.51	2.62	123.38	0.00611	61.90	0.976	−19.36
800	0.874	−54.96	2.55	115.74	0.00646	57.77	0.973	−22.04
900	0.847	−61.62	2.49	107.84	0.00662	55.04	0.969	−24.80
1000	0.817	−67.84	2.41	100.24	0.00670	52.16	0.966	−27.45

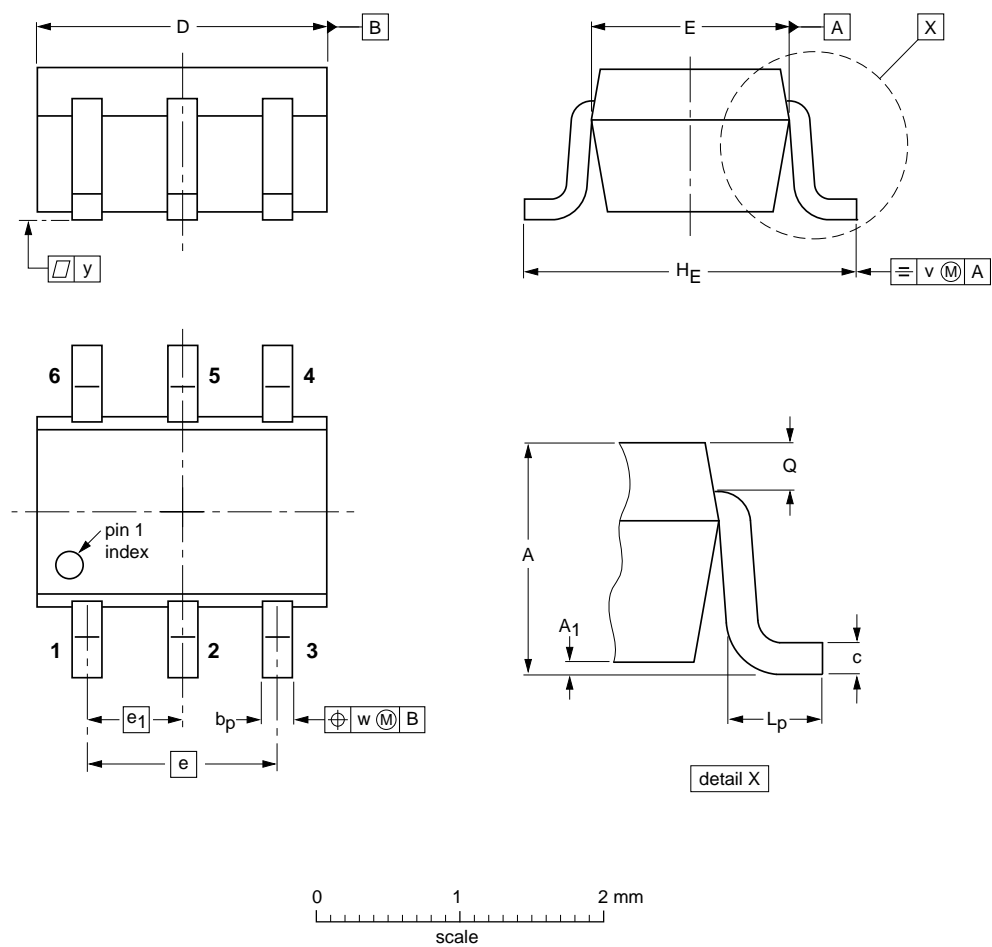
Dual N-channel dual gate MOS-FET

BF1204

PACKAGE OUTLINE


Plastic surface-mounted package; 6 leads

SOT363



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT363			SC-88			04-11-08 06-03-16

## Dual N-channel dual gate MOS-FET

BF1204

## DATA SHEET STATUS

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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Dual N-channel dual gate MOS-FET

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BF1204

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## **Contact information**

For additional information please visit: <http://www.nxp.com>

For sales offices addresses send e-mail to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

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