# CAT24C21

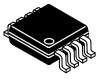
# 1 kb Dual Mode Serial EEPROM for VESA™ “Plug-and-Play”

ON Semiconductor®

http://onsemi.com

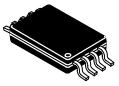
SOIC−8
W SUFFIX
CASE 751BD

TDFN−8
ZD4 SUFFIX
CASE 511AL



MSOP−8
Z SUFFIX
CASE 846AD

PDIP−8
L SUFFIX
CASE 646AA



TSSOP−8
Y SUFFIX
CASE 948AL

### Description

The CAT24C21 is a 1 kb Serial CMOS EEPROM internally organized as 128 words of 8 bits each. The device complies with the Video Electronics Standard Association’s (VESA™), Display Data Channel (DDC™) standards for “Plug−and−Play” monitors. The “transmit−only” mode (DDC1™) is controlled by the VCLK clock input and the “bi−directional” mode (DDC2™) is controlled by the SCL clock input, with both modes sharing a common SDA input/output (I/O). The transmit−only mode is a read−only mode, while the bi−directional mode is a read and write mode following the $I^2C$ protocol. In write mode the CAT24C21 features a 16−byte page write buffer. The device is available in 8−lead DIP, SOIC, TSSOP, MSOP and TDFN packages.

### Features

- DDC1™/DDC2™ Interface Compliant for Monitor Identification
- 400 kHz $I^2C$ Bus Compatible
- 2.5 to 5.5 Volt Operation
- 16−byte Page Write Buffer
- Hardware Write Protect
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial Temperature Range
- 8−lead DIP, SOIC, TSSOP, MSOP or TDFN Packages
- This Device is Pb−Free, Halogen Free/BFR Free, and RoHS Compliant

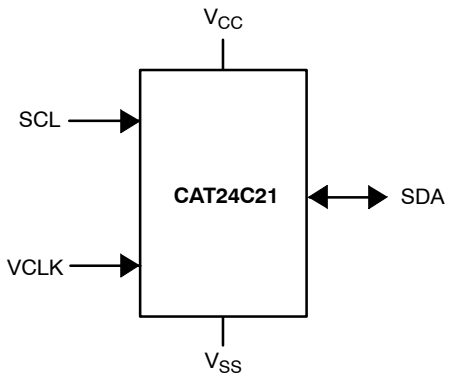
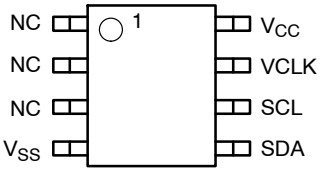



**Figure 1. Functional Symbol**

### PIN CONFIGURATION




PDIP (L), SOIC (W), TSSOP (Y),
TDFN (ZD4), MSOP (Z)

### PIN FUNCTION

| Pin Name | Function |
|---|---|
| NC | No Connect |
| SDA | Serial Data / Address |
| SCL | Serial Clock (bi−directional mode) |
| VCLK | Serial Clock (transmit−only mode) |
| $V_{CC}$ | Power Supply |
| $V_{SS}$ | Ground |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

**Table 1. ABSOLUTE MAXIMUM RATINGS**

| Parameters | Ratings | Units |
|---|---|---|
| Temperature Under Bias | –55 to +125 | °C |
| Storage Temperature | –65 to +150 | °C |
| Voltage on Any Pin with Respect to Ground (Note 1) | –2.0 to +$V_{CC}$ +2.0 | V |
| $V_{CC}$ with Respect to Ground | –2.0 to +7.0 | V |
| Package Power Dissipation Capability ($T_A$ = 25°C) | 1.0 | W |
| Lead Soldering Temperature (10 secs) | 300 | °C |
| Output Short Circuit Current (Note 2) | 100 | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The minimum DC input voltage is –0.5 V. During transitions, inputs may undershoot to –2.0 V for periods of less than 20 ns. Maximum DC voltage on output pins is $V_{CC}$ + 0.5 V, which may overshoot to $V_{CC}$ + 2.0 V for periods of less than 20 ns.
2. Output shorted for no more than one second.

**Table 2. RELIABILITY CHARACTERISTICS**

| Symbol | Parameter | Reference Test Method | Min | Units |
|---|---|---|---|---|
| $N_{END}$ (Notes 3 and 4) | Endurance | MIL–STD–883, Test Method 1033 | 1,000,000 | Program/Erase Cycles |
| $T_{DR}$ (Note 3) | Data Retention | MIL–STD–883, Test Method 1008 | 100 | Years |
| $V_{ZAP}$ (Note 3) | ESD Susceptibility | MIL–STD–883, Test Method 3015 | 2000 | Volts |
| $I_{LTH}$ (Notes 3 and 5) | Latch–up | JEDEC Standard 17 | 100 | mA |

3. This parameter is tested initially and after a design or process change that affects the parameter.
4. Page Mode, $V_{CC}$ = 5 V, 25°C
5. Latch–up protection is provided for stresses up to 100 mA on address and data pins from –1 V to $V_{CC}$ +1 V.

**Table 3. D.C. OPERATING CHARACTERISTICS** ($V_{CC}$ = 2.5 V to 5.5 V, unless otherwise specified. Industrial temperature range.)

| Symbol | Parameter | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $I_{CC}$ | Power Supply Current | $f_{SCL}$ = 400 kHz | | 2 | mA |
| $I_{SB}$ (Note 6) | Standby Current | $V_{IN}$ = GND or $V_{CC}$ | | 1 | μA |
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = GND to $V_{CC}$ | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = GND to $V_{CC}$ | | 10 | μA |
| $V_{IL}$ | Input Low Voltage | | –1 | $V_{CC}$ x 0.3 | V |
| $V_{IH}$ | Input High Voltage | | $V_{CC}$ x 0.7 | $V_{CC}$ + 0.5 | V |
| $V_{OL1}$ | Output Low Voltage | $V_{CC}$ = 3.0 V, $I_{OL}$ = 3 mA | | 0.4 | V |
| $V_{IL}$ | Input Low Voltage (VCLK) | $V_{CC} \geq$ 2.7 V | | 0.8 | V |
| $V_{IH}$ | Input High Voltage (VCLK) | | 2.0 | | V |

6. Maximum standby current ($I_{SB}$) = 10 μA for the Extended Automotive temperature range.

**Table 4. CAPACITANCE** ($T_A$ = 25°C, f = 1.0 MHz, $V_{CC}$ = 5 V)

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $C_{I/O}$ (Note 7) | Input/Output Capacitance (SDA) | $V_{I/O}$ = 0 V | | 8 | pF |
| $C_{IN}$ (Note 7) | Input Capacitance (VCLK, SCL) | $V_{IN}$ = 0 V | | 6 | pF |

7. This parameter is tested initially and after a design or process change that affects the parameter.

**Table 5. A.C. CHARACTERISTICS** ($V_{CC}$ = 2.5 V to 5.5 V, unless otherwise specified. Industrial temperature range.)

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| **TRANSMIT−ONLY MODE** | | | | |
| $T_{VAA}$ | Output valid from VCLK | | 0.5 | μs |
| $T_{VHIGH}$ | VCLK high | 0.6 | | μs |
| $T_{VLOW}$ | VCLK low | 1.3 | | μs |
| $T_{VHZ}$ | Mode transition | | 0.5 | μs |
| $T_{VPU}$ | Transmit−only power−up | 0 | | ns |
| **READ & WRITE CYCLE LIMITS** | | | | |
| $F_{SCL}$ | Clock Frequency | | 400 | kHz |
| $T_I$ (Note 8) | Noise Suppression Time Constant at SCL, SDA Inputs | | 100 | ns |
| $t_{AA}$ | SCL Low to SDA Data Out and ACK Out | | 1 | μs |
| $t_{BUF}$ (Note 8) | Time the Bus Must be Free Before a New Transmission Can Start | 1.2 | | μs |
| $t_{HD:STA}$ | Start Condition Hold Time | 0.6 | | μs |
| $t_{LOW}$ | Clock Low Period | 1.2 | | μs |
| $t_{HIGH}$ | Clock High Period | 0.6 | | μs |
| $t_{SU:STA}$ | Start Condition Setup Time | 0.6 | | μs |
| $t_{HD:DAT}$ | Data In Hold Time | 0 | | ns |
| $t_{SU:DAT}$ | Data In Setup Time | 50 | | ns |
| $t_R$ (Note 8) | SDA and SCL Rise Time | | 0.3 | μs |
| $t_F$ (Note 8) | SDA and SCL Fall Time | | 300 | ns |
| $t_{SU:STO}$ | Stop Condition Setup Time | 0.6 | | μs |
| $t_{DH}$ | Data Out Hold Time | 100 | | ns |
| **POWER−UP TIMING** (Note 8 and 9) | | | | |
| $t_{PUR}$ | Power−up to Read Operation | | 1 | ms |
| $t_{PUW}$ | Power−up to Write Operation | | 1 | ms |
| **WRITE CYCLE LIMITS** | | | | |
| $t_{WR}$ | Write Cycle Time | | 5 | ms |

8. This parameter is tested initially and after a design or process change that affects the parameter.
9. $t_{PUR}$ and $t_{PUW}$ are the delays required from the time $V_{CC}$ is stable until the specified operation can be initiated.

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

### Pin Description

The SCL serial clock input pin is used to clock all data transfers into or out of the device when in the bi−directional mode.

The SDA bi−directional serial data/address pin is used to transfer data into and out of the device. The SDA pin is an open drain output and can be wire−ORed with other open drain or open collector outputs.

### Functional Description

The CAT24C21 has two modes of operation: the transmit−only mode and the bi−directional mode. There is a separate 2−wire protocol to support each mode, each having a separate clock input (VCLK and SCL respectively) and both modes sharing a common bi−directional data line (SDA). The CAT24C21 enters the transmit−only mode upon power up and begins outputting data on the SDA pin with each clock signal on the VCLK pin. The device will remain in the transmit−only mode until there is a valid HIGH to LOW transition on the SCL pin, when it will switch to the bi−directional mode (Figure 2). Once in the bi−directional mode, the only way to return to the transmit−only mode is by powering down the device.

The VCLK serial clock input pin is used to clock data out of the device when in transmit−only mode. When held low, in bi−directional mode, it will inhibit write operations.

**Transmit−Only Mode: (DDC1)**

Upon power−up, the CAT24C21 will output valid data only after it has been initialized. During initialization, data will not be available until after the first nine clocks are sent to the device (Figure 3). The starting address for the transmit−only mode can be determined during initialization. If the SDA pin is high during the first eight clocks, the starting address will be 7FH. If the SDA pin is low during the first eight clocks, the starting address will be 00H. During the ninth clock, SDA will be in the high impedance state.

Data is transmitted in 8 bit words with the most significant bit first, followed by a 9th ‘don’t care’ bit which will be in the high impedance state (Figure 4). The CAT24C21 will continuously sequence through the entire memory array as long as VCLK is present and no falling edges on SCL are detected. When the maximum address (7FH) is reached, addressing will wrap around to the zero location (00H) and transmitting will continue. The bi−directional mode clock (SCL) pin must be held high for the device to remain in the transmit−only mode.

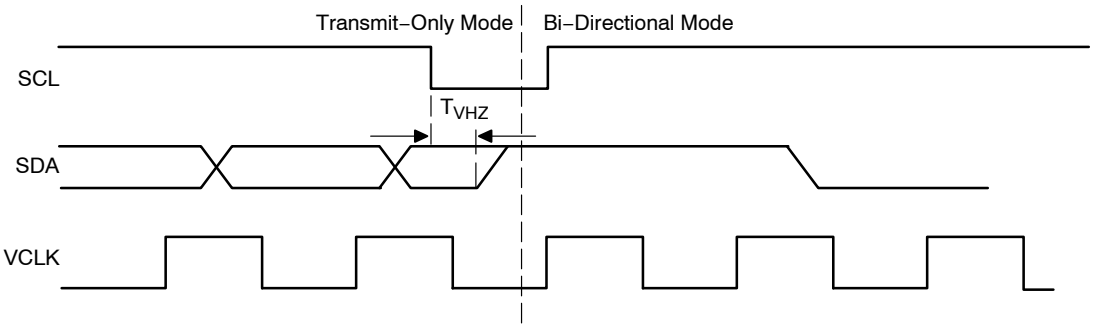



**Figure 2. Mode Transition**

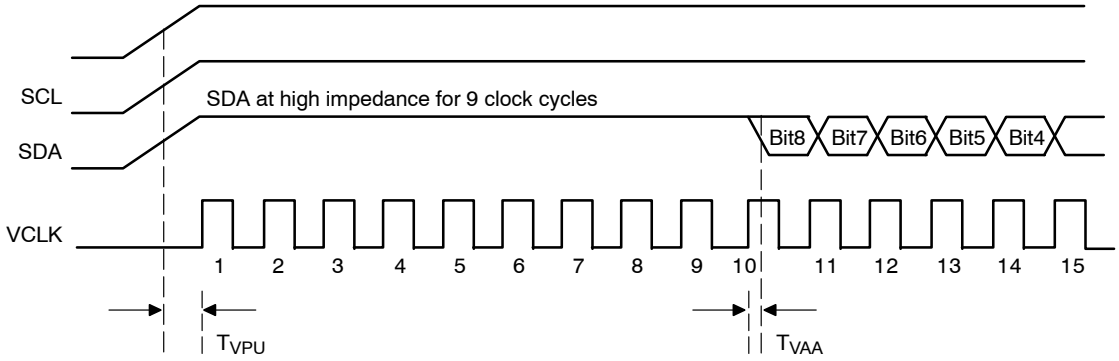



**Figure 3. Device Initialization for Transmit−only Mode**

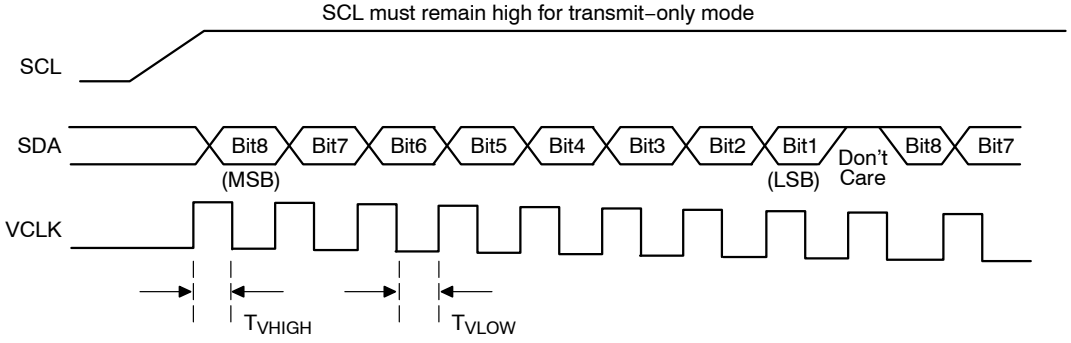



**Figure 4. Transmit−Only Mode**

### Bi−Directional Mode (DDC2)

The following defines the features of the $I^2C$ bus protocol in bi−directional mode (Figure 5):

1. Data transfer may be initiated only when the bus is not busy.
2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

When in the bi−directional mode, all inputs to the VCLK pin are ignored, except when a logic high is required to enable write capability.

### START Condition

The START condition (Figure 7) precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24C21 monitors the SDA and SCL lines and will not respond until this condition is met.

### STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

### Device Addressing

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The four most significant bits of the 8−bit slave address are fixed as 1010 for the CAT24C21 (see Figure 9). The next three significant bits are “don’t care”. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition and the slave address byte, the CAT24C21 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24C21 then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

### Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge (ACK). The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it has received the 8 bits of data (Figure 8).

The CAT24C21 responds with an ACK after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an ACK after receiving each 8−bit byte.

When the CAT24C21 is in a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an ACK. Once it receives this ACK, the CAT24C21 will continue to transmit data. If no ACK is sent by the Master, the device terminates data transmission and waits for a STOP condition.

### Write Operations

VCLK must be held high in order to program the device. This applies to byte write and page write operation. Once the device is in its self−timed program cycle, VCLK can go low and not affect programming.

### Byte Write

In the Byte Write mode (Figure 10), the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an ACK, the Master sends the byte address that is to be written into the address pointer of the CAT24C21. After receiving another ACK from the Slave, the Master device transmits the data byte to be written into the addressed memory location. The CAT24C21 acknowledges once more and the Master generates the STOP condition, at which time the device begins its internal programming cycle to nonvolatile memory (Figure 6). While this internal cycle is in progress, the device will not respond to any request from the Master device.

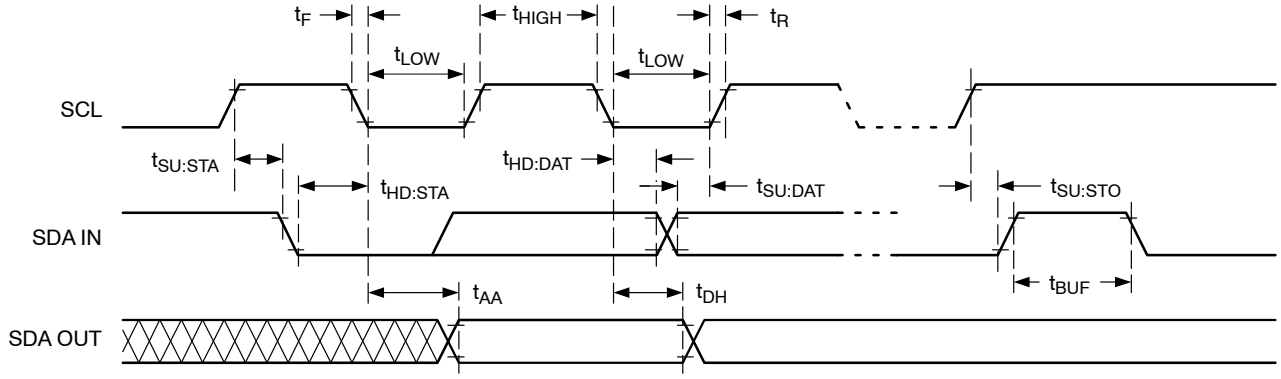



**Figure 5. Bus Timing**

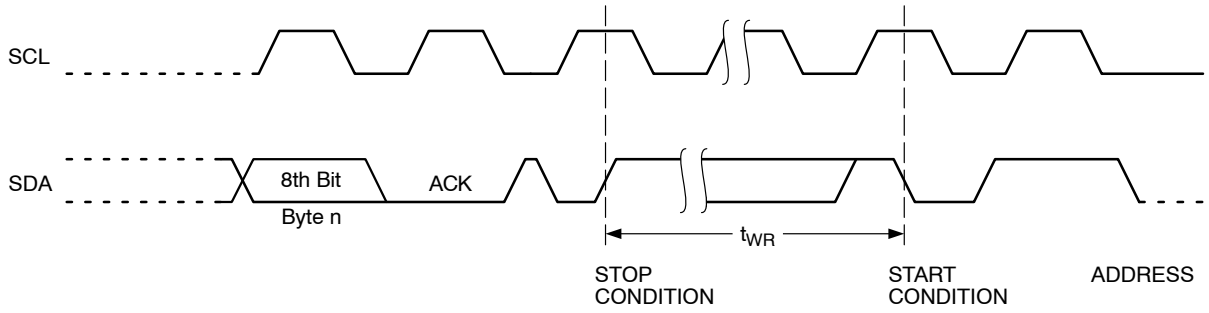



**Figure 6. Write Cycle Timing**

### Page Write

The CAT24C21 writes up to 16 bytes of data in a single write cycle, using the Page Write operation. The Page Write operation (Figure 11) is initiated in the same manner as the Byte Write operation, however instead of terminating after the initial word is transmitted, the Master is allowed to send up to fifteen additional bytes. After each byte has been transmitted the CAT24C21 will respond with an ACK, and internally increment the low order address bits by one. The high order bits remain unchanged.

If the Master transmits more than sixteen bytes prior to sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

Once all sixteen bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point all received data is written to the CAT24C21 in a single write cycle.

### Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24C21 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24C21 is still busy with the write operation, no ACK will be returned. If the CAT24C21 has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

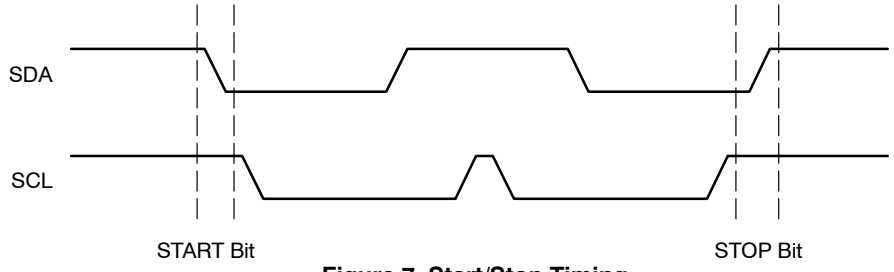



**Figure 7. Start/Stop Timing**

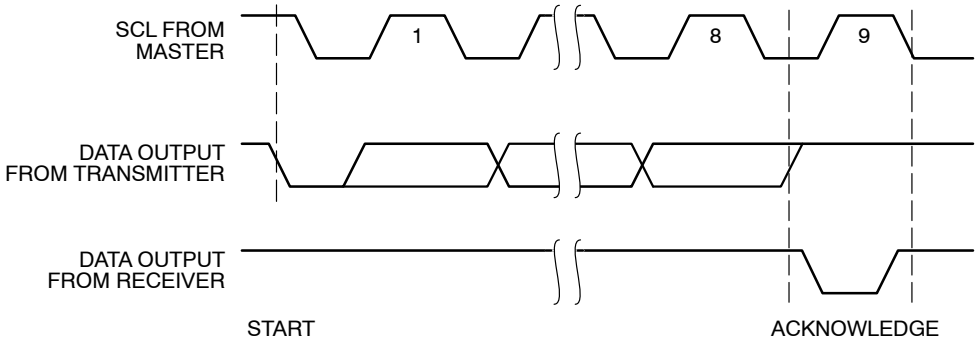



**Figure 8. Acknowledge Timing**

| 1 | 0 | 1 | 0 | X | X | X | R/$\overline{W}$ |
|---|---|---|---|---|---|---|---|

**Figure 9. Slave Address Bits**

### Write Protection

When the VCLK pin is connected to GND and the CAT24C21 is in the bi−directional mode, the entire memory is protected and becomes “read only”.

### Read Operations

The READ operation for the CAT24C21 is initiated in the same manner as the write operation with the one exception that the R/$\overline{W}$ bit is set to a one. Three different READ operations are possible: Immediate Address READ, Selective READ and Sequential READ.

### Immediate Address Read

The CAT24C21’s address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N + 1 (Figure 12). If N = 127, then the counter will ‘wrap around’ to address 0 and continue to clock out data.

### Selective Read

Selective READ operations allow the Master device to select at random any memory location for a READ operation (Figure 13). The Master device first performs a ‘dummy’ write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT24C21 acknowledges the word address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The CAT24C21 then responds with its ACK and sends the 8−bit byte requested. The master device does not send an ACK but will generate a STOP condition.

### Sequential Read

The Sequential READ operation (Figure 14) can be initiated by either the Immediate Address READ or the Selective READ operation. After the CAT24C21 sends the first 8−bit byte, the Master responds with an ACK, which tells the Slave that more data is being requested. The CAT24C21 will continue to output an 8−bit byte for each ACK sent by the Master. The entire memory content can thus be read out sequentially. If the end of memory is reached in the process, then addressing will ‘wrap−around’ to the beginning of memory. Data output will stop when the Master fails to acknowledge and sends a STOP condition.

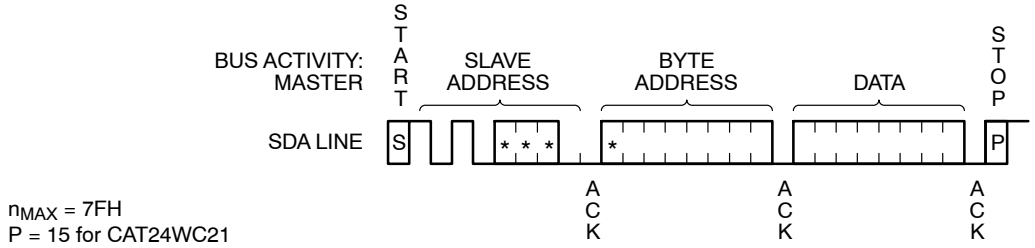



**Figure 10. Byte Write Timing**

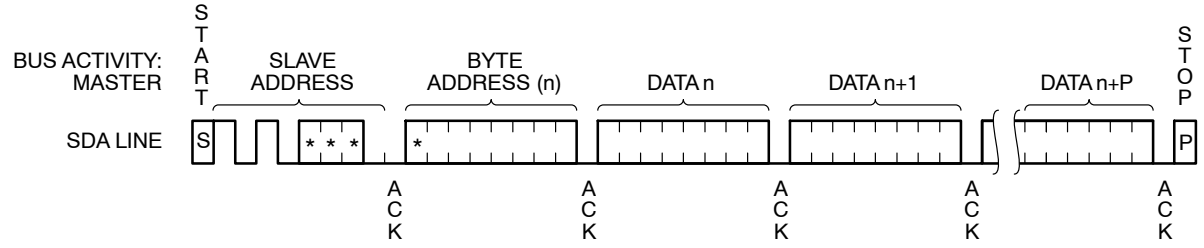



**Figure 11. Page Write Timing**

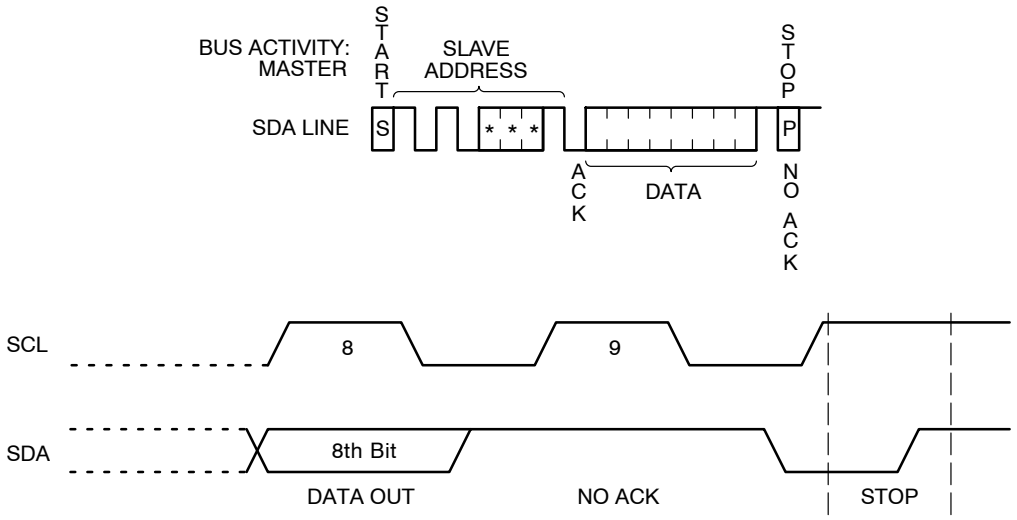



**Figure 12. Immediate Address Read Timing**

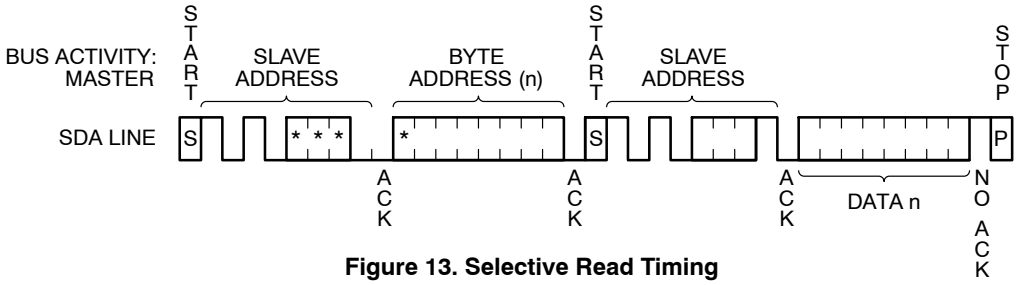



**Figure 13. Selective Read Timing**

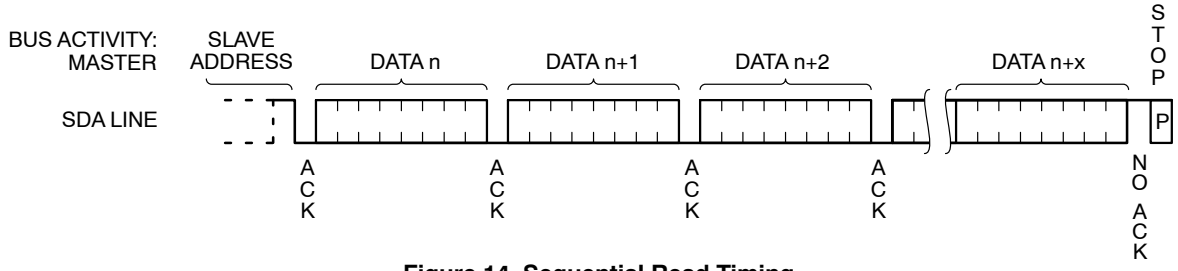
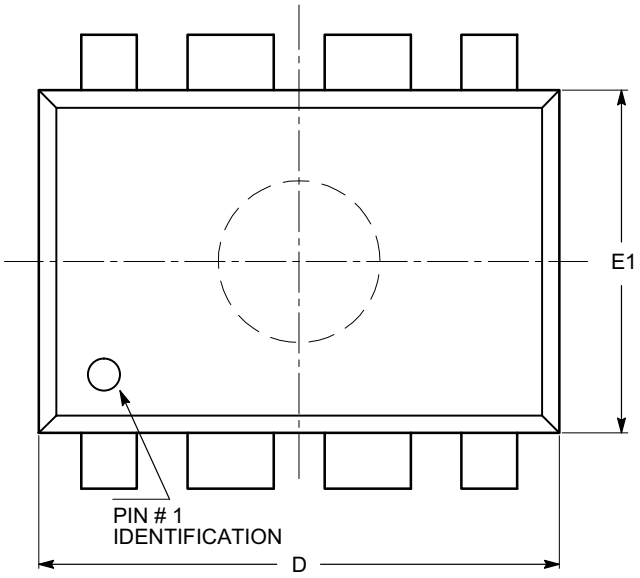



**Figure 14. Sequential Read Timing**

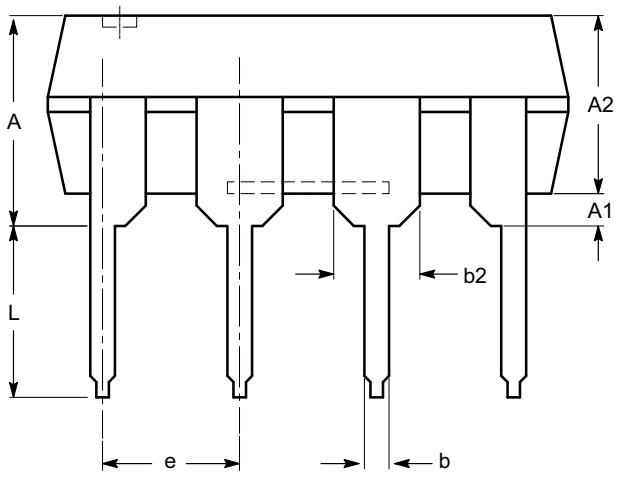
## PACKAGE DIMENSIONS

**PDIP−8, 300 mils**
CASE 646AA−01
ISSUE A

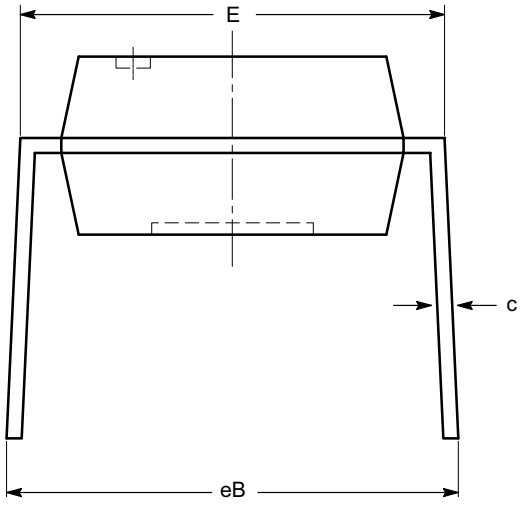



**TOP VIEW**

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | | | 5.33 |
| A1 | 0.38 | | |
| A2 | 2.92 | 3.30 | 4.95 |
| b | 0.36 | 0.46 | 0.56 |
| b2 | 1.14 | 1.52 | 1.78 |
| c | 0.20 | 0.25 | 0.36 |
| D | 9.02 | 9.27 | 10.16 |
| E | 7.62 | 7.87 | 8.25 |
| E1 | 6.10 | 6.35 | 7.11 |
| e | | 2.54 BSC | |
| eB | 7.87 | | 10.92 |
| L | 2.92 | 3.30 | 3.80 |




**SIDE VIEW**

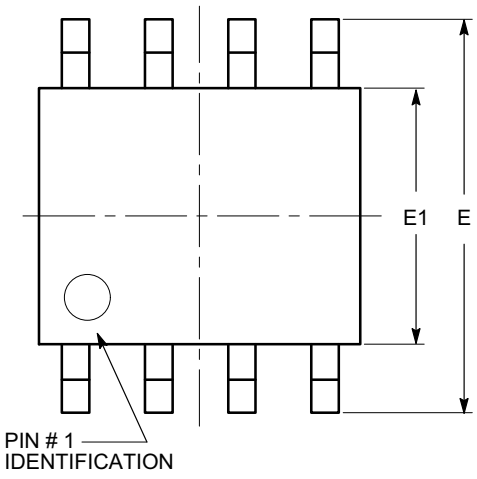



**END VIEW**

**Notes:**
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

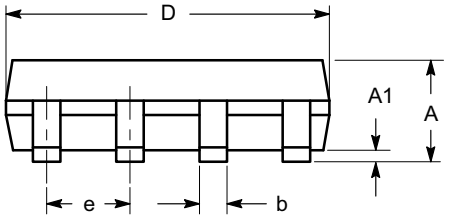
## PACKAGE DIMENSIONS

**SOIC 8, 150 mils**
CASE 751BD−01
ISSUE O

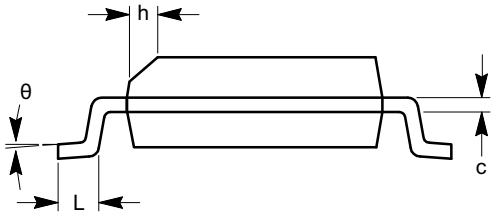



**TOP VIEW**

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 1.35 | | 1.75 |
| A1 | 0.10 | | 0.25 |
| b | 0.33 | | 0.51 |
| c | 0.19 | | 0.25 |
| D | 4.80 | | 5.00 |
| E | 5.80 | | 6.20 |
| E1 | 3.80 | | 4.00 |
| e | | 1.27 BSC | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| θ | 0º | | 8º |




**SIDE VIEW**

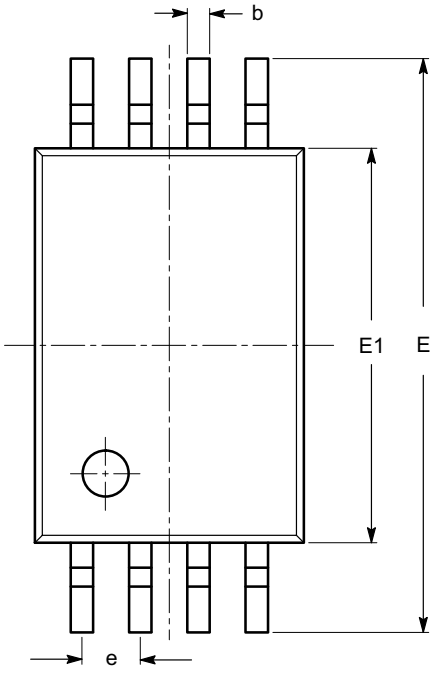



**END VIEW**

**Notes:**
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

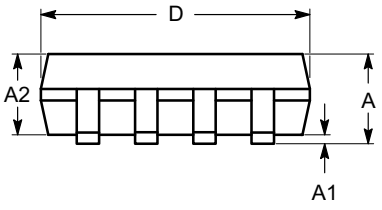
## PACKAGE DIMENSIONS

**TSSOP8, 4.4x3**
CASE 948AL−01
ISSUE O

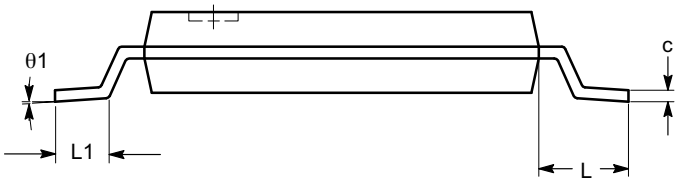



**TOP VIEW**

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | | | 1.20 |
| A1 | 0.05 | | 0.15 |
| A2 | 0.80 | 0.90 | 1.05 |
| b | 0.19 | | 0.30 |
| c | 0.09 | | 0.20 |
| D | 2.90 | 3.00 | 3.10 |
| E | 6.30 | 6.40 | 6.50 |
| E1 | 4.30 | 4.40 | 4.50 |
| e | 0.65 BSC | | |
| L | 1.00 REF | | |
| L1 | 0.50 | 0.60 | 0.75 |
| θ | 0° | | 8° |




**SIDE VIEW**

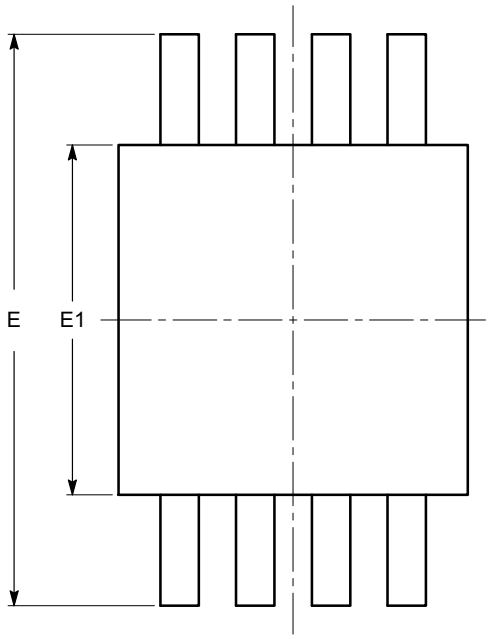



**END VIEW**

**Notes:**
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

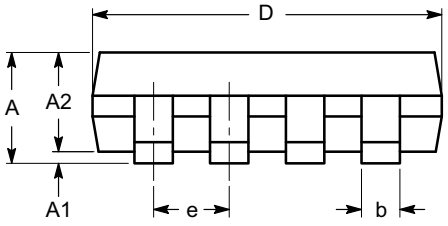
## PACKAGE DIMENSIONS

**MSOP 8, 3x3**
CASE 846AD−01
ISSUE O

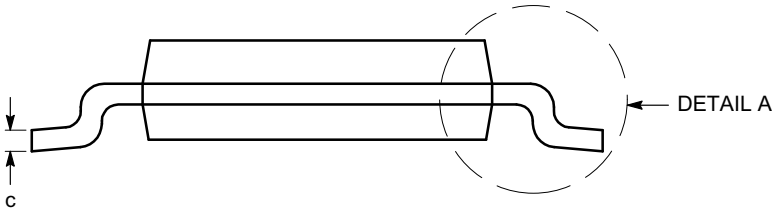



**TOP VIEW**

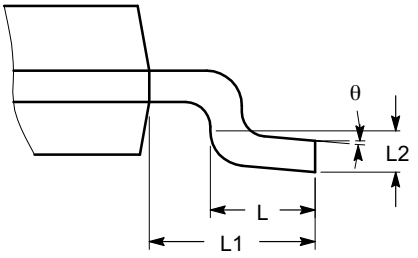
| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | | | 1.10 |
| A1 | 0.05 | 0.10 | 0.15 |
| A2 | 0.75 | 0.85 | 0.95 |
| b | 0.22 | | 0.38 |
| c | 0.13 | | 0.23 |
| D | 2.90 | 3.00 | 3.10 |
| E | 4.80 | 4.90 | 5.00 |
| E1 | 2.90 | 3.00 | 3.10 |
| e | | 0.65 BSC | |
| L | 0.40 | 0.60 | 0.80 |
| L1 | | 0.95 REF | |
| L2 | | 0.25 BSC | |
| θ | 0° | | 6° |




**SIDE VIEW**




**END VIEW**

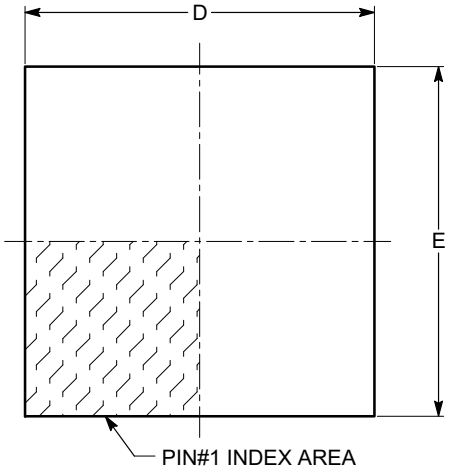



**DETAIL A**

**Notes:**
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-187.

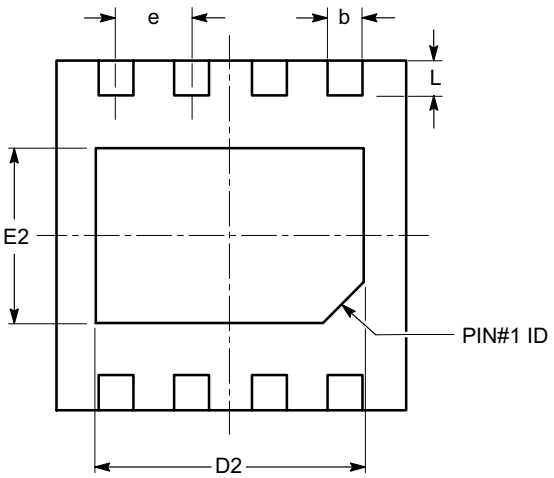
## PACKAGE DIMENSIONS

**TDFN8, 3x3**
CASE 511AL−01
ISSUE A



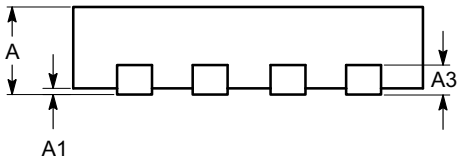

**TOP VIEW**


**SIDE VIEW**




**BOTTOM VIEW**

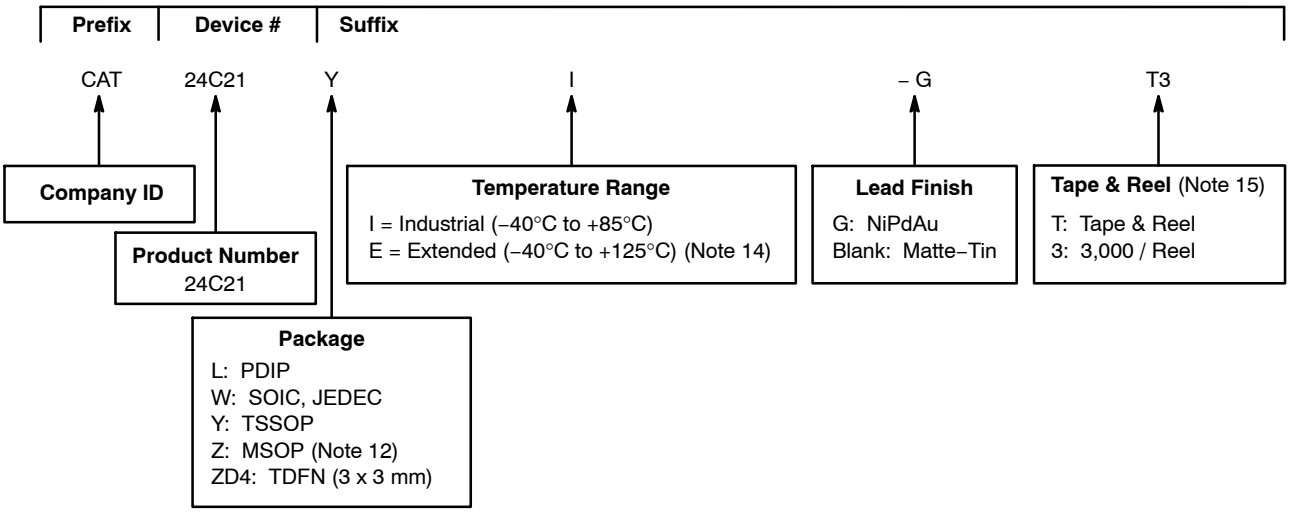
| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20 REF | |
| b | 0.23 | 0.30 | 0.37 |
| D | 2.90 | 3.00 | 3.10 |
| D2 | 2.20 | −−− | 2.50 |
| E | 2.90 | 3.00 | 3.10 |
| E2 | 1.40 | −−− | 1.80 |
| e | | 0.65 TYP | |
| L | 0.20 | 0.30 | 0.40 |




**FRONT VIEW**

**Notes:**
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MO-229.

## Example of Ordering Information




10. All packages are RoHS-compliant (Lead-free, Halogen-free).
11. The device used in the above example is a CAT24C21YI–GT3 (TSSOP, Industrial Temperature, NiPdAu, Tape & Reel, 3,000/Reel).
12. For availability, please contact your nearest ON Semiconductor Sales office.
13. For additional package options, please contact your nearest ON Semiconductor Sales office.
14. Extended Temperature available upon request.
15. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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