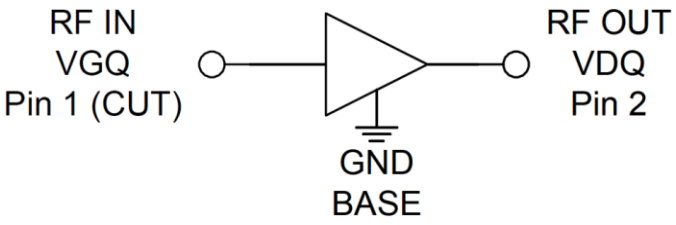
RFHA1023

225W GaN Wideband Pulsed Power Amplifier

Package: Flanged Ceramic, 2-Pin

The RFHA1023 is a 36V 225W high power discrete amplifier designed for L-band pulsed radar, air traffic control and surveillance and general purpose broadband amplifier applications. Using an advanced high power density gallium nitride (GaN) semiconductor process, these high performance amplifiers achieve high output power, high efficiency and flat gain over a broad frequency range in a single package. The RFHA1023 is a matched power transistor packaged in a hermetic, flanged ceramic package. The package provides excellent thermal stability through the use of advanced heat sink and power dissipation technologies. Ease of integration is accomplished through the incorporation of single, optimized matching networks that provide wideband gain and power performance in a single amplifier.



Functional Block Diagram

Features

- Wideband Operation 1.2GHz to 1.4GHz
- Advanced GaN HEMT Technology
- Advanced Heat-Sink Technology
- Supports Multiple Pulse Conditions
  - 10% to 20% Duty Cycle
  - 100µs to 1ms Pulse Width
- Integrated Matching Components for High Terminal Impedances
- 36V Operation Typical Performance
  - Pulsed Output Power 225W
  - Pulse Width 1ms, Duty Cycle 10%
  - Small Signal Gain 15dB
  - High Efficiency 55%
  - -40°C to 85°C Operating Temperature

Applications

- Radar
- Air Traffic Control and Surveillance
- General Purpose Broadband Amplifiers

Ordering Information

RFHA1023S2	Sample bag with 2 pieces
RFHA1023SB	Bag with 5 pieces
RFHA1023SQ	Bag with 25 pieces
RFHA1023SR	7” Short reel with 50 pieces
RFHA1023TR13	13” Reel with 250 pieces
RFHA1023PCBA-410	Fully assembled evaluation board 1.2GHz to 1.4GHz; 36V operation

RF Micro Devices Inc. 7628 Thorndike Road, Greensboro, NC 27409-9421
For sales or technical support, contact RFMD at +1.336.678.5570 or customerservice@rfmd.com.

DS131021

Absolute Maximum Ratings

Parameter	Rating	Unit
Drain Voltage (V_D)	150	V
Gate Voltage (V_G)	-8 to +2	V
Gate Current (I_G)	155	mA
Operational Voltage	40	V
Ruggedness (VSWR)	10:1	
Storage Temperature Range	-55 to +125	°C
Operating Temperature Range (T_C)	-40 to +85	°C
Operating Junction Temperature (T_J)	250	°C
Human Body Model	Class 1A	
MTTF (T_J < 200°C)	3.0E + 06	Hours
MTTF (T_J < 250°C)	1.4E + 05	
Thermal Resistance, R_{TH} (junction to case) T_C = 85°C, DC bias only T_C = 85°C, 100µs pulse, 10% duty cycle T_C = 85°C, 1ms pulse, 10% duty cycle	 0.90 0.18 0.34	°C/W

Caution! ESD sensitive device.

RFMD Green: RoHS compliant per EU Directive 2011/65/EU, halogen free per IEC 61249-2-21, <1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony solder.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

*MTTF - Median time to failure as determined by the process technology wear-out failure mode. Refer to product qualification report for FIT (random) failure rate.

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table above.

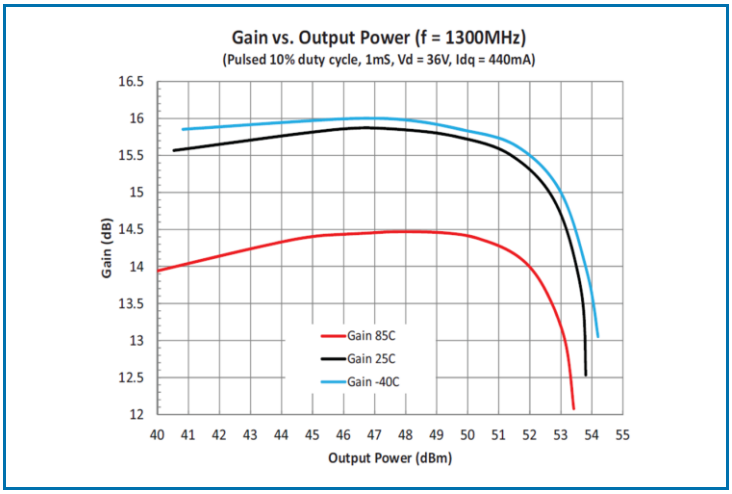
Bias conditions should also satisfy the following expression: $P_{DISS} < (T_J - T_C) / R_{TH\ J\text{-}C}$ and $T_C = T_{CASE}$

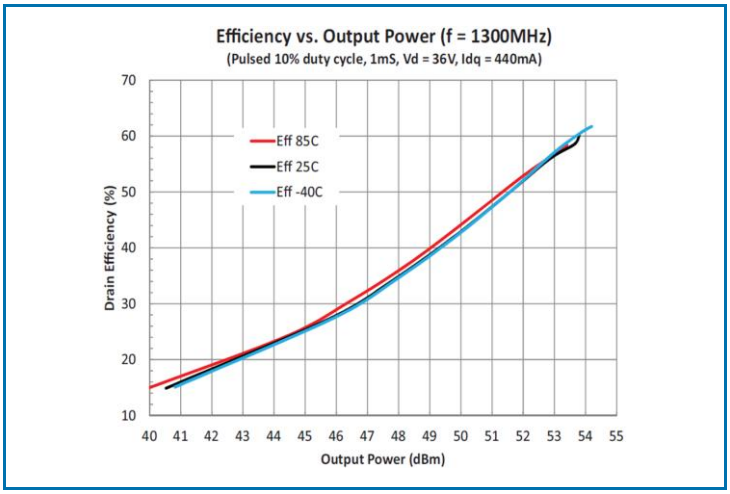
Nominal Operating Parameters

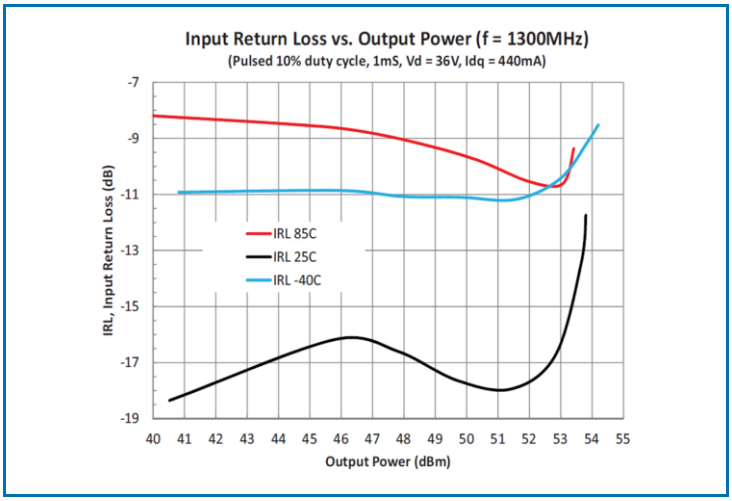
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Recommended Operating Conditions					
Drain Voltage (V_{DSQ})			36	V	
Gate Voltage (V_{GSQ})	-8	-3	-2	V	
Drain Bias Current		440		mA	
Frequency of Operation	1200		1400	MHz	
DC Functional Test					
$I_{G\ (OFF)}$ - Gate Leakage			2	mA	V_G = -8V, V_D = 0V
$I_{D\ (OFF)}$ - Drain Leakage			2	mA	V_G = -8V, V_D = 50V
$V_{GS\ (TH)}$ - Threshold Voltage		-3.4		V	V_D = 36V, I_D = 20mA
$V_{DS\ (on)}$ - Drain Voltage at High Current		0.22		V	V_G = 0V, V_D = 1.5A

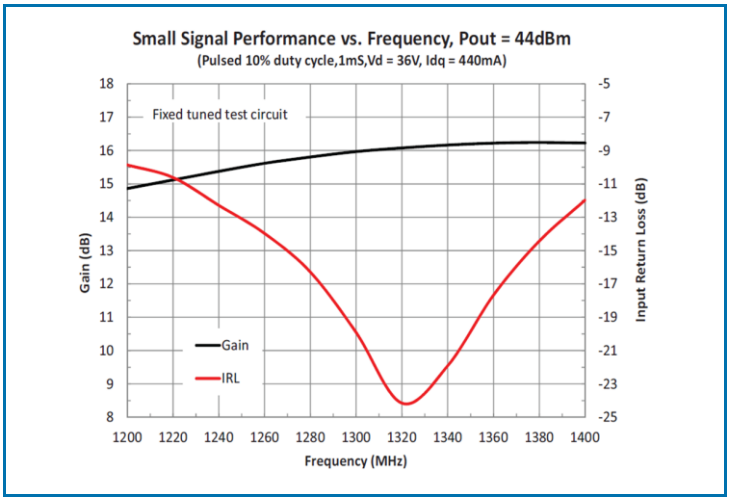
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
RF Functional Test					**Test Conditions: PW = 1ms, DC = 10%, V_{DSQ} = 36V, I_{DQ} = 440mA, T = 25ºC, Performance in a standard tuned test fixture**
Small Signal Gain		14		dB	f = 1200MHz, P_{IN} = 30dBm
Power Gain	11.8			dB	f = 1200MHz, P_{IN} = 41.2dBm
Input Return Loss			-6	dB	f = 1200MHz, P_{IN} = 30dBm
Output Power	53	53.25		dBm	f = 1200MHz, P_{IN} = 41.2dBm
Drain Efficiency	48	50		%	f = 1200MHz, P_{IN} = 41.2dBm
Small Signal Gain		15		dB	f = 1300MHz, P_{IN} = 30dBm
Power Gain	12.3			dB	f = 1300MHz, P_{IN} = 41.2dBm
Input Return Loss			-6	dB	f = 1300MHz, P_{IN} = 30dBm
Output Power	53	53.5		dBm	f = 1300MHz, P_{IN} = 41.2dBm
Drain Efficiency	50	58		%	f = 1300MHz, P_{IN} = 41.2dBm
Small Signal Gain		14		dB	f = 1400MHz, P_{IN} = 30dBm
Power Gain	11.8			dB	f = 1400MHz, P_{IN} = 41.2dBm
Input Return Loss			-6	dB	f = 1400MHz, P_{IN} = 30dBm
Output Power	53	53.25		dBm	f = 1400MHz, P_{IN} = 41.2dBm
Drain Efficiency	55	63		%	f = 1400MHz, P_{IN} = 41.2dBm
RF Typical Performance					**Test Conditions: PW = 1ms, DC = 10%, V_{DSQ} = 36V, I_{DQ} = 440mA, T = 25ºC, Performance in a standard tuned test fixture**
Frequency Range	1200		1400	MHz	
Small Signal Gain		15		dB	f = 1300MHz, P_{IN} = 30dBm
Power Gain		12.3		dB	f = 1300MHz, P_{OUT} = 53.5dBm
Gain Variation with Temperature			-0.015	dB/C°	Peak output power
Output Power (P_{SAT})		53.52		dBm	
		225		W	
Drain Efficiency		58		%	

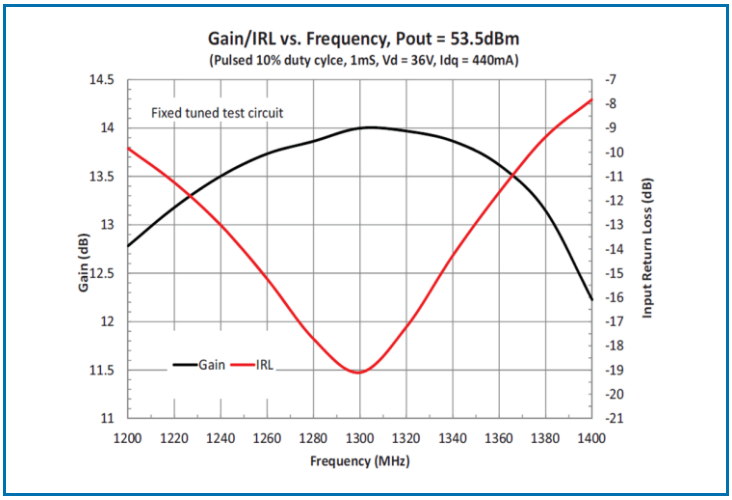
Typical Performance in Standard Fixed Tuned Test Fixture (T = 25°C, unless noted)

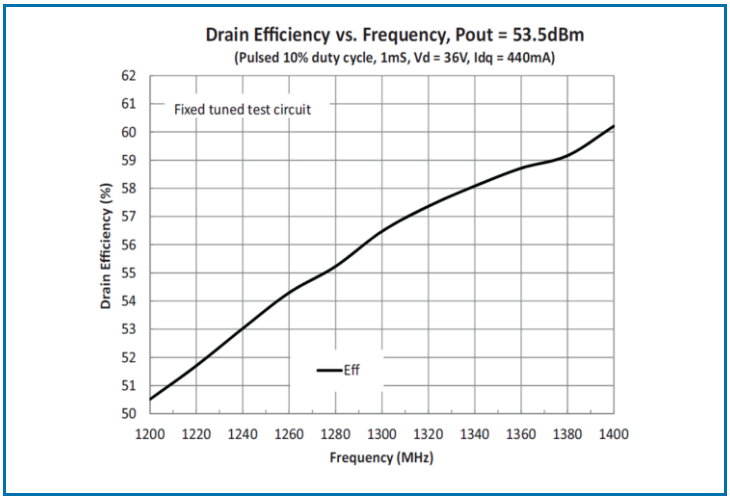




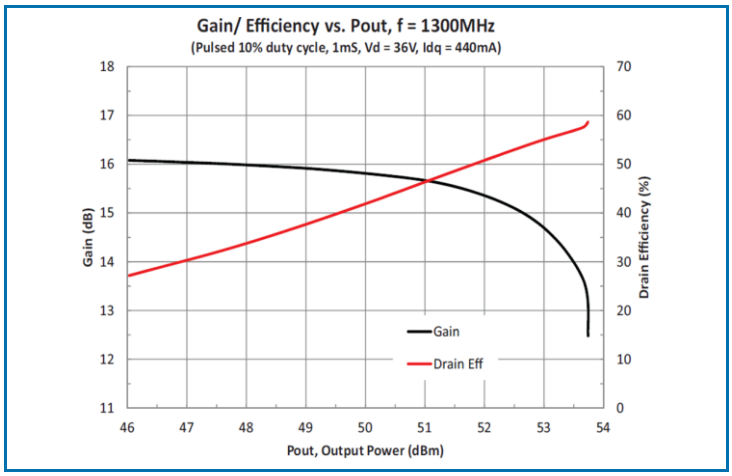


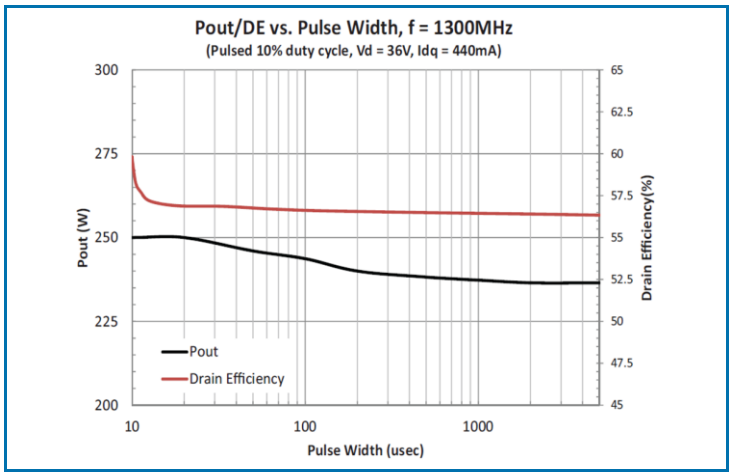


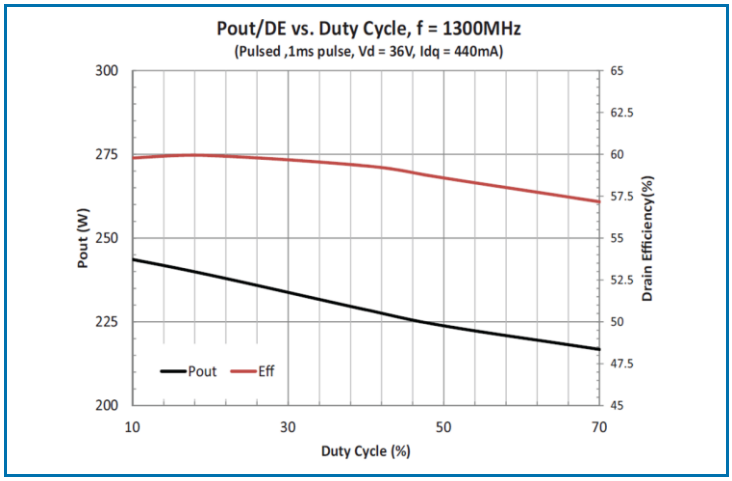


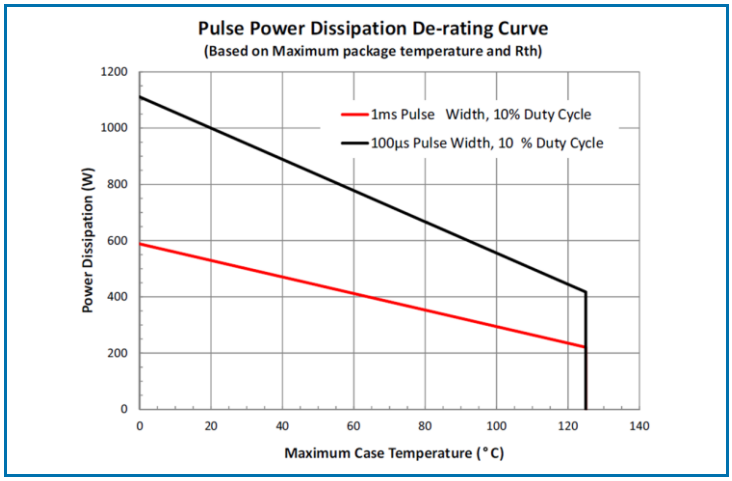


Typical Performance (continued)

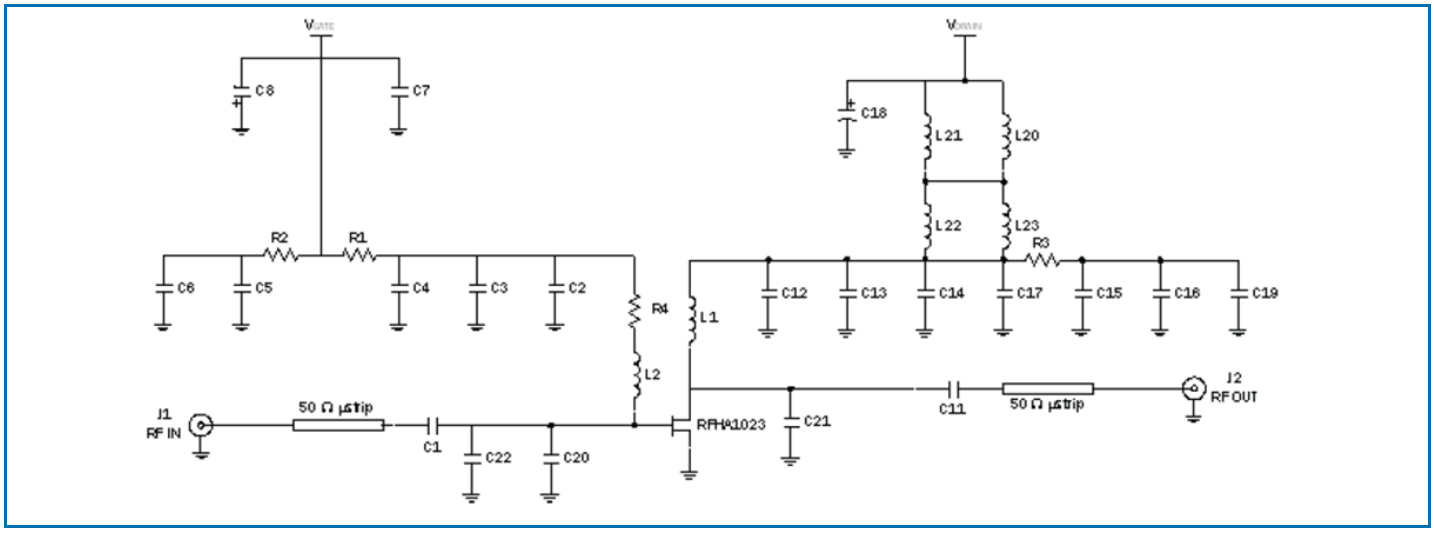








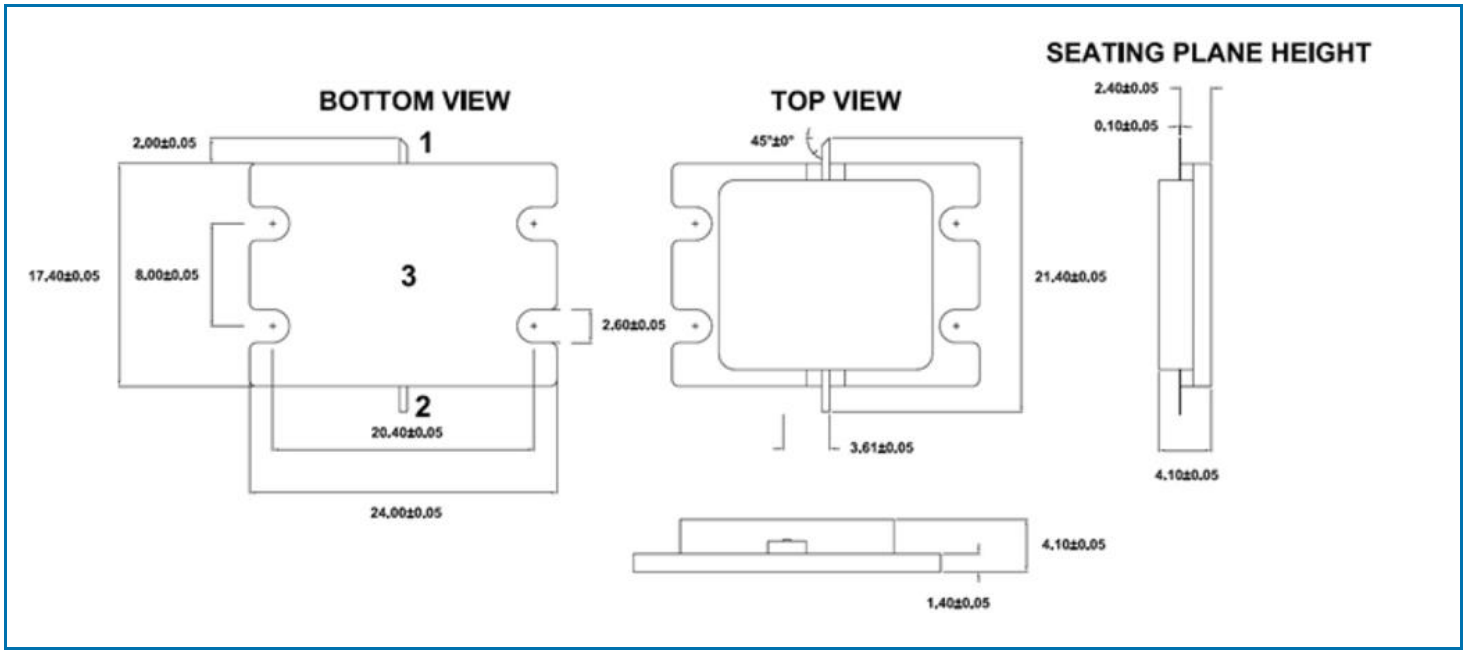
Evaluation Board Schematic



Evaluation Board Bill of Materials (BOM)

Item	Value	Manufacturer	Manufacturer's P/N
R1,R4	10Ω	Panasonic	ERJ-8GEYJ100V
R2	0Ω	Panasonic	ERJ-8GEY0R00
R3	51Ω	Panasonic	ERJ-8GEYJ510
C1, C2, C11, C12	150pF	Dielectric Labs	C11CF151J-9ZN-X0V
C17	56pF	ATC	ATC800A560JT
C5	0.1μF	Panasonic	ECJ-2VB1H104K
C6, C15	10000pF	Panasonic	ECJ-2VB1H103K
C16	0.1μF	Panasonic	ECJ-2VB1H104K
C8, C18	10μF	Panasonic	ECA-2AM100
C20	3.3pF	ATC	ATC100B3R3BT
C21	1.5pF	ATC	ATC100B1R5BT
C22	0.3pF	ATC	ATC100B0R3BT
L1, L2	68nH	Coilcraft	1812SMS-68NJLB
L20, L21	115Ω 10A	Steward	28F0181-1SR-10
L22, L23	75Ω, 10A	Steward	35F0121-1SR-10
C3, C4, C7, C12, C14, C19	NOT POPULATED	-	-

Package Drawing (all dimensions in millimeters)



Pin Names and Descriptions

Pin	Name	Description
1	VG	Gate - V_G RF Input
2	VD	Drain - V_D RF Output
3	GND BASE	Source - Ground Base

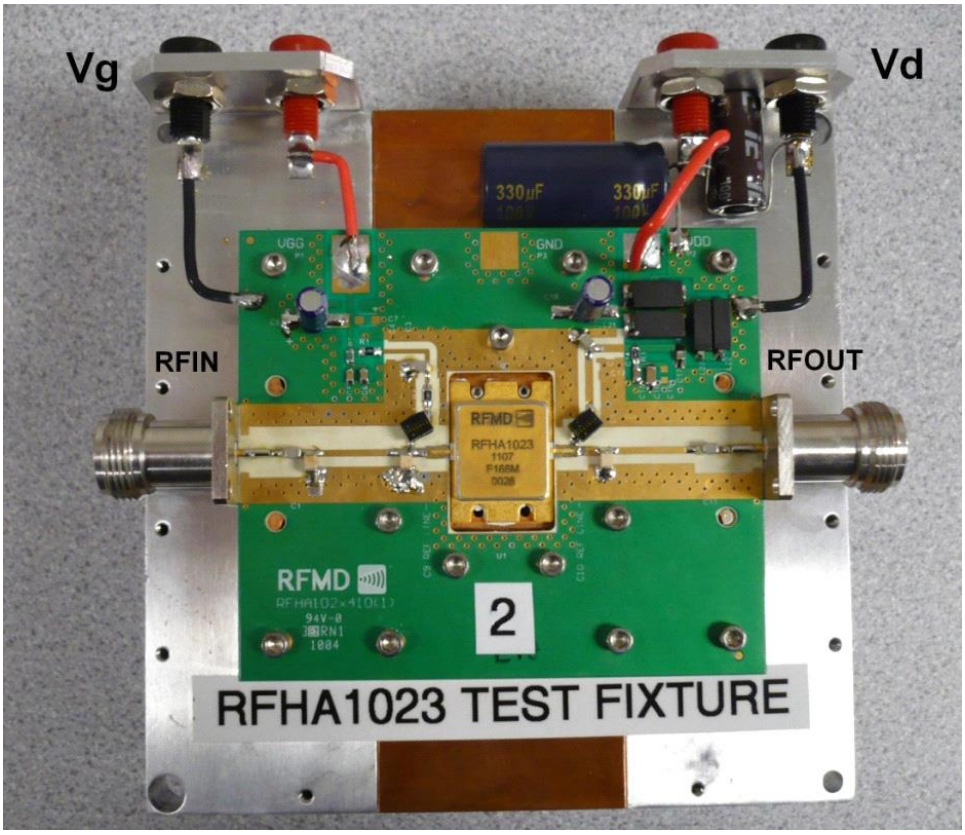
Bias Instruction for RFHA1023 Evaluation Board

- ESD Sensitive Material. Please use proper ESD precautions when handling devices of evaluation board.
- Evaluation board requires additional external fan cooling.
- Connect all supplies before powering up the evaluation board.

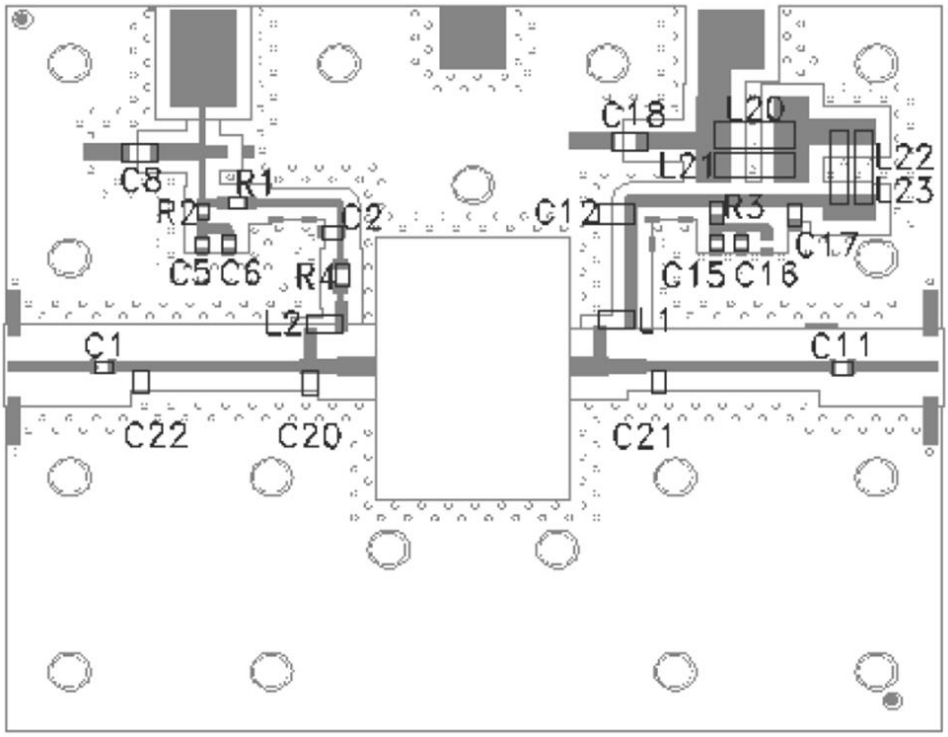
1. Connect RF cables at RFIN and RFOUT.
2. Connect ground to the ground supply terminal, and ensure that both the VG and VD grounds are also connected to this ground terminal.
3. Apply -8V to VG.
4. Apply 36V to VD.
5. Increase V_G until drain current reaches desired 440mA or desired bias point.
6. Turn on RF input.

- IMPORTANT NOTE: Depletion mode device, when biasing the device V_G must be applied BEFORE V_D. When removing bias, V_D must be removed BEFORE V_G is removed. Failure to follow sequencing will cause the device to fail.

- NOTE: For optimal RF performance, consistent and optimal heat removal from the base of the package is required. A thin layer of thermal grease should be applied to the interface between the base of the package and the equipment chassis. It is recommended a small amount of thermal grease is applied to the underside of the device package. Even application and removal of excess thermal grease can be achieved by spreading the thermal grease using a razor blade. The package should then be bolted to the chassis and input and output leads soldered to the circuit board.



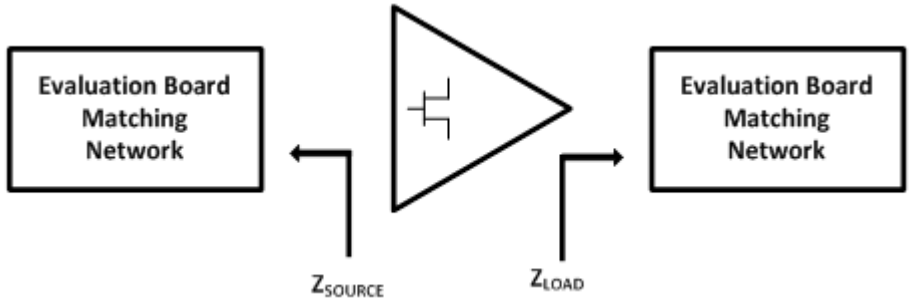
Evaluation Board Layout



Device Impedances

Frequency (MHz)	Z Source (Ω)	Z Load (Ω)
1200	12.98 - j8.23	25.48 - j12.4
1300	11.75 - j7.16	24.6 - j12.9
1400	10.41 - j5.98	23.4 - j13.4

NOTE: Device impedances reported are the measured evaluation board impedances chosen for a tradeoff of efficiency, peak power, and linearity performance across the entire frequency bandwidth.



Device Handling/Environmental Conditions

GaN HEMT devices are ESD sensitive materials. Please use proper ESD precautions when handling devices or evaluation boards.

GaN HEMT Capacitances

The physical structure of the GaN HEMT results in three terminal capacitors similar to other FET technologies. These capacitances exist across all three terminals of the device. The physical manufactured characteristics of the device determine the value of the C_{DS} (drain to source), C_{GS} (gate to source) and C_{GD} (gate to drain). These capacitances change value as the terminal voltages are varied. RFMD presents the three terminal capacitances measured with the gate pinched off (V_{GS} = -8V) and zero volts applied to the drain. During the measurement process, the parasitic capacitances of the package that holds the amplifier is removed through a calibration step. Any internal matching is included in the terminal capacitance measurements. The capacitance values presented in the typical characteristics table of the device represent the measured input (C_{ISS}), output (C_{OSS}), and reverse (C_{RSS}) capacitance at the stated bias voltages. The relationship to three terminal capacitances is as follows:

$$C_{ISS} = C_{GD} + C_{GS}$$

$$C_{OSS} = C_{GD} + C_{DS}$$

$$C_{RSS} = C_{GD}$$

DC Bias

The GaN HEMT device is a depletion mode high electron mobility transistor (HEMT). At zero volts V_{GS} the drain of the device is saturated and uncontrolled drain current will destroy the transistor. The gate voltage must be taken to a potential lower than the source voltage to pinch off the device prior to applying the drain voltage, taking care not to exceed the gate voltage maximum limits. RFMD recommends applying V_{GS} = -5V before applying any V_{DS}.

RF Power transistor performance capabilities are determined by the applied quiescent drain current. This drain current can be adjusted to trade off power, linearity, and efficiency characteristics of the device. The recommended quiescent drain current (I_{DQ}) shown in the RF typical performance table is chosen to best represent the operational characteristics for this device, considering manufacturing variations and expected performance. The user may choose alternate conditions for biasing this device based on performance trade-offs.

Mounting and Thermal Considerations

The thermal resistance provided as R_{TH} (junction to case) represents only the packaged device thermal characteristics. This is measured using IR microscopy capturing the device under test temperature at the hottest spot of the die. At the same time, the package temperature is measured using a thermocouple touching the backside of the die embedded in the device heat-sink but sized to prevent the measurement system from impacting the results. Knowing the dissipated power at the time of the measurement, the thermal resistance is calculated.

In order to achieve the advertised MTTF, proper heat removal must be considered to maintain the junction at or below the maximum of 200°C. Proper thermal design includes consideration of ambient temperature and the thermal resistance from ambient to the back of the package including heat-sinking systems and air flow mechanisms. Incorporating the dissipated DC power, it is possible to calculate the junction temperature of the device.