PRELIMINARY

CY7C1049
CY7C1049L

512K x 8 Static RAM

Features

- **High speed**
  - **—t_{AA} = 17 ns**
- **Low active power**
  - **—1073 mW (max.)**
- **Low CMOS standby power (L version)**
  - **—2.75 mW (max.)**
- **2.0V Data Retention (400 μW at 2.0V retention)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**

Functional Description

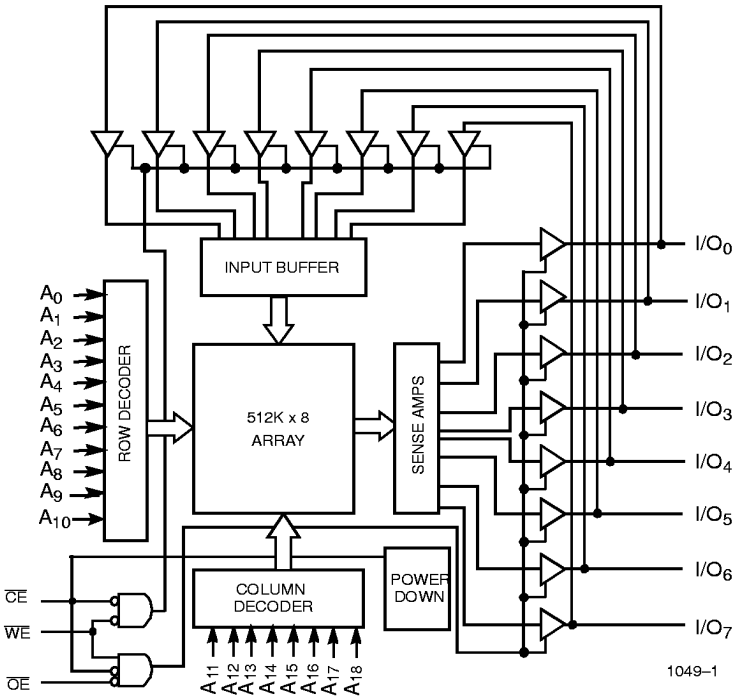
The CY7C1049 is a high-performance CMOS static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), an active LOW output enable ($\overline{OE}$), and three-state drivers. Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1049 is available in a standard 400-mil-wide 36-pin SOJ package with center power and ground (revolutionary) pinout.

Logic Block Diagram



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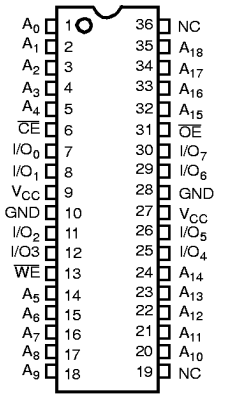
Pin Configuration

SOJ
Top View



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Selection Guide (Commercial Temp)

		7C1049-15	7C1049-17	7C1049-20	7C1049-25	7C1049-35
Maximum Access Time (ns)		15	17	20	25	35
Maximum Operating Current (mA)		200	195	185	180	175
Maximum CMOS Standby Current (mA)		2	2	2	2	2
	L	0.5	0.5	0.5	0.5	0.5

Shaded areas contain advance information

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] .... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1].....–0.5V to V_{CC} +0.5V

DC Input Voltage[1].....–0.5V to V_{CC} +0.5V

Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%
Military[2]	–55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions			7C1049-15		7C1049-17		7C1049-20		Unit
					Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA			2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.2	V_{CC} + 0.5	2.2	V_{CC} + 0.5	2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage[1]				–0.5	0.8	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			–1	+1	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled			–1	+1	–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. f = f_{MAX} = $1/t_{RC}$				200		195		185	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}				40		40		40	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f=0	Com'l/Ind'l			8		8		8	mA
			Military			10		10		10	
			Com'l	L		500		500		500	µA

Shaded areas contain advance information

Notes:

1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature

Electrical Characteristics Over the Operating Range (continued)

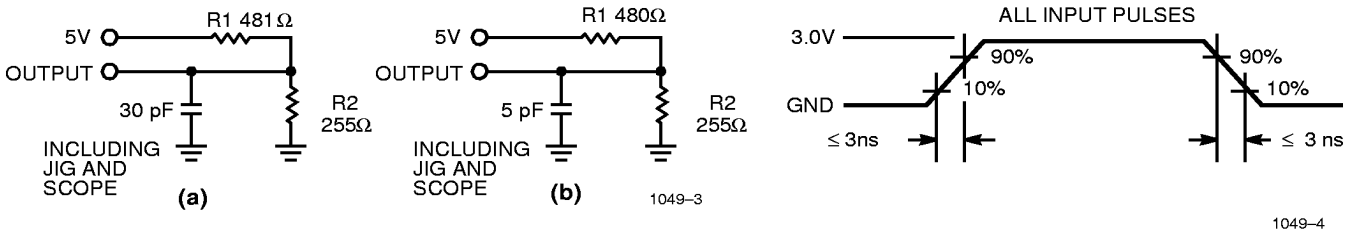
Parameter	Description	Test Conditions		7C1049-25 Min.	7C1049-25 Max.	7C1049-35 Min.	7C1049-35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.5	2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage[1]			–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = $1/t_{RC}$			180		175	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			40		40	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f=0	Com'l/Ind'l		8		8	mA
			Military		10		10	mA
			L		500		500	µA

Capacitance[3]

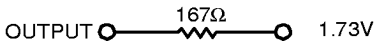
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	I/O Capacitance		10	pF

Note:
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics[5] Over the Operating Range

Parameter	Description	7C1049-15		7C1049-17		7C1049-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	15		17		20		ns
t_{AA}	Address to Data Valid		15		17		20	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		17		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		7		8		8	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		7		7		8	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[5, 6]		7		7		8	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		17		20	ns
WRITE CYCLE[7,8]								
t_{WC}	Write Cycle Time	15		17		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		12		13		ns
t_{AW}	Address Set-Up to Write End	12		12		13		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		12		13		ns
t_{SD}	Data Set-Up to Write End	8		8		9		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]		7		8		8	ns

Shaded areas contain advance information

Notes:

4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
8. The minimum write cycle time for Write Cycle no. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and T_{SD}.

Switching Characteristics[5] Over the Operating Range (continued)

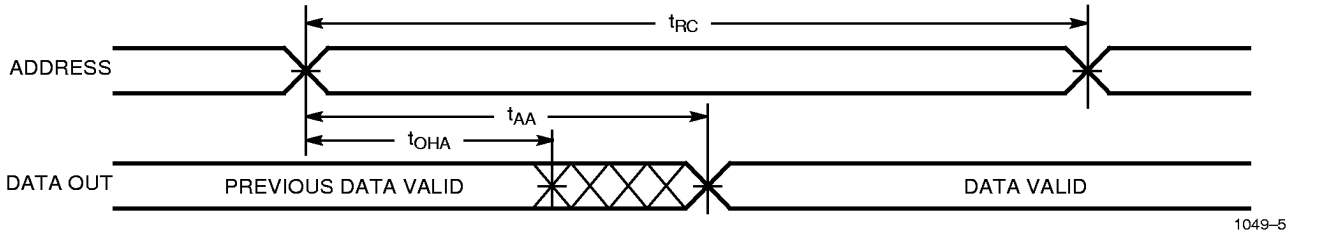
Parameter	Description	7C1049-25		7C1049-35		Unit
		Min.	Max.	Min.	Min.	
READ CYCLE						
t_{RC}	Read Cycle Time	25		35		ns
t_{AA}	Address to Data Valid		25		35	ns
t_{OHA}	Data Hold from Address Change	5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5, 6]		10		15	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[5, 6]		10		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		25		35	ns
WRITE CYCLE[7]						
t_{WC}	Write Cycle Time	25		35		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	15		20		ns
t_{AW}	Address Set-Up to Write End	15		20		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		ns
t_{SD}	Data Set-Up to Write End	10		15		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]		10		15	ns

Data Retention Characteristics Over the Operating Range

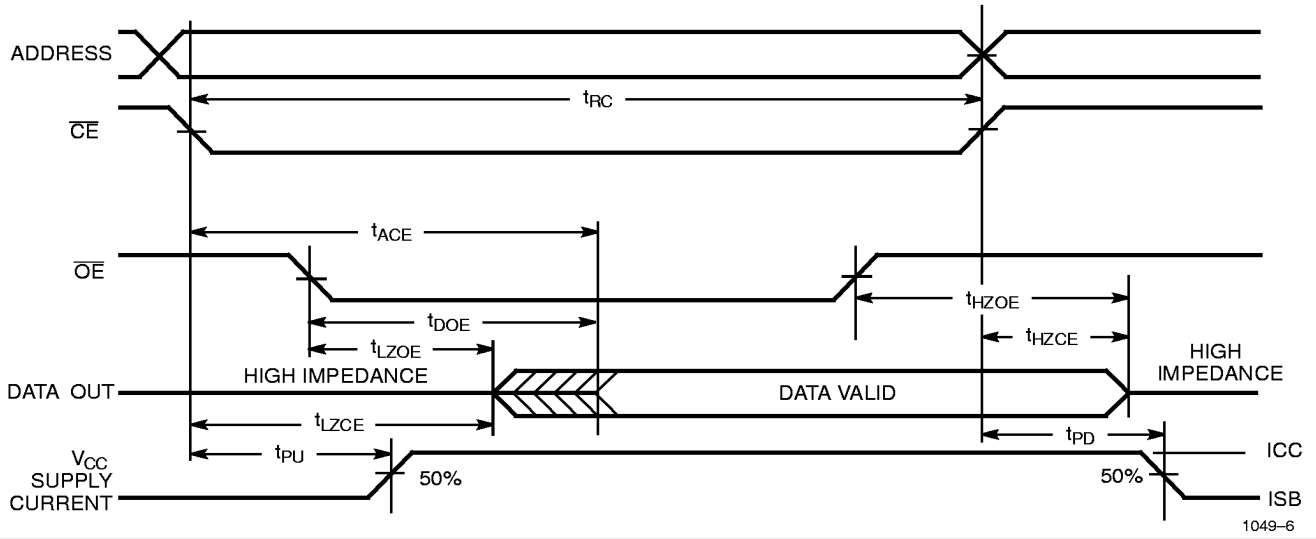
Parameter	Description	Conditions	Min.	Max	Unit
V_{DR}	V_{CC} for Data Retention	No input may exceed V_{CC} + 0.5V $V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	2.0		V
I_{CCDR}	Data Retention Current		(Com'l)	200	µA
			(Ind'l)	500	µA
			(Mil)	2	mA
t_{CDR}	Chip Deselect to Data Retention Time		0		ns
t_R	Operation Recovery Time		t_{RC}		ns

Switching Waveforms

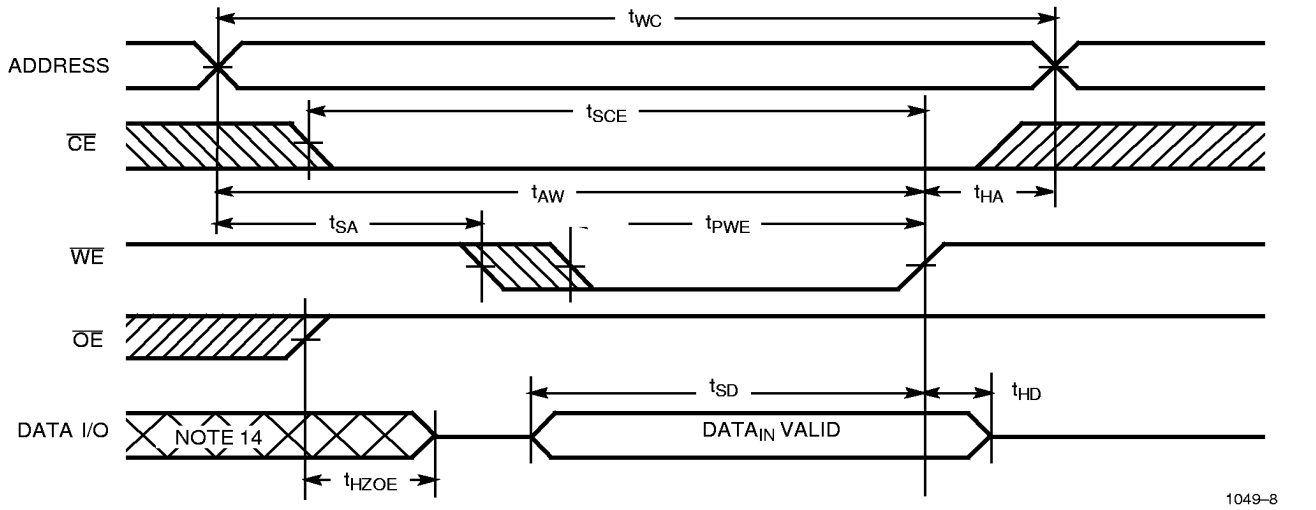
Read Cycle No. 1[9, 10]



Read Cycle No. 2 ($\overline{OE}$ Controlled)[10, 11]



Write Cycle No. 1($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[12, 13]

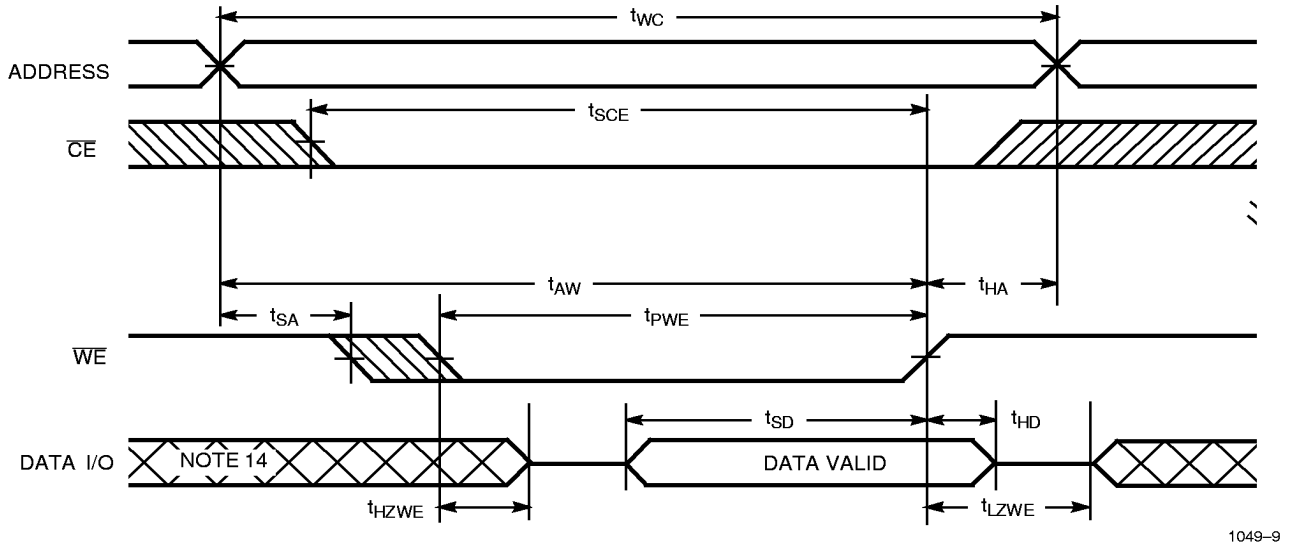


Notes:

9. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
10. $\overline{WE}$ is HIGH for read cycle.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
12. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
14. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[13]



Truth Table

$\overline{CE}$	OE	WE	$I/O_0 - I/O_7$	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C1049-15VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
17	CY7C1049-17VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049L-17VC	V36	36-Lead (400-Mil) Molded SOJ	
20	CY7C1049-20VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049L-20VC	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049-20VI	V36	36-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1049-20VM	V36	36-Lead (400-Mil) Molded SOJ	Military
25	CY7C1049-25VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049L-25VC	V36	36-Lead (400-Mil) Molded SOJ	
35	CY7C1049-35VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049L-35VC	V36	36-Lead (400-Mil) Molded SOJ	

Shaded areas contain advance information.

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Package Diagram

36-Lead (400-Mil) Molded SOJ