



BUK9675-100A

N-channel TrenchMOS logic level FET

18 August 2015

Product data sheet

1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

2. Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance

3. Applications

- Automotive and general purpose power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	100	V
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; Fig. 2		-	-	23	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	98	W
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 10 A; T _j = 25 °C; Fig. 12		-	55	72	mΩ
		V _{GS} = 5 V; I _D = 10 A; T _j = 25 °C; Fig. 12		-	60	75	mΩ
Avalanche ruggedness							
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 23 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped; Fig. 4	[1][2]	-	-	100	mJ

[1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[2] Refer to application note AN10273 for further information.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 D2PAK (SOT404)	 mbb076
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9675-100A	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9675-100A	BUK9675-100A

8. Limiting values

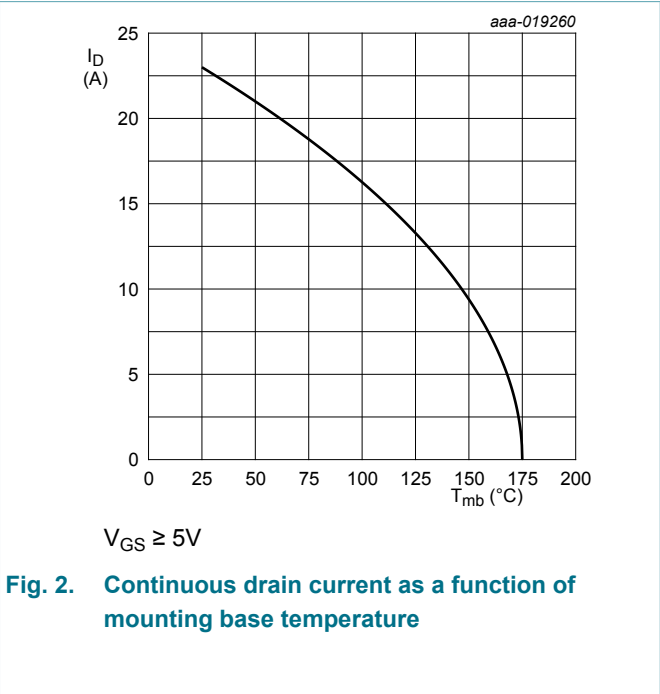
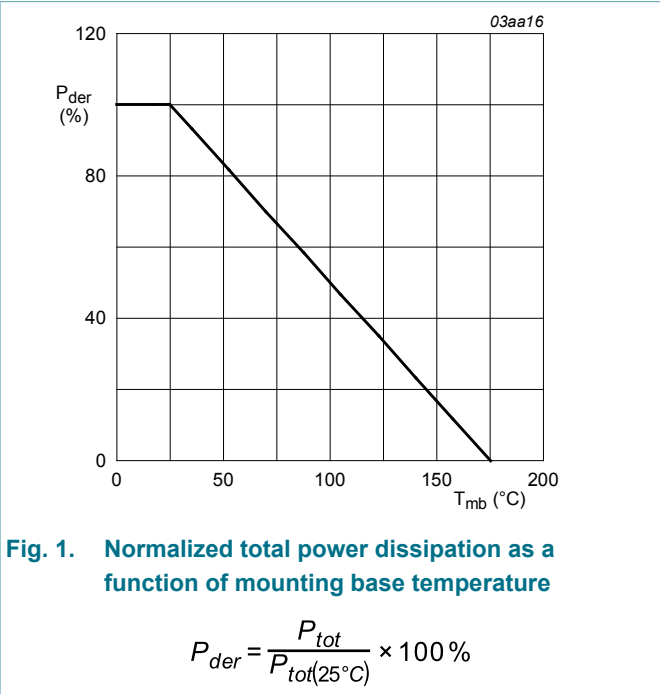
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-15	15	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	98	W
I_D	drain current	$T_{mb} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 2	-	16	A
		$T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 2	-	23	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 3	-	92	A
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C

Symbol	Parameter	Conditions		Min	Max	Unit
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	23	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 µs; T _{mb} = 25 °C		-	92	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 23 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped; Fig. 4	[1] [2]	-	100	mJ

[1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[2] Refer to application note AN10273 for further information.



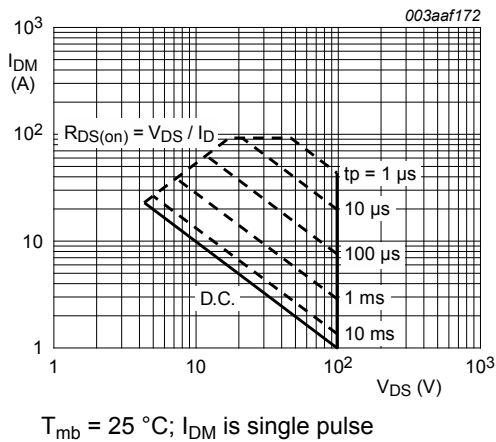


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

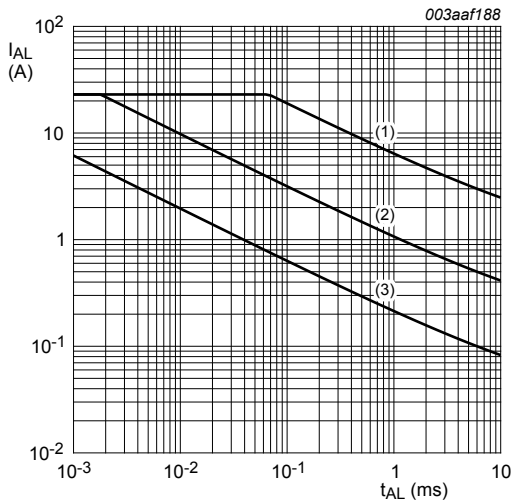


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	1.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; FR4 board	-	50	-	K/W

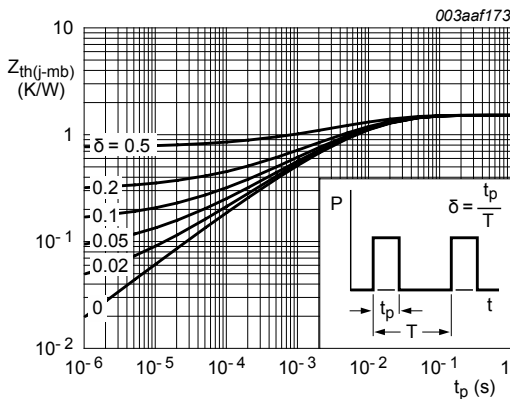


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V; T _j = 25 °C		100	-	-	V
		I _D = 0.25 mA; V _{GS} = 0 V; T _j = -55 °C		89	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; Fig. 10		0.5	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; Fig. 10 ; Fig. 11		1	1.5	2	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; Fig. 10		-	-	2.3	V
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 175 °C		-	-	500	µA
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C		-	0.05	10	µA
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 10 A; T _j = 25 °C; Fig. 12		-	55	72	mΩ
		V _{GS} = 5 V; I _D = 10 A; T _j = 175 °C; Fig. 13		-	-	188	mΩ
		V _{GS} = 4.5 V; I _D = 10 A; T _j = 25 °C; Fig. 12		-	61	84	mΩ
		V _{GS} = 5 V; I _D = 10 A; T _j = 25 °C; Fig. 12		-	60	75	mΩ
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 10 A; V _{DS} = 80 V; V _{GS} = 5 V; Fig. 14 ; Fig. 15		-	24.3	-	nC
Q _{GS}	gate-source charge			-	3	-	nC
Q _{GD}	gate-drain charge			-	12.2	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; Fig. 16		-	1278	1704	pF
C _{oss}	output capacitance			-	129	155	pF
C _{rss}	reverse transfer capacitance			-	88	120	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω; V _{GS} = 5 V; R _{G(ext)} = 10 Ω; T _j = 25 °C		-	13	20	ns
t _r	rise time			-	120	168	ns
t _{d(off)}	turn-off delay time			-	58	87	ns
t _f	fall time			-	57	86	ns
L _D	internal drain inductance	from drain lead 6 mm from package to centre of die; T _j = 25 °C		-	4.5	-	nH

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		from upper edge of drain tab to centre of die; $T_j = 25\text{ }^{\circ}\text{C}$	-	2.5	-	nH
L_S	internal source inductance	from source lead to source bond pad; $T_j = 25\text{ }^{\circ}\text{C}$	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 10\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 17	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	53.7	-	ns
Q_r	recovered charge	$V_{DS} = 30\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$	-	126	-	nC

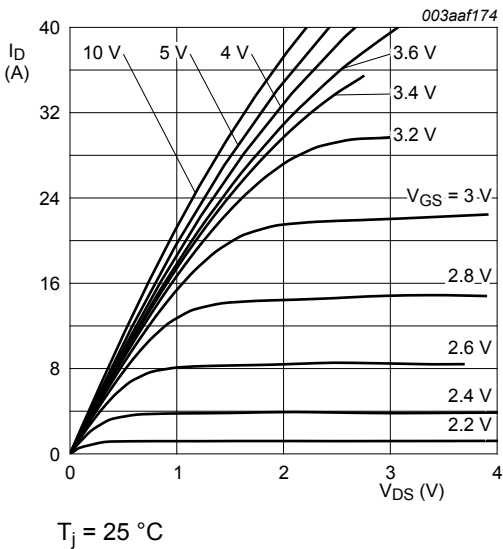


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

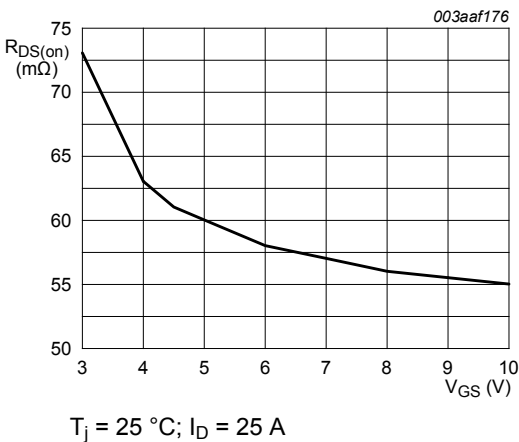


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

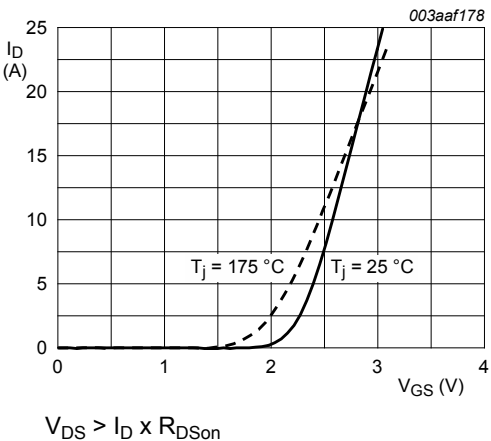


Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

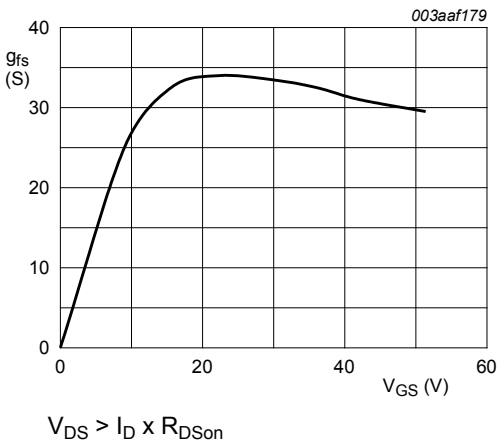


Fig. 9. Forward transconductance as a function of drain current; typical values

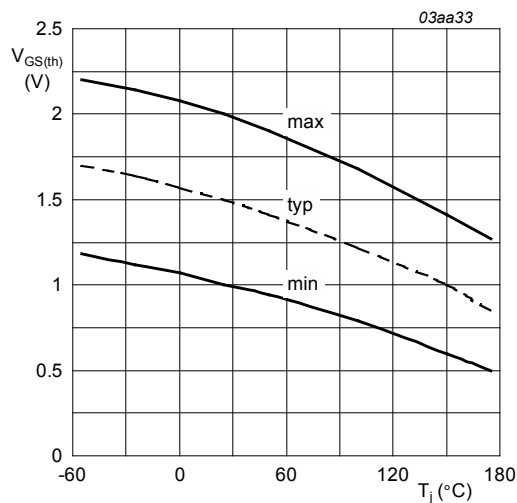
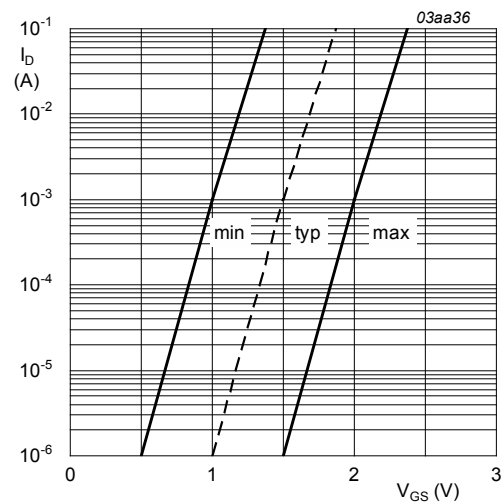


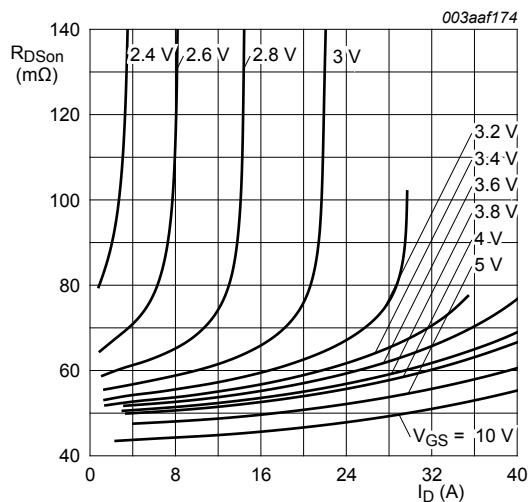
Fig. 10. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$



$$T_j = 25 \text{ °C}; V_{DS} = 5 \text{ V}$$

Fig. 11. Sub-threshold drain current as a function of gate-source voltage



$$T_j = 25 \text{ °C}$$

Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

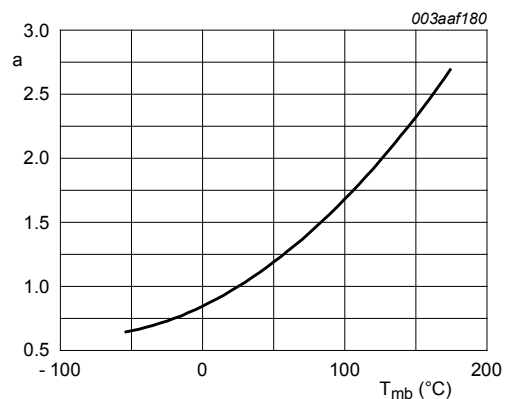


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)(25 \text{ °C})}}$$

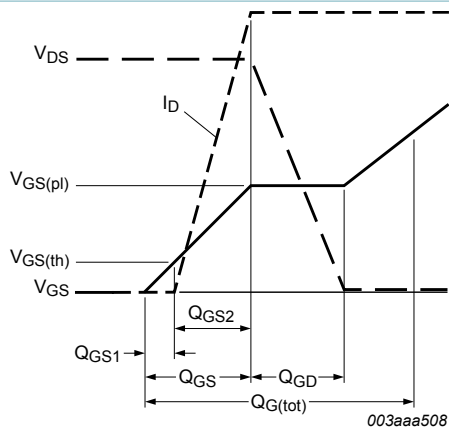
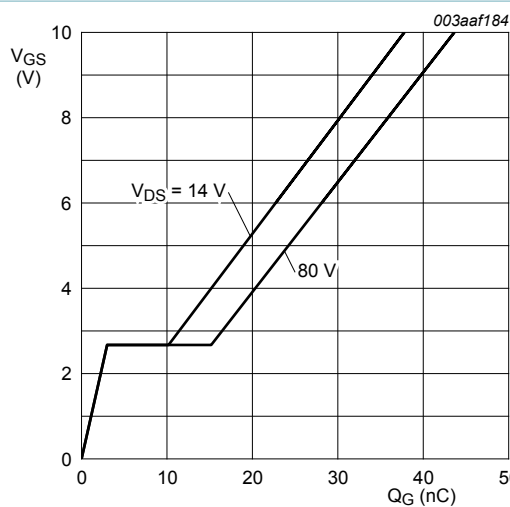
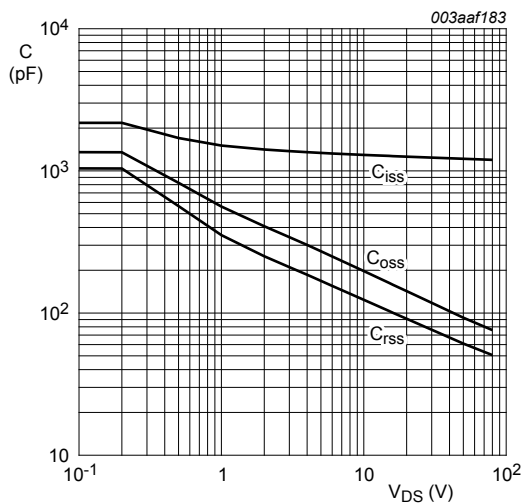


Fig. 14. Gate charge waveform definitions



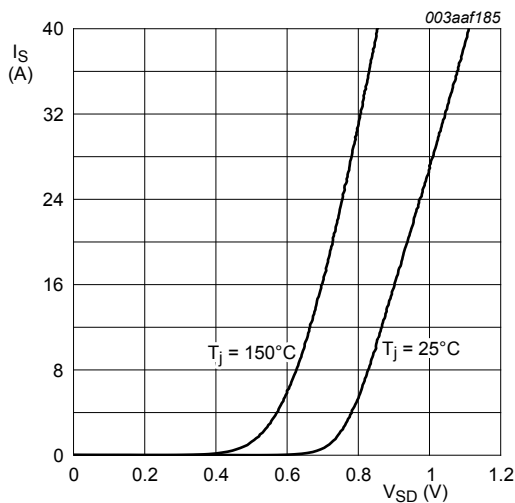
$T_j = 25\text{ }^{\circ}\text{C}$; $I_D = 10\text{ A}$

Fig. 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig. 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

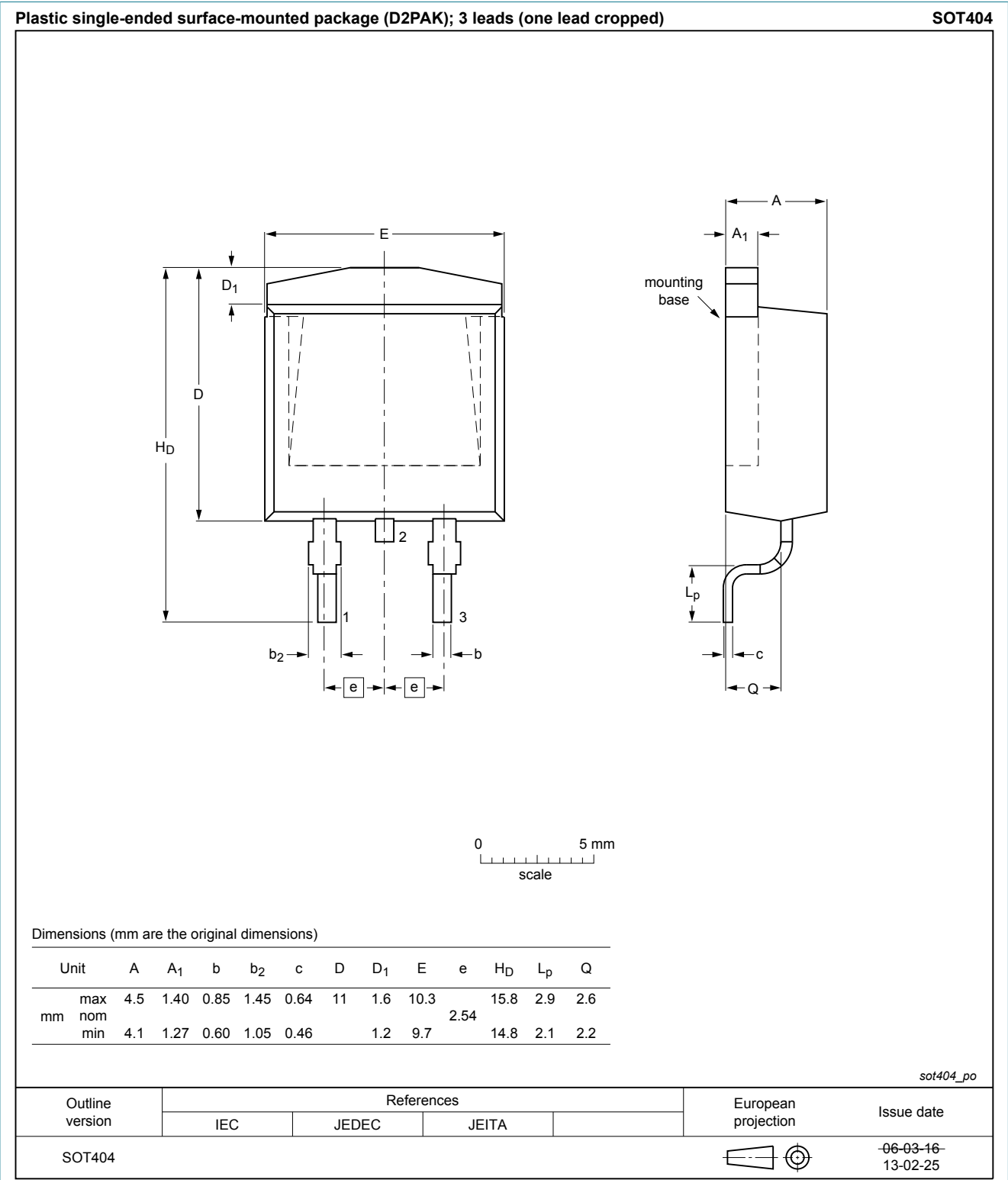


Fig. 18. Package outline D2PAK (SOT404)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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