

N-channel 650 V, 0.073 Ω typ., 30 A MDmesh M5 Power MOSFET in a TO247-4 package

Datasheet - preliminary data

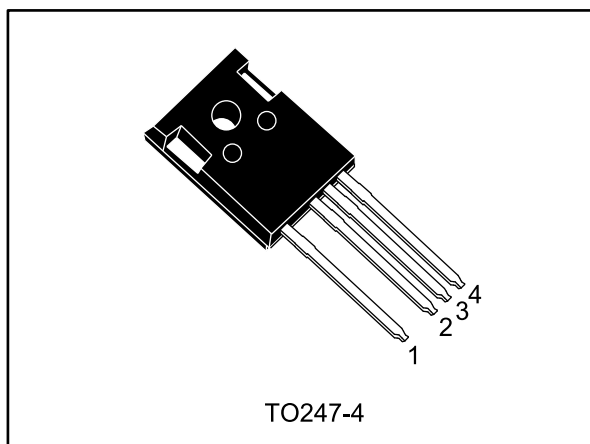
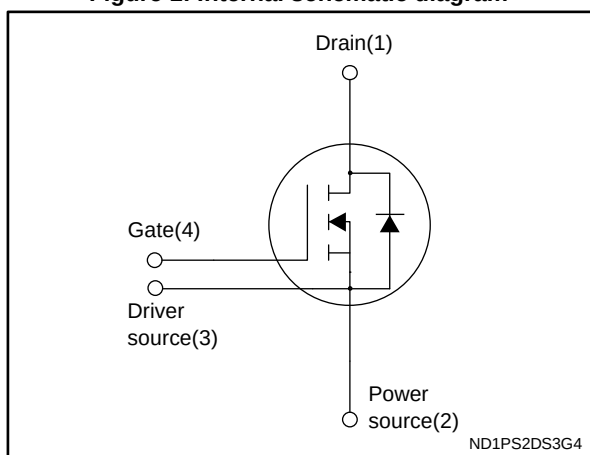


Figure 1: Internal schematic diagram



Features

Order code	$V_{DS} @ T_{Jmax}$	$R_{DS(on)} max$	I_D
STW38N65M5-4	710 V	0.095 Ω	30 A

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- High efficiency switching applications:
 - Servers
 - PV inverters
 - Telecom infrastructure
 - Multi kW battery chargers

Description

This device is an N-channel Power MOSFET based on the MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STW38N65M5-4	38N65M5	TO247-4	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	30	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	19	A
$I_{DM}^{(1)}$	Drain current (pulsed)	120	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	190	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	- 55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature range		

Notes:

⁽¹⁾ Pulse width limited by safe operating area

⁽²⁾ $I_{SD} \leq 30\text{ A}$, $di/dt = 400\text{ A}/\mu\text{s}$, $V_{DS(\text{peak})} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$

⁽³⁾ $V_{DS} \leq 520\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.66	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^{\circ}\text{C}/\text{W}$

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	8	$^{\circ}\text{C}/\text{W}$
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	660	mJ

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 650\text{ V}$			1	μA
		$V_{GS} = 0$, $V_{DS} = 650\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0$, $V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 10\text{ V}$, $I_D = 15\text{ A}$		0.073	0.095	Ω

Notes:

⁽¹⁾ Defined by design, not subject to production test

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	3000	-	pF
C_{oss}	Output capacitance		-	74	-	pF
C_{rss}	Reverse transfer capacitance		-	5.8	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0$, $V_{DS} = 0\text{ to }520\text{ V}$	-	244	-	pf
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	70	-	pf
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	2.4	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 15\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 16: "Gate charge test circuit")	-	71	-	nC
Q_{gs}	Gate-source charge		-	18	-	nC
Q_{gd}	Gate-drain charge		-	30	-	nC

Notes:

⁽¹⁾ $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⁽²⁾ $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(V)}$	Voltage delay time	$V_{DD} = 400\text{ V}$, $I_D = 20\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 17: "Test circuit for inductive load switching and diode recovery times" and Figure 20: "Switching time waveform")	-	60	-	ns
$t_{r(V)}$	Voltage rise time		-	8	-	ns
$t_{f(I)}$	Current fall time		-	8	-	ns
$t_{c(off)}$	Crossing time		-	11.5	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		30	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		120	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 30\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 30\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see Figure 20: "Switching time waveform")	-	382		ns
Q_{rr}	Reverse recovery charge		-	6.6		μC
I_{RRM}	Reverse recovery current		-	35		A
t_{rr}	Reverse recovery time	$I_{SD} = 30\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 20: "Switching time waveform")	-	522		ns
Q_{rr}	Reverse recovery charge		-	10.3		μC
I_{RRM}	Reverse recovery current		-	40		A

Notes:⁽¹⁾ Pulse width limited by safe operating area⁽²⁾ Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.2 Electrical characteristics (curve)

Figure 2: Safe operating area

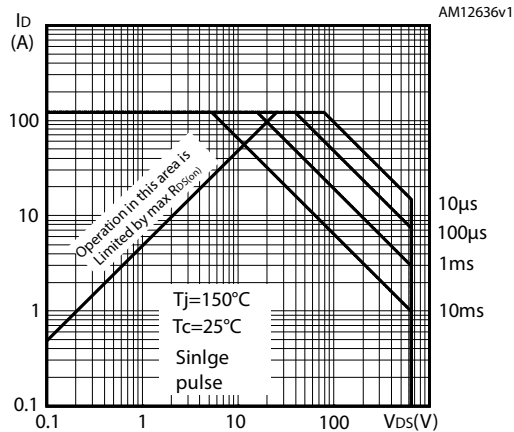


Figure 3: Thermal impedance

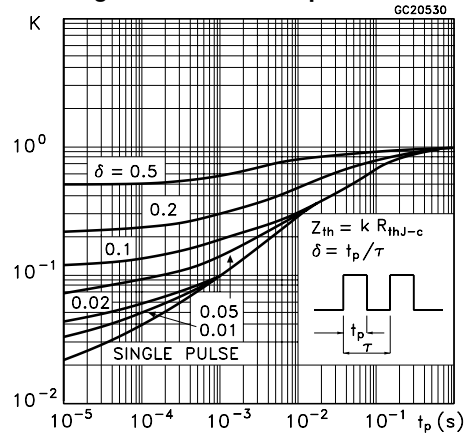


Figure 4: Output characteristics

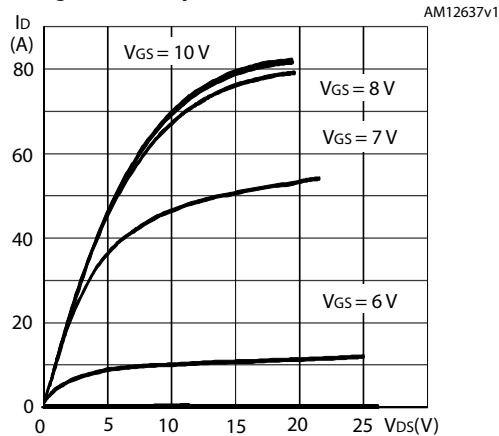


Figure 5: Transfer characteristics

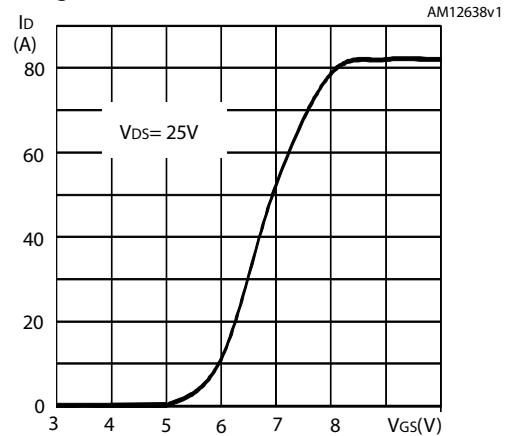


Figure 6: Gate charge vs gate-source voltage

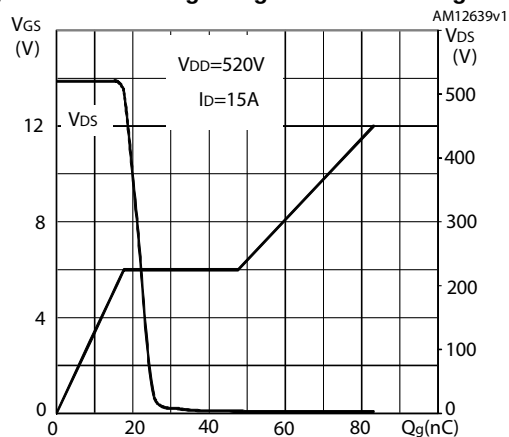


Figure 7: Static drain-source on-resistance

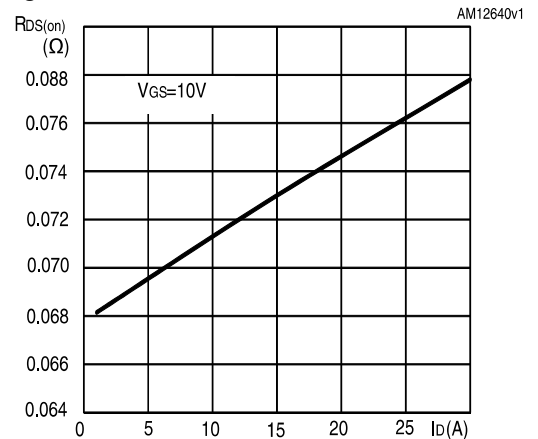


Figure 8: Capacitance variations

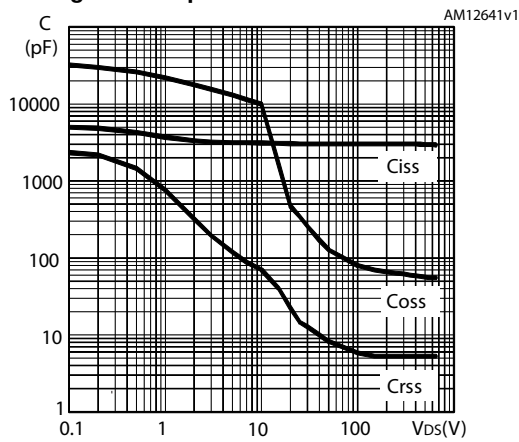


Figure 9: Output capacitance stored energy

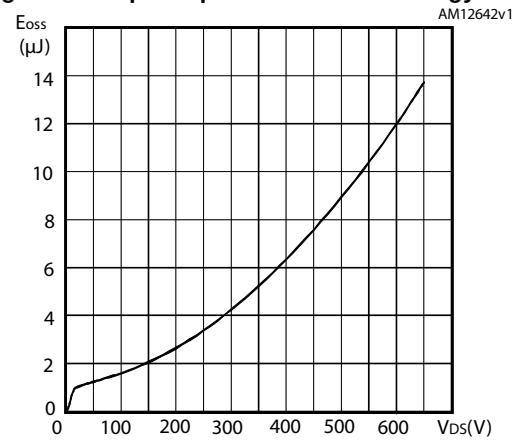


Figure 10: Normalized gate threshold voltage vs temperature

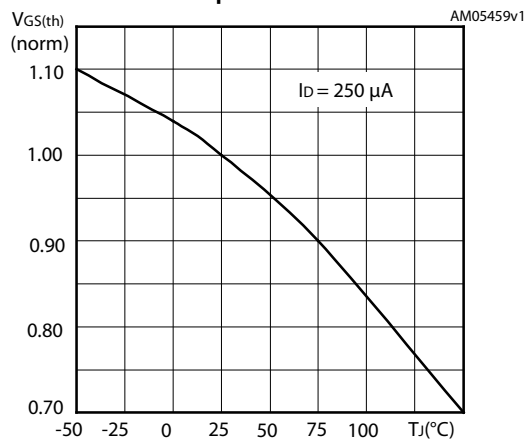


Figure 11: Normalized on-resistance vs temperature

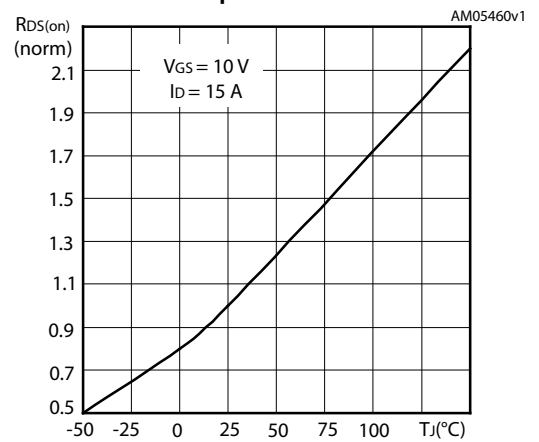


Figure 12: Source-drain diode forward characteristics

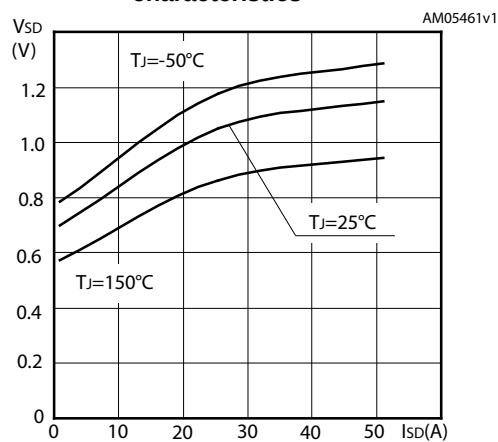
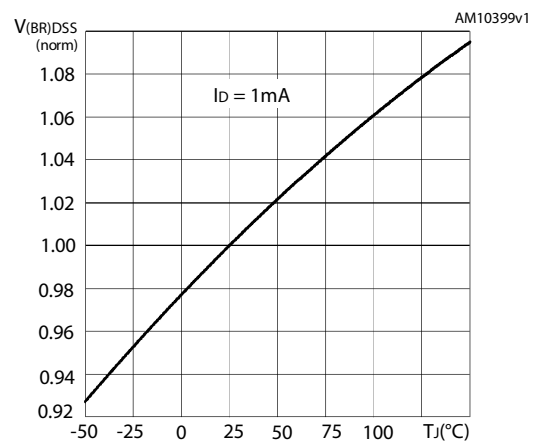
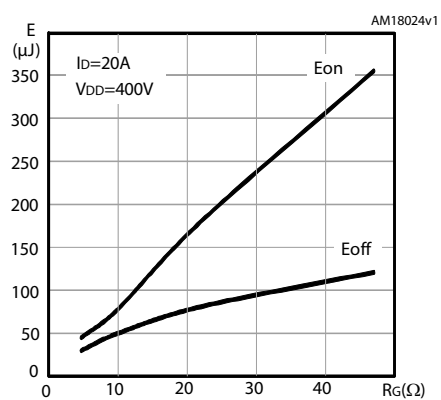
Figure 13: Normalized $V_{(BR)DSS}$ vs temperature

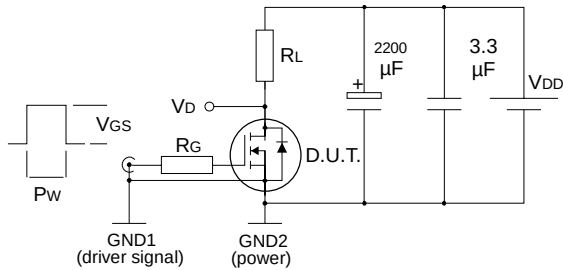
Figure 14: Switching energy vs gate resistance



E_{on} including reverse recovery of a SiC diode.

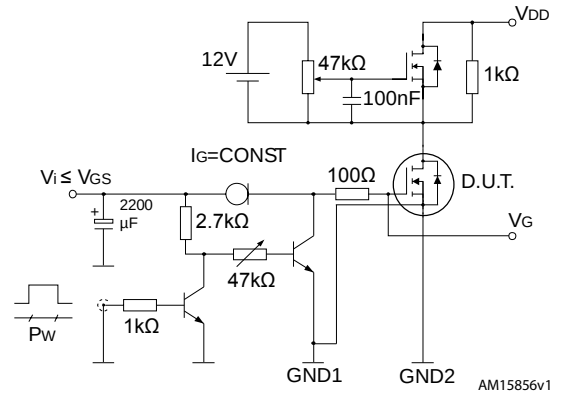
3 Test circuits

Figure 15: Switching times test circuit for resistive load



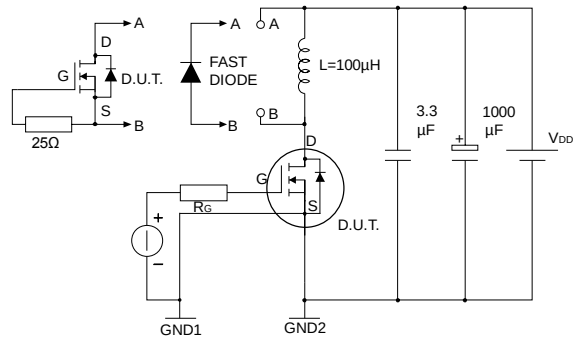
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Figure 16: Gate charge test circuit



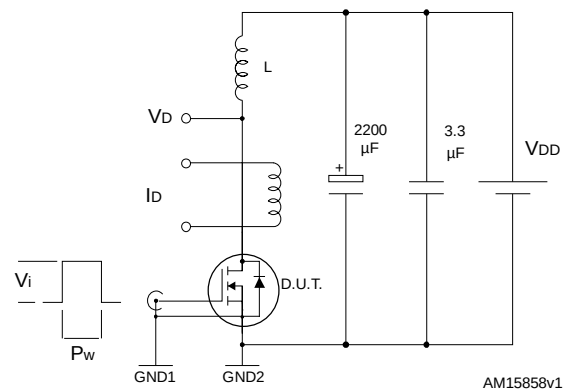
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Figure 17: Test circuit for inductive load switching and diode recovery times



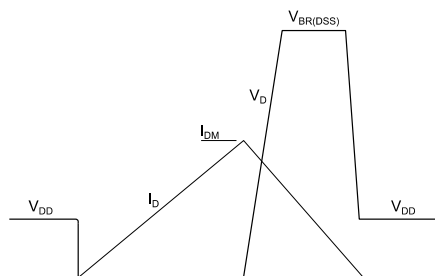
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Figure 18: Unclamped inductive load test circuit



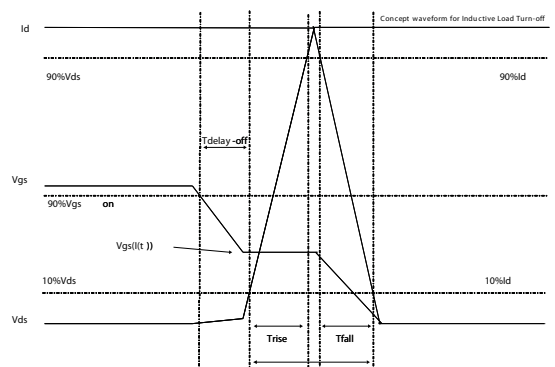
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Figure 19: Unclamped inductive waveform



AM01472v1

Figure 20: Switching time waveform



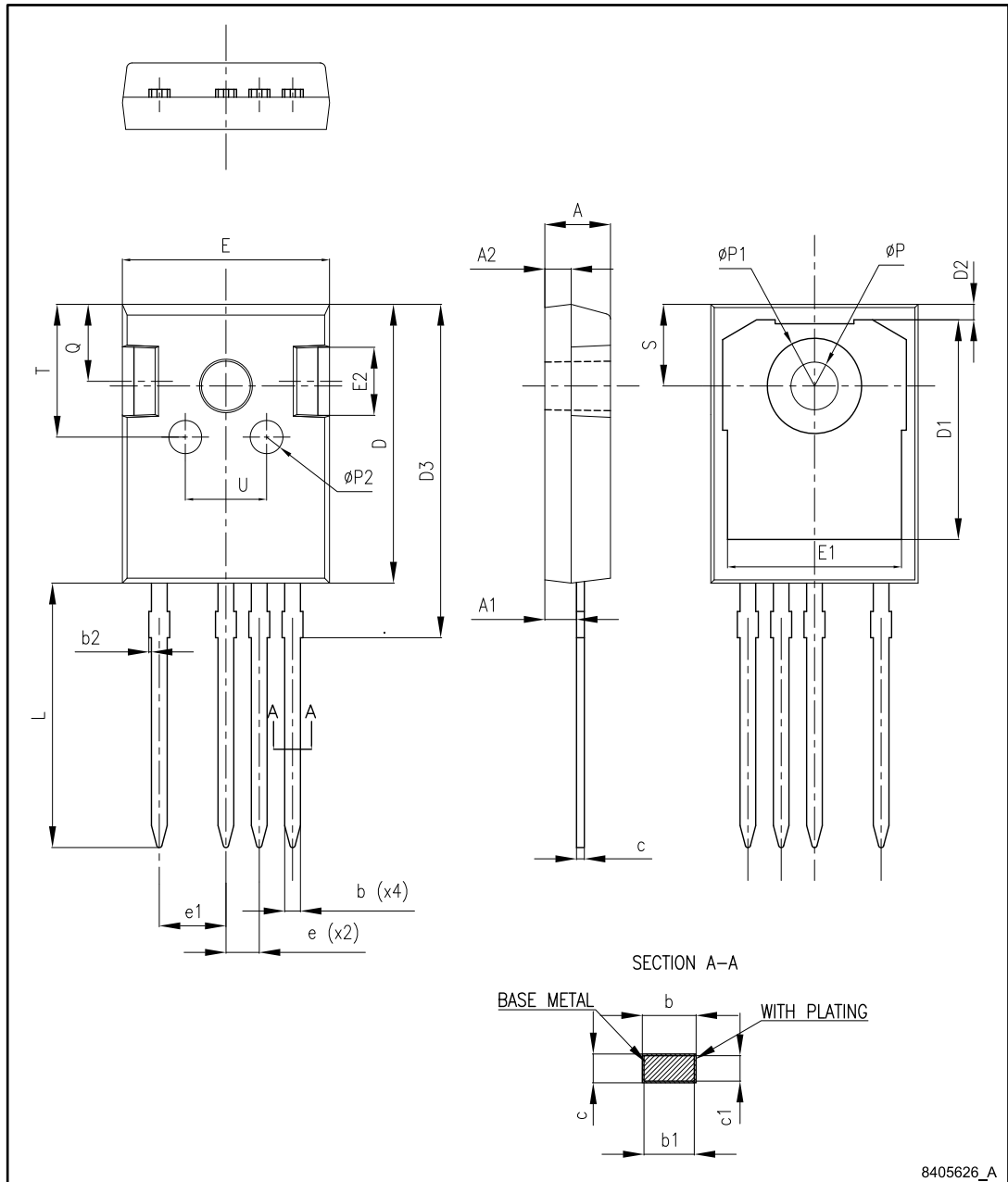
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO247-4 package information

Figure 21: TO247-4 package outline



8405626_A

Table 9: TO247-4 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.29
b1	1.15	1.20	1.25
b2	0		0.20
c	0.59		0.66
c1	0.58	0.60	0.62
D	20.90	21.00	21.10
D1	16.25	16.55	16.85
D2	1.05	1.20	1.35
D3	24.97	25.12	25.27
E	15.70	15.80	15.90
E1	13.10	13.30	13.50
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	2.44	2.54	2.64
e1	4.98	5.08	5.18
L	19.80	19.92	20.10
P	3.50	3.60	3.70
P1			7.40
P2	2.40	2.50	2.60
Q	5.60		6.00
S		6.15	
T	9.80		10.20
U	6.00		6.40

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
20-Apr-2016	1	Initial release.

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